

# TPS55340EVM-148, 8V to 24V Input, 5V Output Flyback Evaluation Module

This user's guide contains information for the TPS55340EVM-148 evaluation module (also called PWR148) as well as the TPS55340 DC/DC converter. The document includes the performance specifications, schematic, and the bill of materials for the TPS55340EVM-148.

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Background www.ti.com

# 1 Background

The TPS55340 DC/DC Regulator is used typically in a boost topology, however this EVM demonstrates it in a flyback topology. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module demonstrates the performance of the TPS55340 in an example application and can accommodate evaluation of other flyback applications supported by the TPS55340. The switching frequency is externally set at a nominal 350kHz. The 40V, 5A, low-side MOSFET is incorporated inside the TPS55340 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS55340 to achieve high efficiencies. The compensation components are external to the integrated circuit (IC). In this example application the absolute maximum input voltage for the TPS55340EVM-148 is 24V.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Maximum Output Current
TPS55340EVM-148	$V_{IN} = 8V$ to 24V, 12V nominal	$I_{OUT}$ max = 2.5A

# 2 Performance Specification Summary

Table 2 provides a summary of the TPS55340EVM-148 performance specifications. The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 2. Performance Specification Summary** 

Specification	Test Condi	tions	Min	Тур	Max	Unit
V <sub>IN</sub> voltage range			8	12	24	V
No Load Input Current	oad Input Current I <sub>OUT</sub> = 0A, V <sub>IN</sub> = 12V			6.3		mA
Output voltage set point				5		V
Line regulation	$I_{OUT} = 2.5A$ , $V_{IN} = 8V$ to 24V			±0.1		%
Operating frequency				350		kHz
Output current range			.001		2.5	Α
Output over current limit <sup>(1)</sup>	V <sub>IN</sub> = 8V			3.4		Α
Output over current limit <sup>(1)</sup>	V <sub>IN</sub> = 24V			4.8		Α
Load regulation	I <sub>OUT</sub> = 1mA to 2.5A, V <sub>IN</sub> = 8V to 24V			±0.1		%
	L 625mA to 4.075A \/ 42\/	Voltage change		-140		mV
Load transient response	$I_{OUT} = 625$ mA to 1.875A, $V_{IN} = 12$ V	Recovery time		500		μs
Load transferit response	I <sub>OUT</sub> = 1.875mA to 625mA, V <sub>IN</sub> = 12V	Voltage change		60		mV
		Recovery time		500		μs
Loop bandwidth	I <sub>OUT</sub> = 2.5A, V <sub>IN</sub> = 12V			7.8		kHz
Phase margin	I <sub>OUT</sub> = 2.5A, V <sub>IN</sub> = 12V			56		0
Output ripple voltage	I <sub>OUT</sub> = 2.5A, V <sub>IN</sub> = 12V			75		mVpp
Peak efficiency	I <sub>OUT</sub> = 0.9A, V <sub>IN</sub> = 12V	<sub>OUT</sub> = 0.9A, V <sub>IN</sub> = 12V		87.9		%
Output current DCM threshold	V <sub>IN</sub> = 12V			340		mA

<sup>(1)</sup> The output over current limit is dependent on the input voltage and based on peak current limit of the TPS55340.

## 3 Modifications

These evaluation modules provide access to the features of the TPS55340 in a flyback topology. Modifications to this module are possible to support other flyback applications.

## 3.1 Output Voltage Set Point

The resistor divider network of R8 and R14 sets the output voltage. Keep R14 fixed at or close to  $10k\Omega$ . To change the output voltage of the EVM, change the value of resistor R8. Calculate the value of R8 for a specific output voltage by using Equation 1 and the 1.24V  $V_{REF}$  of U3. For output voltages greater than 6V, it is recommended to use a TL431 for U3 with  $V_{REF} = 2.495V$  and 36V maximum recommended output voltage.



$$R8 = R14 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$
(1)

Note that  $V_{IN}$  must be in a range so that the on-time is greater than the minimum controllable on-time (77ns typical), and the maximum duty cycle is less than 89% minimum and 93% typical. Additionally, for a flyback application it is recommended to limit the duty cycle to 50% max to reduce stress on external components and avoid sub-harmonic operation inherent to current mode control. The duty cycle in continuous-conduction mode (CCM) can be calculated with Equation 2, where  $V_D$  is the forward voltage drop of the secondary Schottky diode (D1) and N is the primary to secondary turns ratio of the transformer.

$$D_{CCM} = \frac{\left(V_{OUT} + V_{D}\right) \times N}{V_{IN} + \left(V_{OUT} + V_{D}\right) \times N}$$
(2)

After adjusting the output voltage, the maximum input voltage must be taken into consideration. The voltage on the internal FET, the SW pin, is equal to the sum of the input voltage and the output voltage reflected through the transformer. Additional tolerance is recommended to accommodate ringing typical of a flyback supply. By using Equation 3, you can estimate the voltage across the internal FET with a 20% tolerance. This must be less than the 40V absolute maximum rating.

$$V_{FET} = \frac{V_{IN} \max + (V_{OUT} + V_D) \times N}{0.8}$$
(3)

# 3.2 Maximum Output Current

After adjusting input or output voltage settings, verify the maximum output current per Equation 4 below, where  $I_{\text{LIM}}$  is the peak current limit of the TPS55340, Dmax is the CCM duty cycle with the minimum input voltage and  $\eta_{\text{EST}}$  is the estimated maximum load current efficiency.

$$I_{OUT} max = \left(I_{LIM} - \frac{V_{IN} min \times Dmax}{2 \times L_{PRI} \times f_{SW}}\right) \times \frac{V_{IN} min \times Dmax \times \eta_{EST}}{V_{OUT}}$$

$$(4)$$

#### 3.3 Soft-start Time

The primary soft-start time can be adjusted by changing the value of C12. The EVM uses C12 =  $0.1~\mu F$  to control the ramp of the COMP pin voltage. A larger capacitance increases the soft-start time while a smaller capacitance decreases it. Additionally C18 provides a soft-start for the secondary side reference based on the RC time constant of C18 and R6. The EVM uses C18 =  $1.0~\mu F$  to avoid any overshoot during start up. It is recommended to have the soft-start for the secondary side reference be longer than the primary side soft-start to avoid overshoot. A higher RC time constant increases the soft-start time while a lower RC time constant decreases it.

## 3.4 Other Modifications

When changing the switching frequency, input/output voltage range, transformer, output capacitors or compensation additional design changes may be needed. When making design changes it is recommended to replace the transformer with one optimized for the application's requirements for best performance.

## 4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS55340EVM-148 evaluation module. Included are test results typical for the evaluation module covering efficiency, output voltage regulation, load transients, loop response, output voltage ripple, input voltage ripple, start-up and shutdown. Measurements are for an ambient temperature of 25°C.



Test Setup and Results www.ti.com

# 4.1 Input/Output Connections

The TPS55340EVM-148 is provided with input/output connectors and test points as shown in Table 3. Connect a power supply capable of supplying 5A to J6 through a pair of 20 AWG wires. The jumper across JP1 in the ON position (1-2) must be in place. Connect the load to J7 through a pair of 20 AWG wires. The maximum load current capability must be at least 2.5A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the  $V_{\rm IN}$  input voltage with TP3 providing a convenient ground reference. Use TP2 to monitor the output voltage with TP4 as the ground reference.

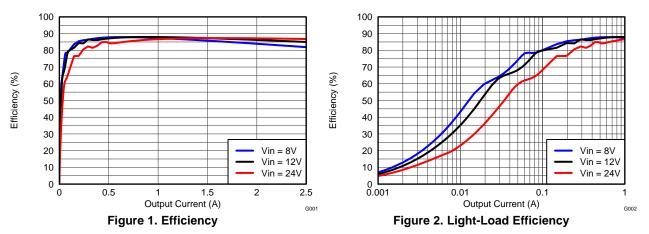
**Table 3. EVM Connectors and Test Points** 

Reference Designator	Function
J1	V <sub>IN</sub> input voltage connector. (See Table 1 for V <sub>IN</sub> range.)
J2	V <sub>OUT</sub> output voltage connector
J3	2-pin header for primary side GND connections
J4	2-pin header for secondary side GND connections
J5	2-pin header for SYNC signal and GND connections
JP1	3-pin header for enable. Install jumper from pins 1-2 to enable or from pins 2-3 to disable.
TP1	V <sub>IN</sub> test point
TP2	V <sub>OUT</sub> test point
TP3	GND test point at V <sub>IN</sub> connector
TP4	GND test point at V <sub>OUT</sub> connector
TP5	SW test point
TP6	Test point between optocoupler, voltage divider network and output. Used for inner loop response measurements.
TP7	Test point between voltage divider network and output. Used for outer loop response measurements.
TP8	COMP test point



# 4.2 Efficiency

The efficiency of this EVM peaks at a load current of about 600mA at 8V input and 1.5A at 24V input, then decreases as the load current increases toward full load. Figure 1 shows the efficiency for the TPS55340EVM-148. Figure 2 shows the light-load efficiency by using a semi log scale.



The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

# 4.3 Output Voltage Line and Load Regulation

Figure 3 shows the load regulation for the TPS55340EVM-148. Figure 4 shows the line regulation for the TPS55340EVM-148 with a 2.5A load.

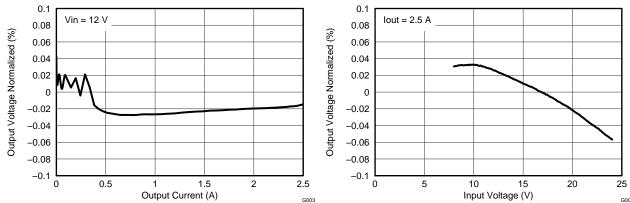


Figure 3. Output Voltage Load Regulation

Figure 4. Output Voltage Line Regulation



180

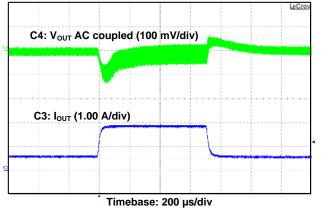
Gain

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# 4.4 Load Transient and Loop Response

Figure 5 show the TPS55340EVM-148 response to load transients. The current step is from 25% to 75% of maximum rated load at  $V_{IN}$  = 12V. The current step slew rate is 100 mA/ $\mu$ s. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 6 shows the TPS55340EVM-148 loop-response characteristics. Gain and phase plots are shown for  $V_{IN}$  voltage of 12V with load current of 2.5A. The loop-response measurement is taken by replacing R3 with a 49.9- $\Omega$  resistor. The signal is then injected across it with test points TP2 and TP6.



40 120 20 60 Gain (dB) -20 -60 -40 -120 lout = 2.5 A Vin = 12 V -60 10 100 100k 1M Frequency (Hz)

Figure 5. Load Transient Response

Figure 6. Loop Response



# 4.5 Output Voltage Ripple

Figure 7 shows the TPS55340EVM-148 output voltage ripple and switching waveform. The output current is the rated full load of 2.5A and  $V_{IN} = 12V$ . The ripple voltage is measured directly across C6.

Figure 8 shows the TPS55340EVM-148 output voltage ripple and switching waveform while operating in discontinuous conduction mode (DCM). The input voltage is 12V and the output is loaded with  $20\Omega$  (250mA).

The TPS55340 features pulse-skipping for output regulation when operating at light loads. Figure 9 shows the output voltage ripple and the pulse-skipping at SW. The input voltage is 24V and the output has no load.

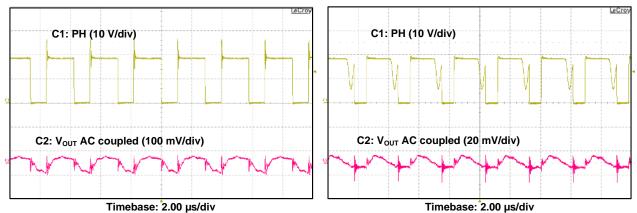


Figure 7. Maximum Load Output Voltage Ripple

Figure 8. DCM Output Voltage Ripple

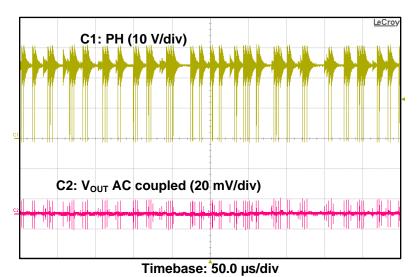


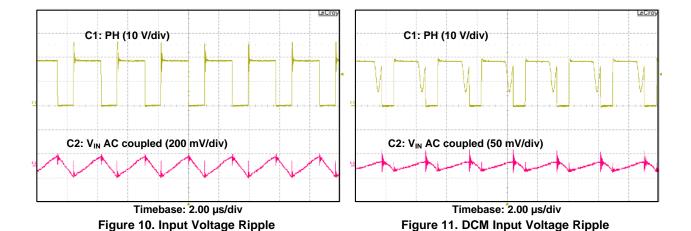
Figure 9. Pulse-Skipping Output Voltage Ripple

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# 4.6 Input Voltage Ripple

Figure 10 shows the TPS55340EVM-148 input voltage ripple. The output current is the rated full load of 2.5A at  $V_{IN}$  = 12V. The ripple is measured directly across the input capacitor C2.

Figure 11 shows the TPS55340EVM-148 input voltage ripple operating in DCM. The input voltage is 12V and the output is loaded with  $20\Omega$  (250mA).



# 4.7 Voltage Overshoot on SW Pin

Figure 12 shows the voltage overshoot on the SW pin with 200MHz bandwidth. This is measured with 24V input voltage and 2.5A output current.

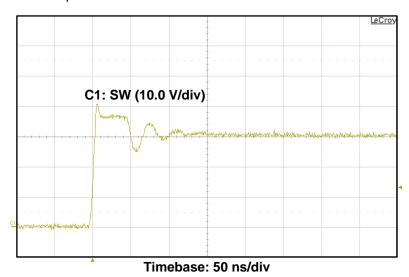


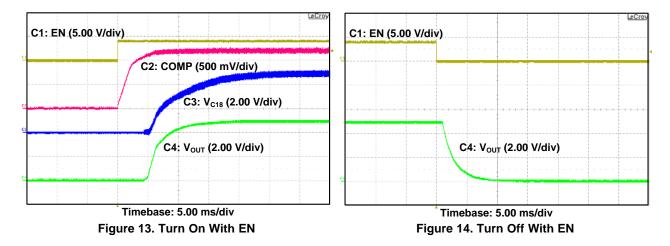
Figure 12. SW Pin Voltage Overshoot



#### 4.8 Turn On and Off with EN

Figure 13 shows the start-up waveforms for the TPS55340EVM-148. The input voltage is 12V, the EN goes high, the COMP voltage rises, the device begins switching and the output voltage ramps from 0V to 5V. The load is  $5\Omega$  (1A).

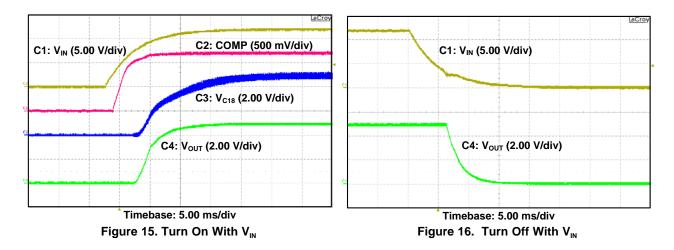
Figure 14 shows the shutdown waveforms for the TPS55340EVM-148. The input voltage is 12V, the EN goes low and the output voltage ramps from 5V to 0V. The load is  $5\Omega$  (1A).



# 4.9 Turn On and Off with $V_{IN}$

Figure 15 shows the start-up waveforms for the TPS55340EVM-148. The input voltage ramps with the input voltage power supply and EN is tied to  $V_{IN}$ .  $V_{IN}$  ramps up, the COMP voltage rises, the converter starts switching and the output voltage ramps to 5V. The load is  $5\Omega$  (1A).

Figure 16 shows the shutdown waveforms for the TPS55340EVM-148. The input voltage ramps down with the input voltage power supply and EN is tied to  $V_{IN}$ . When  $V_{IN}$  is less than the 2.5V typical UVLO, the converter stops switching and the output voltage ramps down. The load is  $5\Omega$  (1A).





Board Layout www.ti.com

# 5 Board Layout

This section provides a description of the TPS55340EVM-148 board layout and layer illustrations.

## 5.1 Layout

The board layout for the TPS55340EVM-148 is shown in Figure 17 through Figure 21. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and two internal layers are 2-oz copper.

The top layer contains the main power traces for  $V_{IN}$ ,  $V_{OUT}$ , and SW. Also on the top layer are connections for the remaining pins of the TPS55340 and a large area filled with ground. The internal layers and bottom are primarily ground with additional fill areas for  $V_{IN}$ , and  $V_{OUT}$ . The top-side ground traces connect to the bottom and internal ground planes with multiple vias placed around the board. Nine vias directly under the TPS55340 device provide a thermal path from the top-side ground plane to the bottom-side ground plane.

Place the output decoupling capacitors (C5-C8) next to D1 and the secondary winding of T1. The copper area of the SW node on the primary side is kept small to minimize noise. The vias near the diode, D1, on the  $V_{\text{OUT}}$  plane aid with thermal dissipation. Additionally, keep the voltage setpoint resistor divider components close to U3. The voltage divider network ties to the output voltage at the point of regulation, the copper  $V_{\text{OUT}}$  trace near TP2. For the TPS55340, an additional input bulk capacitor may be necessary, depending on the EVM connection to the input supply. Critical analog circuits such as the frequency set resistor, soft-start capacitor, and compensation components terminate to ground by using a separate ground trace on the top and bottom connected power ground pour only at one point directly under the IC.

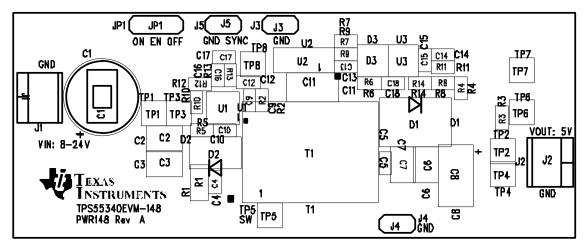


Figure 17. Top-Side Assembly and Silk

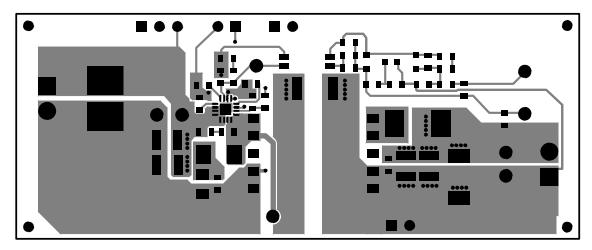


Figure 18. Top-Side Layout



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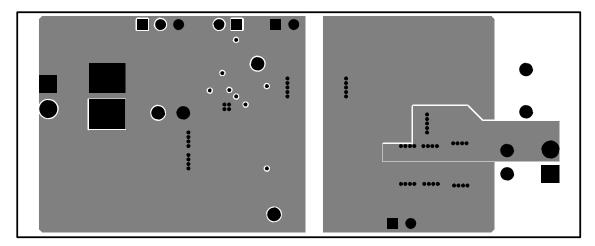


Figure 19. Internal Layer-1 Layout

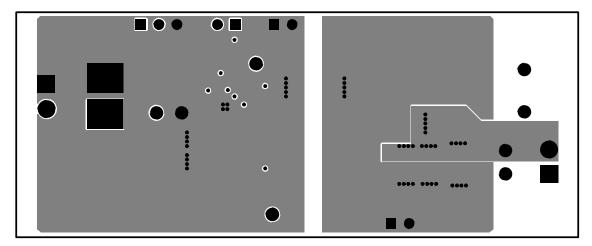


Figure 20. Internal Layer-2 Layout

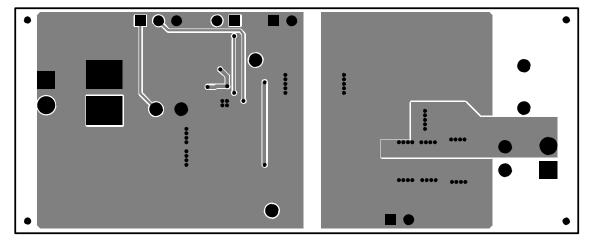


Figure 21. Bottom-Side Layout



Schematic and Bill of Materials www.ti.com

# 6 Schematic and Bill of Materials

This section presents the TPS55340EVM-148 schematic and bill of materials.

# 6.1 Schematic

Figure 22 is the schematic for the TPS55340EVM-148.

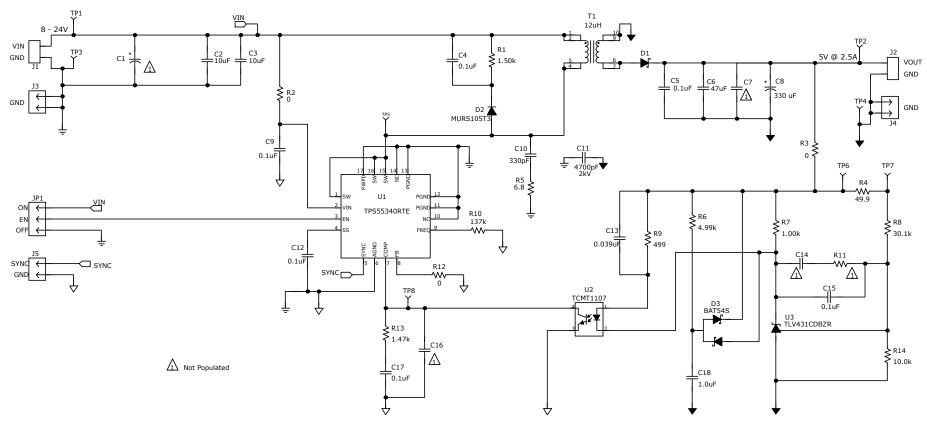


Figure 22. Schematic



# 6.2 Bill of Materials

Table 4 presents the bill of materials for the TPS55340EVM-148.

**Table 4. Bill of Materials** 

0 C1 1 C6 0 C7 1 C8 1 C10 1 C11 1 C13 1 C18 4 C4, C9, 0 C14, C 2 C2-3 2 C5, C1: 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10 0 R11	9, C15, C17 (C16 (Fig. 12 (Fig	Open 47 μF Open 330 μF 330 μF 4700 pF 0.039 μF 1.0 μF 0.1 μF 0.1 μF MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 kΩ 0 Ω	Capacitor Capacitor, ceramic, 10 V, X5R, 10% Capacitor, ceramic Capacitor, low ESR, 10 V, ±20 %  Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 16 V, X7R, 20% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, Ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 3-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	Multiple sizes 1210 1210 D4 0603 1812 0603 0603 0603 1210 0603 SMC SMB SOT23 0.27 × 0.25 in 0.100 in × 2	Engineering Only Std Std 10TPE330M 6TPE330ML alt. Std	Engineering Only Std Std Sanyo Std Std Std Std Std Std Std Std TDK Std
0 C7 1 C8 1 C10 1 C11 1 C13 1 C18 4 C4, C9, 0 C14, C; 2 C2-3 2 C5, C1; 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	9, C15, C17 (C16 (Fig. 12 (Fig	Open 330 μF 330 μF 4700 pF 0.039 μF 1.0 μF 0.1 μF Open 10 μF 0.1 μF MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 ΚΩ	Capacitor, ceramic  Capacitor, low ESR, 10 V, ±20 %  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 2 kV, X7R, 10%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 16 V, X7R, 20%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 50 V, X5R, 10%  Capacitor, ceramic, 50 V, X5R, 10%  Capacitor, ceramic, 10 V, X7R, 10%  Diode, Schottky, 4 A, 40 V  Diode, Ultra-fast rectifier, 1 A, 50 V  Diode, dual Schottky, 200 mA, 30 V  Terminal block, 2-pin, 6-A, 3.5mm  Header, male 2-pin, 100 mil spacing  Header, male 3-pin, 100 mil spacing	1210 D4  0603 1812 0603 0603 0603 0603 1210 0603 SMC SMB SOT23 0.27 × 0.25 in	Std  10TPE330M 6TPE330ML alt.  Std  Std  Std  C1608X7R1C105M  Std  Std  Std  Std  Std  MURS105T3G  BAT54STA  ED555/2DS	Std Sanyo  Std Std Std Std TDK Std
1 C8  1 C10  1 C11  1 C13  1 C18  4 C4, C9, O C14, C  2 C2-3  2 C5, C1:  1 D1  1 D2  1 D3  2 J1-2  3 J3-5  1 JP1  1 R1  1 R3  1 R4  1 R5  1 R6  1 R7  1 R8  1 R9  1 R10	9, C15, C17 (C16 (Fig. 12 (Fig	330 μF  330 μF  4700 pF  4700 pF  0.039 μF  1.0 μF  0.1 μF  Open  10 μF  0.1 μF  MBRS340T3G  MURS105T3G  BAT54STA  ED555/2DS  PEC02SAAN  PEC03SAAN  1.50 ΚΩ	Capacitor, low ESR, 10 V, ±20 %  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 16 V, X7R, 20%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 50 V, X5R, 10%  Capacitor, ceramic, 50 V, X5R, 10%  Capacitor, ceramic, 10 V, X7R, 10%  Diode, Schottky, 4 A, 40 V  Diode, ultra-fast rectifier, 1 A, 50 V  Diode, dual Schottky, 200 mA, 30 V  Terminal block, 2-pin, 6-A, 3.5mm  Header, male 2-pin, 100 mil spacing  Header, male 3-pin, 100 mil spacing	D4  0603  1812  0603  0603  0603  1210  0603  SMC  SMB  SOT23  0.27 × 0.25 in	10TPE330M 6TPE330ML alt. Std Std Std C1608X7R1C105M Std Std Std Std Std Std STD MBRS340T3G MURS105T3G BAT54STA ED555/2DS	Sanyo  Std  Std  Std  Std  TDK  Std  Std  Std  Std  Std  Std  Std  St
1 C10 1 C11 1 C13 1 C18 4 C4, C9, 0 C14, C 2 C2-3 2 C5, C1: 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	9, C15, C17 (C16 (C16 (C16 (C16 (C16 (C16 (C16 (C16	330 pF 4700 pF 0.039 μF 1.0 μF 0.1 μF Open 10 μF 0.1 μF MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 ΚΩ	Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 2 kV, X7R, 10%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 16 V, X7R, 20%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 50 V, X7R, 10%  Capacitor, ceramic, 50 V, X5R, 10%  Capacitor, ceramic, 10 V, X7R, 10%  Diode, Schottky, 4 A, 40 V  Diode, ultra-fast rectifier, 1 A, 50 V  Diode, dual Schottky, 200 mA, 30 V  Terminal block, 2-pin, 6-A, 3.5mm  Header, male 2-pin, 100 mil spacing  Header, male 3-pin, 100 mil spacing	0603 1812 0603 0603 0603 1210 0603 SMC SMB SOT23 0.27 × 0.25 in	6TPE330ML alt. Std Std Std C1608X7R1C105M Std Std Std Std MBRS340T3G MURS105T3G BAT54STA ED555/2DS	Std Std Std Std TDK Std Std Std Std Std Std Std StD On Semi Zetex OST
1 C11 1 C13 1 C18 4 C4, C9, 0 C14, C; 2 C2-3 2 C5, C1; 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	9, C15, C17 ( ) C16 ( ) 12 ( ) I   I   I   I   I   I   I   I   I   I	4700 pF 0.039 μF 1.0 μF 0.1 μF Open 10 μF 0.1 μF MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 ΚΩ	Capacitor, ceramic, 2 kV, X7R, 10% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 16 V, X7R, 20% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, Ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	1812 0603 0603 0603 1210 0603 SMC SMB SOT23 0.27 × 0.25 in	Std Std C1608X7R1C105M Std Std Std Std STD MBRS340T3G MURS105T3G BAT54STA ED555/2DS	Std Std TDK Std Std Std Std Std STD On Semi On Semi Zetex OST
1 C13 1 C18 4 C4, C9, 0 C14, C; 2 C2-3 2 C5, C1; 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	9, C15, C17 (C16 (C16 (C16 (C16 (C16 (C16 (C16 (C16	0.039 μF  1.0 μF  0.1 μF  Open  10 μF  0.1 μF  MBRS340T3G  MURS105T3G  BAT54STA  ED555/2DS  PEC02SAAN  PEC03SAAN  1.50 ΚΩ	Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 16 V, X7R, 20% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	0603 0603 0603 1210 0603 SMC SMB SOT23 0.27 × 0.25 in	Std C1608X7R1C105M Std Std Std Std STD MBRS340T3G MURS105T3G BAT54STA ED555/2DS	Std TDK Std Std Std Std Std STD On Semi On Semi Zetex OST
1 C18 4 C4, C9, 0 C14, C; 2 C2-3 2 C5, C1; 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	9, C15, C17 (C16 (C16 (C16 (C16 (C16 (C16 (C16 (C16	1.0 μF  0.1 μF  Open  10 μF  0.1 μF  MBRS340T3G  MURS105T3G  BAT54STA  ED555/2DS  PEC02SAAN  PEC03SAAN  1.50 ΚΩ	Capacitor, ceramic, 16 V, X7R, 20% Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	0603 0603 1210 0603 SMC SMB SOT23 0.27 × 0.25 in	C1608X7R1C105M Std Std Std Std STD MBRS340T3G MURS105T3G BAT54STA ED555/2DS	TDK Std Std Std StD On Semi On Semi Zetex OST
4 C4, C9, 0 C14, C 2 C2-3 2 C5, C1: 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	9, C15, C17 (C16 (C15) (C16) (	0.1 μF Open 10 μF 0.1 μF MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 ΚΩ	Capacitor, ceramic, 50 V, X7R, 10% Capacitor, ceramic Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	0603 0603 1210 0603 SMC SMB SOT23 0.27 x 0.25 in	Std Std Std StD MBRS340T3G MURS105T3G BAT54STA ED555/2DS	Std Std Std STD On Semi On Semi Zetex OST
0 C14, C 2 C2-3 2 C5, C1: 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	C16 (12 (13 (14 (14 (14 (14 (14 (14 (14 (14 (14 (14	Open 10 μF 0.1 μF MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 kΩ	Capacitor, ceramic Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	0603 1210 0603 SMC SMB SOT23 0.27 × 0.25 in	Std Std STD MBRS340T3G MURS105T3G BAT54STA ED555/2DS	Std Std STD On Semi On Semi Zetex OST
2 C2-3 2 C5, C1: 1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	112 (1	10 μF 0.1 μF MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 kΩ	Capacitor, ceramic, 50 V, X5R, 10% Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	1210 0603 SMC SMB SOT23 0.27 × 0.25 in	Std STD MBRS340T3G MURS105T3G BAT54STA ED555/2DS	Std STD On Semi On Semi Zetex OST
2 C5, C1:  1 D1  1 D2  1 D3  2 J1-2  3 J3-5  1 JP1  1 R1  1 R3  1 R4  1 R5  1 R6  1 R7  1 R8  1 R9  1 R10	12 (	0.1 μF  MBRS340T3G  MURS105T3G  BAT54STA  ED555/2DS  PEC02SAAN  PEC03SAAN  1.50 kΩ	Capacitor, ceramic, 10 V, X7R, 10% Diode, Schottky, 4 A, 40 V Diode, ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	0603 SMC SMB SOT23 0.27 × 0.25 in	STD  MBRS340T3G  MURS105T3G  BAT54STA  ED555/2DS	STD On Semi On Semi Zetex OST
1 D1 1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	1 1 1 1	MBRS340T3G MURS105T3G BAT54STA ED555/2DS PEC02SAAN PEC03SAAN	Diode, Schottky, 4 A, 40 V  Diode, ultra-fast rectifier, 1 A, 50 V  Diode, dual Schottky, 200 mA, 30 V  Terminal block, 2-pin, 6-A, 3.5mm  Header, male 2-pin, 100 mil spacing  Header, male 3-pin, 100 mil spacing	SMC SMB SOT23 0.27 × 0.25 in	MBRS340T3G MURS105T3G BAT54STA ED555/2DS	On Semi On Semi Zetex OST
1 D2 1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10		MURS105T3G  BAT54STA  ED555/2DS  PEC02SAAN  PEC03SAAN  1.50 ΚΩ	Diode, ultra-fast rectifier, 1 A, 50 V Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	SMB SOT23 0.27 × 0.25 in	MURS105T3G BAT54STA ED555/2DS	On Semi Zetex OST
1 D3 2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10		BAT54STA ED555/2DS PEC02SAAN PEC03SAAN 1.50 KΩ	Diode, dual Schottky, 200 mA, 30 V Terminal block, 2-pin, 6-A, 3.5mm Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing	SOT23 0.27 × 0.25 in	BAT54STA ED555/2DS	Zetex OST
2 J1-2 3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	1 1	ED555/2DS PEC02SAAN PEC03SAAN 1.50 kΩ	Terminal block, 2-pin, 6-A, 3.5mm  Header, male 2-pin, 100 mil spacing  Header, male 3-pin, 100 mil spacing	0.27 × 0.25 in	ED555/2DS	OST
3 J3-5 1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10		PEC02SAAN PEC03SAAN 1.50 kΩ	Header, male 2-pin, 100 mil spacing Header, male 3-pin, 100 mil spacing			
1 JP1 1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10		PEC03SAAN 1.50 kΩ	Header, male 3-pin, 100 mil spacing	0.100 in × 2	DECO2CA AN	Outline.
1 R1 1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10		1.50 kΩ			PEC02SAAN	Sullins
1 R3 1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10				0.100 in × 3	PEC03SAAN	Sullins
1 R4 1 R5 1 R6 1 R7 1 R8 1 R9 1 R10	(	0 Ω	Resistor, thick film, 1/4 W, ± 5%	1206	Std	Std
1 R5 1 R6 1 R7 1 R8 1 R9 1 R10			Resistor, chip, 1/16 W, 1%	0603	Std	Std
1 R6 1 R7 1 R8 1 R9 1 R10	4	49.9 Ω	Resistor, chip, 1/16 W, 1%	0603	Std	Std
1 R7 1 R8 1 R9 1 R10	(	6.8 Ω	Resistor, chip, 1/16 W, 1%	0603	STD	STD
1 R8 1 R9 1 R10	4	4.99 kΩ	Resistor, chip, 1/16 W, 1%	0603	Std	Std
1 R9 1 R10		1.00 kΩ	Resistor, chip, 1/16 W, 1%	0603	Std	Std
1 R10	:	30.1 kΩ	Resistor, chip, 1/16 W, 1%	0603	Std	Std
	4	499 Ω	Resistor, chip, 1/16 W, 1%	0603	Std	Std
0 R11		137 kΩ	Resistor, chip, 1/16 W, 1%	0603	STD	STD
	(	Open	Resistor, chip, 1/16 W, 1%	0603	Std	Std
1 R13		1.47 kΩ	Resistor, chip, 1/16 W, 1%	0603	Std	Std
1 R14		10.0 kΩ	Resistor, chip, 1/16 W, 1%	0603	Std	Std
2 R2, R12	12 (	0 Ω	Resistor, chip, 1/16 W, 1%	0603	Std	Std
1			Shunt, 100-mil, black	0.100	929950-00	3M
1 T1		12 μH	XFMR, 1.2 turns ratio	13.46 × 17.75 mm	NA5889-AL	Coilcraft
6 TP1-2,	, TP5-8	5000	Test point, red, thru hole color keyed	0.100 × 0.100 in	5000	Keystone
2 TP3-4		5001	Test point, black, thru hole color keyed	0.100 × 0.100 in	5001	Keystone
1 U1	-	TPS55340RTE	IC, 5-A high-voltage boost converter with soft-start and programmable switching frequency	QFN-16	TPS55340RTE	TI
1 U2	-	TCMT1107	IC, Photocoupler, CTR = 80% - 160%	MF4	TCMT1107	Vishay
1 U3	-	TLV431CDBZR	IC, Low-voltage adjustable shunt regulator	SOT23-3	TLV431CDBZR	TI
1			PCB, 3.125 ln x 1.25 ln x 0.062 ln		PWR148	Any
2. Thes		are ESD sensitive, observe ESD must be clean and free from flux must comply with workmanship	x and all contaminants. Use of no-clean flux is	not acceptable.		
		1.7	· · · · · · · · · · · · · · · · · · ·	substituted with equi	valent MFG's components.	

# 6.3 Reference

1. TPS55340, Integrated 5-A 40-V Boost/SEPIC/Flyback Converter with Adjustable Switching Frequency data sheet (SLVSBD4)

# **EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS**

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

#### REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

#### General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

# For EVMs annotated as FCC - FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

#### Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

#### FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- · Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## For EVMs annotated as IC - INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

# Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

# [Important Notice for Users of this Product in Japan]

## This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

- Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
- 3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited (address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

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本開発キットは技術基準適合証明を受けておりません。

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# EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

- 1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
- 2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
- 3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
- 4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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