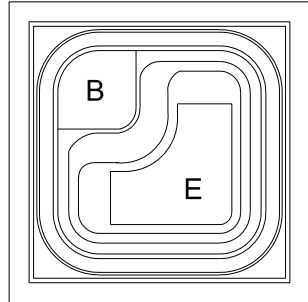


The CP388X-2N5088 is a silicon NPN transistor designed for low noise amplifier applications.



BACKSIDE COLLECTOR R0

MECHANICAL SPECIFICATIONS:

Die Size	13 x 13 MILS
Die Thickness	5.9 MILS
Base Bonding Pad Size	3.9 x 3.9 MILS
Emitter Bonding Pad Size	5.4 x 5.4 MILS
Top Side Metalization	Al-Si – 17,000Å
Back Side Metalization	Au – 9,000Å
Scribe Alley Width	1.8 MILS
Wafer Diameter	5 INCHES
Gross Die Per Wafer	102,852

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

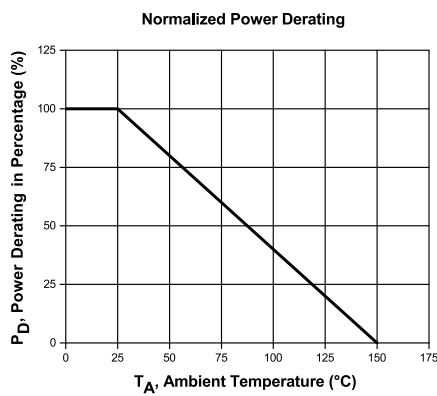
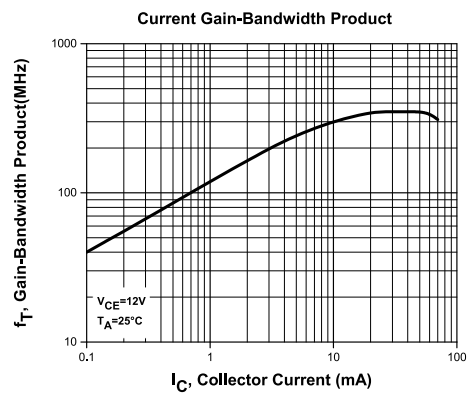
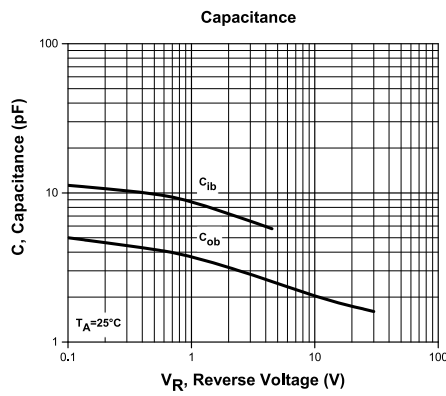
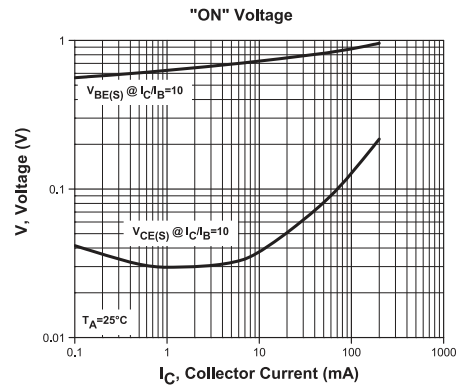
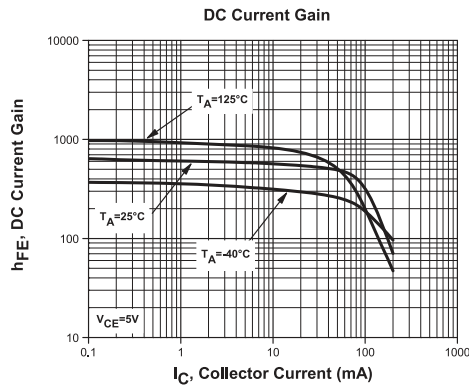
	SYMBOL		UNITS
Collector-Base Voltage	V_{CB0}	35	V
Collector-Emitter Voltage	V_{CE0}	30	V
Emitter-Base Voltage	V_{EB0}	4.5	V
Continuous Collector Current	I_C	50	mA
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$)

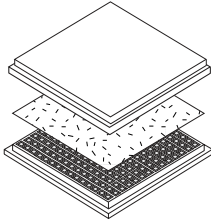
SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CBO}	$V_{CB}=20\text{V}$		50	nA
I_{EBO}	$V_{EB}=3.0\text{V}$		50	nA
I_{EBO}	$V_{EB}=4.5\text{V}$		100	nA
BV_{CBO}	$I_C=100\mu\text{A}$	35		V
BV_{CE0}	$I_C=1.0\text{mA}$	30		V
$V_{CE(SAT)}$	$I_C=10\text{mA}, I_B=1.0\text{mA}$		0.50	V
$V_{BE(ON)}$	$V_{CE}=5.0\text{V}, I_C=10\text{mA}$		0.80	V
h_{FE}	$V_{CE}=5.0\text{V}, I_C=100\mu\text{A}$	300	900	
h_{FE}	$V_{CE}=5.0\text{V}, I_C=1.0\text{mA}$	350		
h_{FE}	$V_{CE}=5.0\text{V}, I_C=10\text{mA}$	300		
h_{fe}	$V_{CE}=5.0\text{V}, I_C=1.0\text{mA}, f=1.0\text{kHz}$	350	1400	
f_T	$V_{CE}=5.0\text{V}, I_C=500\mu\text{A}, f=20\text{MHz}$	50		MHz
C_{ob}	$V_{CB}=5.0\text{V}, I_E=0, f=100\text{kHz}$		4.0	pF
C_{ib}	$V_{EB}=0.5\text{V}, I_C=0, f=100\text{kHz}$		15	pF
NF	$V_{CE}=5.0\text{V}, I_C=100\mu\text{A}, R_S=10\text{k}\Omega,$ $f=10\text{Hz to } 15.7\text{kHz}$		3.0	dB

CP388X-2N5088

Typical Electrical Characteristics



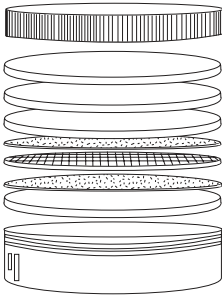
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

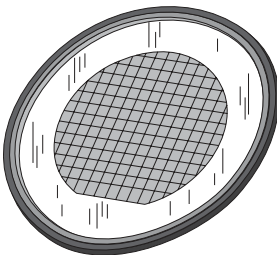
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

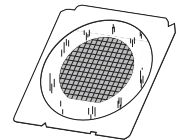
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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