

# KIT34FS6407EVB and KIT34FS6408EVB Evaluation Board

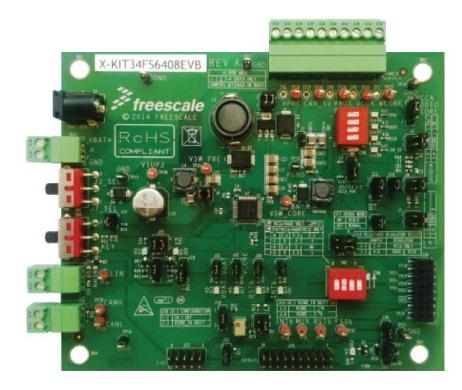


Figure 1. KIT34FS6407EVB and KIT34FS6408EVB Board





# Contents

1	Important Notice	3
2	Getting Started	4
3	Terms	5
4	Getting to Know the Hardware	6
5	Accessory Interface Board	.21
6	Installing the Software and Setting up the Hardware	.23
7	Initialization and Configuration Mode	.30
	Schematic	
9	Board Layout	.32
10	References	.37
11	Revision History	.38



# Important Notice

Freescale provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation kit may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact Freescale sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typical", must be validated for each customer application by customer's technical experts.

Freescale does not convey any license under its patent rights nor the rights of others. Freescale products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use Freescale products for any such unintended or unauthorized application, the Buyer shall indemnify and hold Freescale and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale was negligent regarding the design or manufacture of the part. Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2015



# 2 Getting Started

## 2.1 Kit Contents/Packing List

The KIT34FS6407EVB and KIT34FS6408EVB contents include:

- · Assembled and tested evaluation board/module in anti-static bag
- Warranty card

## 2.2 Jump Start

Freescale's analog product development boards help to easily evaluate Freescale products. These tools support analog mixed signal and power solutions including monolithic ICs using proven high-volume SMARTMOS mixed signal technology, and system-in-package devices utilizing power, SMARTMOS and MCU dies. Freescale products enable longer battery life, smaller form factor, component count reduction, ease of design, lower system cost and improved performance in powering state of the art systems.

· Click on the appropriate link for your board

KIT34FS6407EVB: www.freescale.com/KIT34FS6407EVB

KIT34FS6408EVB: www.freescale.com/KIT34FS6408EVB

- Review your Tool Summary Page
- Look for



· Download documents, software, and other information

Once the files are downloaded, review the user guide in the bundle. Jump start bundles are available on each tool summary page with the most relevant and current information. The information includes everything needed for design.

## 2.3 Required Equipment and Software

To use this kit, you need

- 2.7 V to 40 V power supply, 3.0 A capability
- Freescale's KITUSBSPIDGLVME interface dongle
- SPIGen Graphical User Interface or MC3390X\_GUI

When not connected to an evaluation board, the KITUSBSPIDGLVME can be used in standalone mode to program its onboard MC68HC908JW32 microcontroller. In this case, the interface dongle and USB cable are required. For more information, see the "SPIGen 7 User Guide".

### 2.4 System Requirements

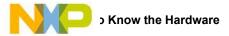
The kit requires the following:

• USB-enabled PC with Windows® XP or higher



# 3 Terms

Part Number or Parameter	Definition
CAN_5V	5.0 V CAN voltage
EVB	Evaluation Board
FCCU	Fault Collection and Control Unit
FS0B	Fail-safe Output Number 0
INTB	Interrupt
Ю	Input/Output
LDO	Low-dropout Regulator
RSTB	Reset
SMPS	Switching Mode Power Supply
SPIGen	Software utility (installed on a PC) provides communication functions between the PC and a Freescale evaluation board
V <sub>AUX</sub>	Auxiliary power supply
V <sub>CCA</sub>	Power supply for ADC
V <sub>PRE</sub>	Pre-regulator voltage
WD	Watchdog



# 4 Getting to Know the Hardware

## 4.1 Board Overview

KIT34FS6407EVB and KIT34FS6408EVB evaluation boards demonstrate the functionality of the SMARTMOS MC34FS6407 and MC34FS6408 power system basis chips, respectively. These ICs are equipped with an intelligent power management system including safety features targeting the latest ISO26262 automotive functional safety standard. The EVB is a standalone board that can be used either with a compatible microcontroller or with a PC. The latter case requires a KITUSBSPIDGLEVME accessory interface board. See Section 2.3 "Required Equipment and Software".

## 4.2 Board Features

This EVB comes mounted with either an MC34FS6407 or an MC34FS6408 IC. The main features of the board are:

- V<sub>BAT</sub> power supply either through power jack (2.0 mm) or phoenix connector
- V<sub>CORE</sub> configuration:1.2 V or 3.3 V
- V<sub>CCA</sub> configuration: 5.0 V/3.3 V
- · Internal transistor or external PNP
- V<sub>AUX</sub> configuration: 3.3 V or 5.0 V
- Enabled or disabled at startup
- · Ignition key switch
- CAN bus
- IO connector (IO\_0 to IO\_5)
- Debug connector (SPI bus, CAN digital, RSTB, FS0B, INTB, Debug, MUX\_OUT)
- · Signalling LED to give state of signals or regulators

### 4.3 Device Features

The MC34FS6407 and the MC34FS6408 are multi-output ICs, with power supply and HSCAN transceiver. The MC34FS6407 is designed to support up 800 mA on V<sub>CORE</sub>, while MC34FS6408 supports up to 1.5 A on V<sub>CORE</sub>. All other features are the same.

Device	Description	Features
MC34FS6407/ MC34FS6408	Power system basis chip with high-speed CAN and LIN transceivers	<ul> <li>Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost or standard buck</li> <li>Switching mode power supply (SMPS) dedicated to MCU core supply: 1.2 V or 3.3 V, delivering up to 1.5 A for the MC34FS6408 and up to 800 mA for the MC34FS6407</li> <li>Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (VCCA): 5.0 V or 3.3 V</li> <li>Linear voltage regulator dedicated to auxiliary functions or to a sensor supply (VCCA tracker or independent 5.0 V/3.3 V)</li> <li>Multiple wake-up sources in Low-power mode: CAN and/or IOs</li> <li>Battery voltage sensing and multiplexer output terminal (various signal monitoring)</li> <li>Enhanced safety block associated with fail-safe outputs</li> <li>Six configurable I/Os</li> <li>ISO11898 high-speed CAN interface compatibility for baud rates of 40 kB/s to 1.0 MB/s</li> <li>High EMC immunity and ESD robustness</li> </ul>



### 4.4 Board Description

The EVB comes with either a Freescale MC34FS6407 or MC34FS6408 IC mounted on it. Below is a view of the board indicating the major components.

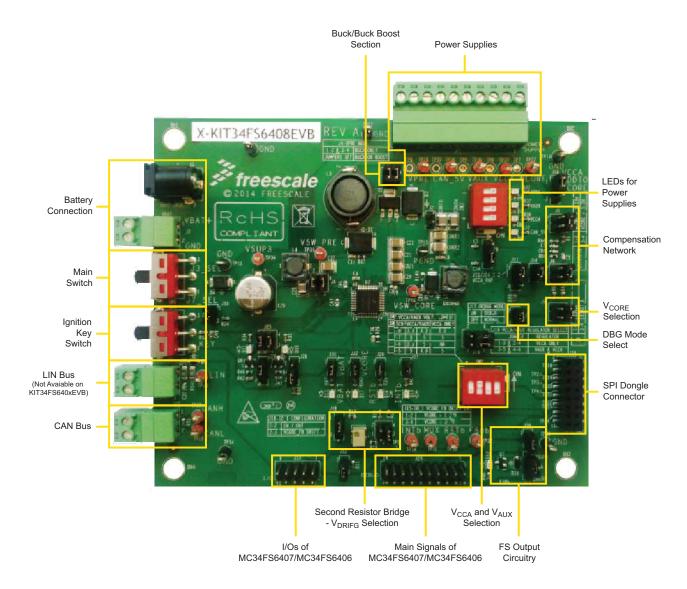


Figure 2. Board Description —MC34FS6407and MC34FS6408

#### Table 2. Board Description

Name	Description
Buck/Buck-Boost Section	VPRE DC/DC selection mode, either Boost or Buck
Battery Connection	Battery voltage input, either on Jack (black connector) or Phoenix (green) connector
Main Switch	Battery voltage ON/OFF

#### Table 2. Board Description (continued)

Name	Description
Ignition Key Switch	Simulate ignition key. Connected to IO_0
LIN Bus	LIN bus as a master (Not available on KIT34FS640xEVB)
CAN Bus	CANH and CANL differential pair
I/Os of MC34FS6407_8	All IOs, VDDIO and GND available
Second Resistor Bridge - V <sub>DRIFT</sub> Selection	Bridge resistor for V <sub>CORE</sub> redundant check
Main Signals of MC34FS6407_8	SPI, VDDIO, fail-safe pin, CAN, MUXOUT, INTB and RSTB available
V <sub>CCA</sub> and V <sub>AUX</sub> Selection	V <sub>CCA</sub> and V <sub>AUX</sub> voltage selection
FS Output Circuitry	FS0B configuration
SPI Dongle Connector	Connector with SPI bus. Compliant to SPIGen Freescale board
DBG Mode Select	Controls Debug or Normal mode entering at boot up
V <sub>CORE</sub> Selection	V <sub>CORE</sub> voltage selection
Compensation Network	Compensation network selection
LEDs for Power Supplies	Switches for ON/OFF on LEDs
Power Supplies	• MC34FS6407 or MC34FS6408 output power supply (V <sub>PRE</sub> , V <sub>CORE</sub> , V <sub>AUX</sub> , V <sub>CCA</sub> )

## 4.5 Evaluation Board Configuration

Figure 3 shows a configuration example for the EVB, which enables:

- V<sub>CORE</sub> 3.3 V
- Compensation network for MPC5643L
- $V_{CCA}$  and  $V_{AUX}$  = 5.0 V
- V<sub>CCA</sub> with external PNP
- Debug mode
- VPRE in Buck mode
- +  $V_{DDIO}$  tied to  $V_{CCA}$
- Various signalling LEDs enabled
- IO1 configured as IN/OUT



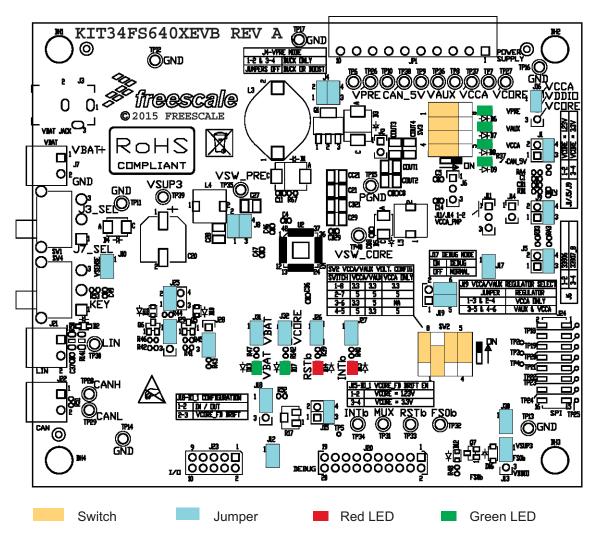


Figure 3. Default Board Configuration

## 4.6 LED Definitions

The following table lists the LEDs used as visual output devices on the EVB:

#### Table 3. LEDs

Schematic Label	Name	Description
D6	V <sub>PRE</sub>	Indicator of pre-regulator voltage
D7	V <sub>AUX</sub>	Indicator of auxiliary power supply
D8	V <sub>CCA</sub>	Indicator of ADC power supply
D9	CAN_5V	Indicator of 5.0 V CAN voltage
D10	IO_5	Indicator of IO_5 state
D11	IO_4	Indicator of IO_4 state
D12	FS0B	Indicator for fail-safe output number 0
D13	V <sub>BAT_P</sub>	Indicator of battery voltage after protection diode
D14	RSTB	Indicator of a reset
D15	INTB	Indicator of an interrupt
D17	V <sub>CORE</sub>	Indicator of V <sub>CORE</sub> power supply

# 4.7 Test Point Definitions

The following test-point jumpers provide access to signals on the MC34FS6407or MC34FS6408:

#### Table 4. Test Points

Schematic Label	Signal Name	Description
TP2	J24.3	-
TP3	J24.5	-
TP4	J24.7	-
TP5	J20.16	-
TP6	PGND	Power ground
TP7	PGND	Power ground
TP8	GND	Ground
TP9	GND	Ground
TP10	GND	Ground
TP11	GND	Ground
TP12	GND	Ground
TP13 GND		Ground
TP14	GND	Ground
TP15 GND		Ground



#### Table 4. Test Points (continued)

Schematic Label Signal Name		Description
TP16	GND	Ground
TP17	GND	Ground
TP18	J24.2	-
TP19	J24.4	-
TP20	J24.6	-
TP21	J24.8	-
TP22	J24.10	-
TP23	J24.12	-
TP24	J24.14	-
TP25	J24.16	-
TP26	V <sub>PRE</sub>	Pre-regulator voltage
TP27	V <sub>CORE</sub>	Core voltage for the MCU
TP28 CANH		-
TP29 CANL		-
TP30 LIN		LIN bus (Not available on KIT34FS640xEVB)
TP31 MUX_OUT		Output from the analog multiplexer
TP32	FS0B	Fail-safe output
TP33	RSTB	Reset signal
TP34	INTB	Interrupt output
TP35 V <sub>SW</sub>		V <sub>PRE</sub> Switching voltage
TP36	V <sub>AUX</sub>	Auxiliary power supply
TP37	V <sub>CCA</sub>	ADC power supply
TP38	CAN_5V	CAN power supply
TP39	V <sub>SUP3</sub>	Supply voltage
TP40 VSW_Core		V <sub>CORE</sub> supply voltage

# 4.8 Connector and Jumper Definitions

#### Table 5. Main Power Supply Connector

JP1 Pin Number	Name of Power Rail	Description
1	V <sub>CORE</sub>	Core voltage for the MCU
2	PGND	Power ground
3	V <sub>CCA</sub>	ADC power supply
4	GND	Ground
5	V <sub>AUX</sub>	Auxiliary power supply
6	GND	Ground
7	CAN_5V	CAN power supply
8	GND	Ground
9	V <sub>PRE</sub>	Pre-regulator voltage
10	PGND	Power ground

#### Table 6. Jumpers J1 through J31 (Including Connectors)

Schematic Label	Pin Number	Pin Name	Jumper/Pin Function	
J1	Compensation network for FB_core – part 1			
	1-2		V <sub>CORE</sub> = 1.23 V	
	3-4		V <sub>CORE</sub> = 3.3 V	
J2			pacitance for V <sub>CORE</sub> is 40 μF, 20 μF otherwise	
	No jumper		C <sub>OUT</sub> = 20 μF	
	1-2		C <sub>OUT</sub> = 40 μF	
J3	J3 Power supply DC 12 V			
J4	Buck-boost/standard buck mode configuration			
	1-2		Rusk boost configuration	
	3-4		Buck-boost configuration	
	No jumper		Buck only configuration	
J5	V <sub>CORE</sub> selection			
	1-2		V <sub>CORE</sub> = 1.23 V	
	3-4		V <sub>CORE</sub> = 3.3 V	



Image: Second Second Procession Pr	Schematic Label	Pin Number	Pin Name	Jumper/Pin Function		
$ \begin{array}{ c c c c } \hline V_{CORE} \\ \hline V_{CORE} \\ \hline $	J6	Configuration for Boots_core pin				
J7         Power supply (max. voltage = 40 V) This connector should be used to supply EVB from protected voltage source           1         VBAT         Positive supply           2         GND         Ground           38         Power supply for EVB Allows disconnecting of all three supply pins for current measurements Normally (no measurement), jumpers should be connected         Normally (no MC34FS6407 (or MC34FS6407 (or MC34FS6407 (or MC34FS6407 (or MC34FS6408)))           39         Compensation network for FB_core – part 2         1.2         VCORE = 1.23 V           3.4         UCORE = 3.3 V         VCORE = 3.3 V         VCORE = 3.3 V           J10         V <sub>SNS</sub> _EN – connects battery voltage before filter to V <sub>SENSE</sub> 1.2         Emitter of Q2 connected to VCCA_E           311         External transistor for V <sub>CCA</sub> External transistor Q2 is not used         1.2           312         IO_0_PD – pulls down IO_0         1.2         FS0B pull-up is supplied from V <sub>SUP3</sub> 313         FS0B pull-up connection         1.2         FS0B pull-up is supplied from V <sub>SUP3</sub> 314         Connects bate of the transistor Q2 to the VCCA_B pin         1.4		1-2		Boots_core pin connected to GND – used for devices with linear voltage regulator on $V_{\mbox{CORE}}$		
This connector should be used to supply EVB from protected voltage source         1       VBAT       Positive supply         2       GND       Ground         J8       Power supply for EVB Allows disconnecting of all three supply pins for current measurements Normally (no measurement), jumpers should be connected         1-2       Enables power supply (V <sub>BAT_P</sub> ) for VSUP3 pin of MC34FS6407(or MC34FS6407(or MC34FS6408)         J9       Compensation network for FB_core – part 2         1-2       V <sub>CORE</sub> = 1.23 V         3-4       V <sub>CORE</sub> = 3.3 V         J10       V <sub>SNS_</sub> EN – connects battery voltage before filter to V <sub>SENSE</sub> J11       External transistor for V <sub>CCA</sub> 1-2       Emitter of Q2 connected to VCCA_E         2-3       External transistor Q2 is not used         J12       IO_0_PD – pulls down IO_0         J13       FS0B pull-up connection         1-2       FS0B pull-up is supplied from V <sub>SUP3</sub> J14       Connects base of the transistor Q2 to the VCCA_B pin		2-3		Boots_core pin connected to SW_core – used for devices with switching mode power supply on $V_{\mbox{CORE}}$		
2       GND       Ground         J8       Power supply for EVB Allows disconnecting of all three supply pins for current measurements Normally (no measurement), jumpers should be connected         1-2       Enables power supply (V <sub>BAT_P</sub> ) for VSUP3 pin of MC34FS6407(or MC34FS6407 (or MC34FS6408)         J9       Compensation network for FB_core – part 2         1-2       V <sub>CORE</sub> = 1.23 V         3-4       V <sub>CORE</sub> = 3.3 V         J10       V <sub>SNS_EN</sub> – connects battery voltage before filter to V <sub>SENSE</sub> J11       External transistor for V <sub>CCA</sub> 1-2       Emitter of Q2 connected to VCCA_E         2-3       External transistor Q2 is not used         J12       IO_0_PD – pulls down IO_0         J13       FS0B pull-up connection         1-2       FS0B pull-up is supplied from V <sub>SUP3</sub> J11       Connects base of the transistor Q2 to the VCCA_B pin	J7	Power supply (n This connector s	nax. voltage = 40 should be used to	V) o supply EVB from protected voltage source		
J8       Power supply for EVB Allows disconnecting of all three supply pins for current measurements Normally (no measurement), jumpers should be connected         1-2       Enables power supply (V <sub>BAT</sub> _P) for VSUP3 pin of MC34FS6407(or MC34FS6407(or MC34FS6408)         J9       Compensation network for FB_core – part 2         1-2       V <sub>CORE</sub> = 1.23 V         3-4       V <sub>CORE</sub> = 3.3 V         J10       V <sub>SNS</sub> _EN – connects battery voltage before filter to V <sub>SENSE</sub> J11       External transistor for V <sub>CCA</sub> 1-2       Emitter of Q2 connected to VCCA_E         2-3       External transistor Q2 is not used         J12       IO_0_PD – pulls down IO_0         J13       FS0B pull-up connection         1-2       FS0B pull-up is supplied from V <sub>SUP3</sub> 2-3       FS0B pull-up is supplied from V <sub>DDIO</sub> J14       Connects base of the transistor Q2 to the VCCA_B pin		1	VBAT	Positive supply		
Allows disconnecting of all three supply pins for current measurements Normally (no measurement), jumpers should be connected1-2Enables power supply ( $V_{BAT_P}$ ) for VSUP3 pin of MC34FS6407(or MC34FS6407 (or MC34FS6408)3-4Enables power supply ( $V_{SUP}$ ) for VSUP1 and VSUP2 pins of MC34FS6407(or MC34FS6408)J9Compensation network for FB_core – part 21-2 $V_{CORE} = 1.23 V$ 3-4 $V_{CORE} = 3.3 V$ J10 $V_{SNS_EN}$ – connects battery voltage before filter to $V_{SENSE}$ J11External transistor for $V_{CCA}$ 1-2Emitter of Q2 connected to VCCA_E2-3External transistor Q2 is not usedJ12 $IO_0_PD$ – pulls down $IO_0$ J13FS0B pull-up connection1-2FS0B pull-up is supplied from $V_{SUP3}$ 2-3FS0B pull-up is supplied from $V_{DDIO}$ J14Connects base of the transistor Q2 to the VCCA_B pin		2	GND	Ground		
$\frac{1}{3.4}$ $\frac{1}$	J8	Allows disconne	cting of all three	supply pins for current measurements pers should be connected		
$MC34FS6408)$ $J9$ $Compensation network for FB_core - part 2$ $1-2$ $V_{CORE} = 1.23 V$ $3-4$ $V_{CORE} = 3.3 V$ $J10$ $V_{SNS}EN - connects battery voltage before filter to V_{SENSE}$ $J11$ $External transistor for V_{CCA}$ $1-2$ $Emitter of Q2 connected to VCCA_E$ $2-3$ $External transistor Q2 is not used$ $J12$ $IO_0-PD - pulls down IO_0$ $J13$ $FS0B pull-up connection$ $1-2$ $FS0B pull-up is supplied from V_{SUP3}$ $2-3$ $FS0B pull-up is supplied from V_{DDIO}$ $J14$ $Connects base of the transistor Q2 to the VCCA_B pin$		1-2		Enables power supply (V <sub>BAT_P</sub> ) for VSUP3 pin of MC34FS6407(or MC34FS6408)		
1-2 $V_{CORE} = 1.23 V$ 3-4 $V_{CORE} = 3.3 V$ J10 $V_{SNS}_{EN} = Connects battery voltage before filter to V_{SENSE}J11External transistor for V_{CCA}1-2Emitter of Q2 connected to VCCA_E2-3External transistor Q2 is not usedJ12IO_0_PD - pulls down IO_0J13FSOB pull-up connection1-2FSOB pull-up is supplied from V_{SUP3}2-3FSOB pull-up is supplied from V_{DDIO}J14Connects base of the transistor Q2 to the VCCA_B pin$		3-4				
Intermediate 3-4Note3-4 $V_{CORE} = 3.3 V$ J10 $V_{SNS}EN$ - connects battery voltage before filter to $V_{SENSE}$ J11External transistor for $V_{CCA}$ 1-2Emitter of Q2 connected to VCCA_E2-3External transistor Q2 is not usedJ12 $D_0PD - pulls down IO_0$ J13FSOB pull-up connection1-2FSOB pull-up is supplied from $V_{SUP3}$ 2-3FSOB pull-up is supplied from $V_{DDIO}$ J14Connects base of the transistor Q2 to the VCCA_B pin	J9	Compensation network for FB_core – part 2				
J10       V <sub>SNS</sub> _EN – connects battery voltage before filter to V <sub>SENSE</sub> J11       External transistor for V <sub>CCA</sub> 1-2       Emitter of Q2 connected to VCCA_E         2-3       External transistor Q2 is not used         J12       IO_0_PD – pulls down IO_0         J13       FSOB pull-up connection         1-2       FSOB pull-up is supplied from V <sub>SUP3</sub> 2-3       FSOB pull-up is supplied from V <sub>DDIO</sub> J14       Connects base of the transistor Q2 to the VCCA_B pin		1-2		V <sub>CORE</sub> = 1.23 V		
J11       External transistor for V <sub>CCA</sub> 1-2       Emitter of Q2 connected to VCCA_E         2-3       External transistor Q2 is not used         J12       IO_0_PD – pulls down IO_0         J13       FSOB pull-up connection         1-2       FSOB pull-up is supplied from V <sub>SUP3</sub> 2-3       FSOB pull-up is supplied from V <sub>DDIO</sub> J14       Connects base of the transistor Q2 to the VCCA_B pin		3-4		V <sub>CORE</sub> = 3.3 V		
1-2       Emitter of Q2 connected to VCCA_E         2-3       External transistor Q2 is not used         J12       IO_0_PD – pulls down IO_0         J13       FSOB pull-up connection         1-2       FSOB pull-up is supplied from V <sub>SUP3</sub> 2-3       FSOB pull-up is supplied from V <sub>DDIO</sub> J14       Connects base of the transistor Q2 to the VCCA_B pin	J10	V <sub>SNS</sub> EN – con	nects battery volt	age before filter to V <sub>SENSE</sub>		
Image: Problem state     Problem state       2-3     External transistor Q2 is not used       J12     IO_0_PD - pulls down IO_0       J13     FS0B pull-up connection       1-2     FS0B pull-up is supplied from V <sub>SUP3</sub> 2-3     FS0B pull-up is supplied from V <sub>DDIO</sub> J14     Connects base of the transistor Q2 to the VCCA_B pin	J11	External transistor for V <sub>CCA</sub>				
J12     IO_0_PD – pulls down IO_0       J13     FS0B pull-up connection       1-2     FS0B pull-up is supplied from V <sub>SUP3</sub> 2-3     FS0B pull-up is supplied from V <sub>DDIO</sub> J14     Connects base of the transistor Q2 to the VCCA_B pin		1-2		Emitter of Q2 connected to VCCA_E		
J13       FS0B pull-up connection         1-2       FS0B pull-up is supplied from V <sub>SUP3</sub> 2-3       FS0B pull-up is supplied from V <sub>DDIO</sub> J14       Connects base of the transistor Q2 to the VCCA_B pin		2-3		External transistor Q2 is not used		
1-2     FS0B pull-up is supplied from V <sub>SUP3</sub> 2-3     FS0B pull-up is supplied from V <sub>DDIO</sub> J14     Connects base of the transistor Q2 to the VCCA_B pin	J12	IO_0_PD - pulls	s down IO_0	·		
2-3     FS0B pull-up is supplied from V <sub>DDIO</sub> J14     Connects base of the transistor Q2 to the VCCA_B pin	J13	FS0B pull-up connection				
J14 Connects base of the transistor Q2 to the VCCA_B pin		1-2		FS0B pull-up is supplied from V <sub>SUP3</sub>		
		2-3		FS0B pull-up is supplied from V <sub>DDIO</sub>		
	J14 Connects base of the transistor Q2 to the VCCA_B pin		Q2 to the VCCA_B pin			
<ul> <li>J15 External resistor bridge monitoring (for future use)</li> <li>Used in conjunction with J18</li> <li>Resistor bridge has to be in same configuration as J5</li> <li>Voltage on this voltage divider has to be adjusted to same level as for first bridge using potentiometer R17</li> </ul>	J15	Resistor bridge has to be in same configuration as J5				
1-2 V <sub>CORE</sub> = 1.23 V		1-2		V <sub>CORE</sub> = 1.23 V		
3-4 V <sub>CORE</sub> = 3.3 V		3-4		V <sub>CORE</sub> = 3.3 V		



Schematic Label	Pin Number	Pin Name	Jumper/Pin Function					
J16	V <sub>DDIO</sub> tracking							
	1-2		V <sub>DDIO</sub> tracks V <sub>CCA</sub>					
	2-3		V <sub>DDIO</sub> tracks V <sub>CORE</sub>					
J17	DBG_EN - enab	les debug mode						
	No jumper		Normal mode					
	1-2		Normal mode Debug mode					
J18	DRIFT_MONIT -	<ul> <li>External resisto</li> </ul>	or bridge monitoring					
	1-2		Second resistor bridge on IO_1 is disabled					
	2-3		Reserved for future use					
J19	V <sub>CCA</sub> /V <sub>AUX</sub> regu	lator selection						
	1-3 and 2-4		V <sub>AUX</sub> is disabled					
	3-5 and 4-6		V <sub>AUX</sub> is enabled					



Schematic Label	Pin Number	Pin Name	Jumper/Pin Function
J20	Additional Inputs	s/Output	•
	1	FS0B	Fail-safe output
	2	VDDIO	V <sub>DDIO</sub> voltage
	3	MISO	SPI – Master Input Slave Output
	4	RSTB	Reset pin – connect to the reset line of the MCU
	5	MOSI	SPI – Master Output Slave Input
	6	GND	Ground
	7	SCLK	SPI – clock
	8	GND	Ground
	9	NCS	SPI – Chip Select
	10	GND	Ground
	11	MUX_OUT	Output from the multiplexer – connect to the MCU's ADC
	12	INTB	Interrupt pin – connect to the MCU IO with an interrupt capability
	13	RXD_L	LIN receive pin – connect to the MCU — Not Available on KIT34FS640xEVB
	14	TXD_L	LIN transmit pin – connect to the MCU — Not Available on KIT34FS640xEVB
	15	GND	Ground
	16	TP5	-
	17	RXD	CAN receive pin – connect to the MCU
	18	TXD	CAN transmit pin – connect to the MCU
	19	DBG	Debug pin
	20	GND	Ground
J21	LIN connector		
	1	LIN	LIN after transceiver (NOT the MCU side) — Not Available on KIT34FS640xEVB
	2	GND	Ground
J22	CAN connector		
	1	CANH	CANH signal after transceiver (NOT the MCU side)
	2	CANL	CANL signal after transceiver (NOT the MCU side)



Schematic Label	Pin Number	Pin Name	Jumper/Pin Function
J23	General Inputs/0	Outputs	·
	pin1	IO_1	-
	pin2	IO_0	-
	pin3	IO_3	-
	pin4	IO_2	-
	pin5	IO_5	-
	pin6	IO_4	-
	pin7	VDDIO	-
	pin8	NC	-
	pin9	VBAT	-
	pin10	GND	-
J24	SPI/USB dongle SPI/USB dongle	or MCU connects should be direct	tion tly connected to this port
	pin1	GND	Ground
	pin2	TP18	-
	pin3	TP2	-
	pin4	TP19	-
	pin5	TP3	-
	pin6	TP20	-
	pin7	TP4	-
	pin8	TP21	-
	pin9	SCLK	SPI – clock
	pin10	TP22	Not connected
	pin11	MOSI	SPI – Master Output Slave Input
	pin12	TP23	-
	pin13	MISO	SPI – Master Input Slave Output
	pin14	TP24	-
	pin15	NCS	SPI – Chip Select
	pin16	TP25	-
J25	Power supply fo	r LEDs on IO_4	and IO_5 (D11, D10)
	1-2		Enables power supply for IO_4 (D11)
	3-4		Enables power supply for IO_5 (D10)
J26	RSTB_LED_EN	– enables LED	D14 for RSTB output



Schematic Label	Pin Number	Pin Name	n _5 connected to LED D10 via transistor Q5 _5 pulled down n					
J27	INTB_LED_EN -	– enables LED D	15 for INTB output					
J28	105_0UT - 10_9	5 output configura	ation					
	1-2		IO_5 connected to LED D10 via transistor Q5					
	2-3		IO_5 pulled down					
J29	104_0UT - 10_4	4 output configura	ation					
	1-2		IO_4 pulled down					
	2-3		IO_4 connected to LED D11 via transistor Q6					
J30	Enable LED D12	2 for fail-safe.						
J31	Enables LED D1	3 as indicator of	power supply					
J32	Enables LED D1	7 as indicator for	r V <sub>CORE</sub> power supply					



#### 4.8.1 Compensation Network

A voltage regulator needs feedback from the V<sub>CORE</sub> voltage to be able to adjust (control) output voltage. For this reason, two bridges are implemented in the external MC34FS6407 or MC34FS6408 circuitry. Static feedback (steady-state) voltage is defined by a simple resistor bridge (given by RA3/RB3 and RA4). Dynamic behavior of the regulator is controlled by another bridge that is an RC divider (defined by RBx, CBx, R1, C1, R2, C2). Figure 4 shows the compensation network. Steady-state voltage can be either 1.2 V or 3.3 V. To tune the dynamic performance, the board is equipped with two different bridges (possible combinations of the jumpers J1 and J9 are shown in Table 7). The combinations shown in Table 7 are chosen to provide optimal performance for the given output voltage. The real dynamic performance can differ for different applications and can be tuned by changing the compensation network and by adding output capacitors (J2).

Table 7. Compensation	Network and V <sub>CORE</sub> Settings
-----------------------	--

V <sub>CORE</sub>	Jumper Settings							
(V)	Static Behavior	Dynamic Behavior						
	J5	J1	J9					
1.23	3-4	3-4	3-4					
3.3	1-2	1-2	1-2					

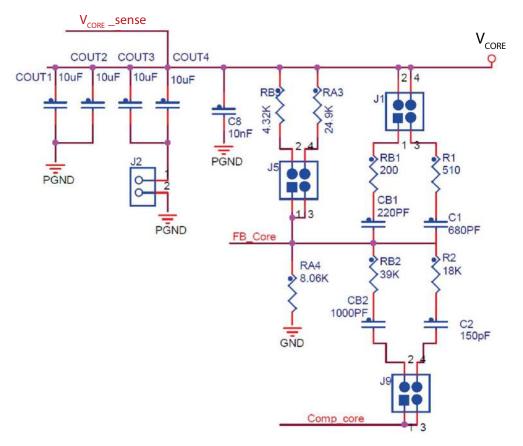


Figure 4. Compensation Network and V<sub>CORE</sub> Setup Schematic



## 4.8.2 Second Resistor Bridge - V<sub>DRIFT</sub> Monitoring

To increase the safety level of an application, a second resistor bridge has been added. This bridge generates the same voltage as the bridge connected to FB\_core pin. If the difference between voltages is greater than  $V_{DRIFT}$ , the FS state machine is impacted.

#### Table 8. V<sub>DRIFT</sub> Monitoring Settings

V <sub>CORE</sub>	Hardware Settings					
(V)	J15	J18				
1.23	1+2	3+4				
3.3	3+4	1+2				

Invoking this functionality involves both the board hardware and the software configuration. On the hardware side, the second resistor bridge must be configured by jumper J18, as shown in the Figure 5, and adjusted by the potentiometer R17 to set the same voltage as on the first bridge. Software sets registers INIT\_Vreg1 (bit Vcore\_FB to 1) and register INIT\_FSSM1 (bit IO\_1\_FS to 1).

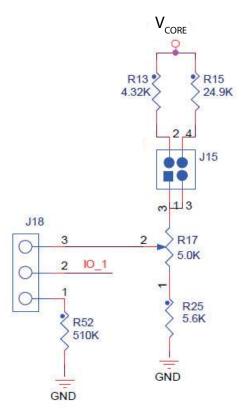


Figure 5. Second Resistor Bridge

# 4.9 Switch Definitions

#### Table 9. Switches

Switch Number	Position	Function	Description
SW1	Power supply select		
	1-2	Supply from J7 selected	
	2-3	Power jack on J3 selected	
SW2	V <sub>CCA</sub> /V <sub>AUX</sub> switch Only one choice is possible	at the same time	
	1	3.3 V / 3.3 V	
	2	5.0 V / 5.0 V	
	3	3.3 V / 5.0 V	This setting is not allowed if $V_{AUX}$ is not used - option $V_{CCA}$ only (selected by J19)
	1-2       2-3       SW2     V <sub>CCA</sub> /V <sub>AUX</sub> switch Only one choice is possible       1       2       3       4       SW3       LEDs - indicators for power       1       2       3       4       SW4       Ignition switch       1-2	5.0 V / 3.3 V	
SW3	LEDs - indicators for power	supplies	
	1	V <sub>PRE</sub>	Enables LED indicator for pre-regulator
	2	V <sub>AUX</sub>	Enables LED indicator for auxiliary power supply
	3	V <sub>CCA</sub>	Enables LED indicator for V <sub>CCA</sub> regulator
	4	CAN_5 V	Enables LED indicator for CAN regulator
SW4	Ignition switch		
	1-2	IO_0 connected to V <sub>BAT</sub> (ignition key active)	
	2-3	No voltage on the IO_0	



# 5 Accessory Interface Board

The KIT34FS6407EVB and KIT34FS6408EVB are generally used with the KITUSBSPIDGLEVME interface dongle (see Figure 6), which provides a bidirectional SPI/USB conversion. This small board makes use of the USB, SPI, and parallel ports built into Freescale's MC68HC908JW32 microcontroller. The main function provided by this dongle is to allow Freescale evaluation kits that have a parallel port to communicate via a USB port to a PC. For more information regarding KITUSBSPIDGLEVME interface dongle, go to http://www.freescale.com/webapp/sps/site/prod\_summary.jsp?code=KITUSBSPIDGLEVME.



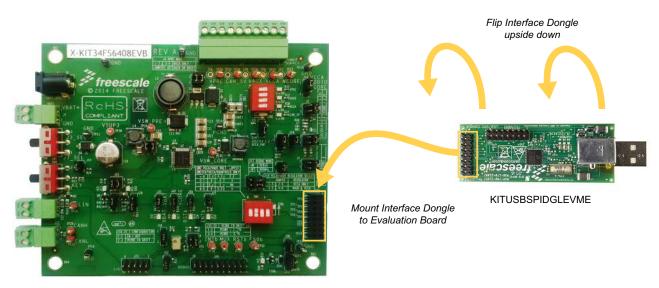
Figure 6. KITUSBSPIDGLEVME Interface Dongle

For information on setting up the dongle with the EVB, see Section 5.1 "Connecting the KITUSBSPIDGLEVME Interface Dongle".



# 5.1 Connecting the KITUSBSPIDGLEVME Interface Dongle

A typical connection of KITUSBSPIDGLEVME Interface Dongle (see Section 5 "Accessory Interface Board") to the KIT34FS6407EVB or KIT34FS6408EVB evaluation board is done through connector J24 (see Figure 7). In this configuration, it is recommended that you use the EVB in a debug mode (J17 configured as Debug). In this mode there is no timeout used for the INIT phase, so the initialization commands can be sent anytime. WD refresh is also not mandatory in the debug mode. This means that no action is taken if WD refresh fails (WD window expires, WD refreshed during closed window, wrong WD answer).



KIT34FS6407EVB/KIT34FS6408EVB

#### Figure 7. Connecting KITUSBSPIDGLEVME to the Evaluation Board



# 6 Installing the Software and Setting up the Hardware

#### 6.1 Installing the GUI Software

Two different Graphical User Interfaces (GUI's) provide the software interface that allows you to communicate with the KIT34FS6407EVB or the KIT34FS6408EVB.

- SPIGen is Freescale's generic GUI for use with the KITUSBSPIDGLEVME Interface Dongle.
- The MC3390X\_GUI is a special purpose graphical user interface designed specifically for MC3390x and MC34FS640x evaluation boards.

Both GUI's are similar in function and either may be used with the KIT34FS6407/8 EVBs.

#### 6.1.1 Installing SPIGen on your Computer

The latest version of SPIGen is designed to run on any Windows 8, Windows 7, Vista, or XP-based operating system. To install the software, do the following:

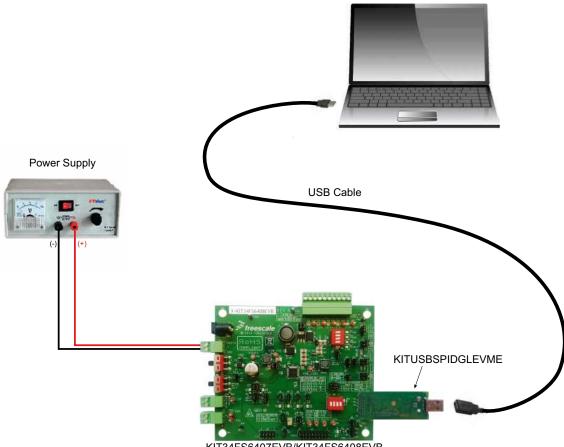
- 1. Download and install SPIGen
  - a) Go to www.freescale.com/analogtools and find your kit.
  - b) Click on the kit name to open the corresponding Tool Summary Page
  - c) On the tool summary page, look for "Jump Start Your Design." Click on "Get Started with the KIT34FS640xEVB" link.
  - d) From the list of items that appear, click on "SPI Generator (SPIGen) Software" and follow the sequence of instructions to begin the download process.
  - e) After you click the appropriate download button, a large downward arrow appears momentarily at the bottom left corner of your screen, indicating that the download has begun.
  - f) When the download completes, an SPIGEN.exe button appears at the bottom left corner of your screen. Click on the button and select "Run." A wizard guides you through the installation process.
  - g) If you instructed the SPIGen wizard to create a short-cut, an SPIGen icon appears on you desktop. If you elected not to create a short-cut, the SPIGen executable is installed by default at C:Program Files\SPIGen
  - 2. Download the configuration file MC33907\_8\_SPIGEN.spi.
    - a) Go to www.freescale.com/analogtools and find your kit.
    - b) Click on the kit name to open the corresponding Tool Summary Page
    - c) On the tool summary page, look for "Jump Start Your Design." Click on 'Get Started with the KIT34FS640xEVB."
    - d) From the list of items that appear, click on "MC33907/MC33908 SPIGen Configuration Modification File."
    - e) You will be prompted with the option to Open or Save the file. Select the option to Save.
    - f) After the download completes successfully, look for MC33907\_8\_SPIGEN.spi in your system download folder (C:\Users\xxxx\Downloads).

#### 6.1.2 Installing the MC3390X\_GUI on your Computer

- 1. Go to www.freescale.com/analogtools and find your kit.
- 2. Click on the kit name to open the corresponding Tool Summary Page
- 3. On the Tool Summary Page, look for "Jump Start Your Design." Click on "Get Started with the KIT34FS640xEVB" link.
- 4. From the list of items that appear, click on "MC33907/8 Graphical User Interface." You will be prompted to accept the licensing agreement.
- 5. When you have accepted licensing agreement, click on the download button that appears.
- 6. A zip file named "KT33907\_8\_GUI" will download to your system download folder (C:\Users\xxxx\Downloads.) Click on the zip file in your system download folder and Unzip the MC3390X\_GUI folder into a folder of your choice.
- 7. When the Unzip operation is complete, click on the Freescale setup icon that appears in the folder you extracted to. An Installation wizard guides you through the setup process.
- 8. If you elected to create a desktop icon during the setup process, a Freescale MC3390X\_GUI icon appears on your desktop. If you did not opt to create a desktop icon, the icon is located at C:\Program Files (x86)\MC3390X\_GUI.

## 6.2 Configuring the Hardware

Figure 8 shows the setup required to use KIT34FS6407EVB or KIT34FS6408EVB.



KIT34FS6407EVB/KIT34FS6408EVB

Figure 8. Evaluation Board Setup

#### 6.2.1 Step-by-step Instructions for Setting Up the Hardware

Set up the KIT34FS6407EVB/KIT34FS6408EVB hardware and software as follows:

- 1. Install the software GUI (either SPIGen or MC3390X\_GUI) on your computer (See Section 6.1 "Installing the GUI Software".)
- 2. Flip the KITUSBSPIDGLEVME Interface Dongle over and mount its IO Port connector to Connector J24 on the evaluation board.
- 3. Connect a USB cable from the Interface Dongle to the PC.
- 4. Set the EVB jumpers and switches as needed. Refer to Figure 3 for an example.
- 5. Select Debug or Normal mode with jumper J17.
- 6. Attach loads to connector JP1 as needed.
- 7. Attach DC power supply on J3 or J7 (maximum voltage: 40 V).
- 8. Switch SW1 to supply the board.
- If SW2 switches are ON and V<sub>BAT</sub> is set correctly, then V<sub>PRE</sub>, V<sub>CCA</sub>, V<sub>AUX</sub>, CAN\_5 V LEDs should turn ON. V<sub>BAT</sub> value is dependent on V<sub>PRE</sub> configuration. In Buck mode, it must be 8.2 V min. FS0B LED should turn ON (J13 / J30 must be plugged).



### 6.3 Running the GUI

With the KIT34FS6407/8 EVB's, you are provided with two separate graphical user interfaces (GUI's) that allow you to configure registers:

- SPI generator (SPIGen)
- MC3390X\_GUI

Both GUI's are similar in function. You may use either one at your own discretion.

#### 6.3.1 Running SPIGen

To run SPIGen, do the following:

- 1. Click on the SPIGen icon. This icon appears on your desktop if you elected to create a short-cut during the installation process. Otherwise, the icon resides in the folder C:Program Files\SPIGen. The generic SPIGen start-up screen appears.
- From the SPIGen menu bar, click on FILE>Open and select the configuration file "MC33907\_8\_SPIGEN.spi" (previously downloaded in Section 6.1.1.) Figure 9 shows SPIGen screen with the configuration file installed.
- 3. In Debug mode, use the SPIGen batch RST\_counter\_to\_0.spi to reset the error counter. FS0B should turn off (LED D12 turned off).

At this stage, EVB is powered and SPIGen is working. When Normal mode is selected with J17, a valid WD must be sent, otherwise the device goes into deep fail-safe.

		ic SPI Generator		
File Edit View Configuration				
🗅 🚅 🛃   🐰 🗈 🛍   🏟 🥝 Words				
vice View D ×	Word To Send		4 13 12 11 10 4 13 12 11 10	SPI Word Sent           9         8         7         6         5         4         3         2         1         0           SPI Word Received           9         8         7         6         5         4         3         2         1         0           SPI Word Received           9         8         7         6         5         4         3         2         1         0           Image: second colspan="4">Image: second colspan="4">SPI Word Received           9         8         7         6         5         4         3         2         1         0           Image: second colspan="4">Image: second colspan="4">Image: second colspan="4">Image: second colspan="4">SPI Word Received           9         8         7         6         5         4         3         2         1         0           Image: second colspan="4">Image: second colspan="4">SPI Word Received           Image: second colspan="4">Image: second colspan="4"
☑ Generic		Length In Bits	s: 🔘 8 💿 16 🔘	24 32 40 Binary O Hex
<ul> <li>MC33813</li> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC331HB2001</li> </ul>	SPI Word Session Log	Evtra Dine		Send Once Send Continuously
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> </ul>	SPI Word Session Log	Extra Pins		
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0	High Low	Quick Commands
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1	High Low	Send Once Continuously
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1 Data 2	High Low High Low	Quick Commands
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1 Data 2 Data 3	High Low High Low High Low	Quick Commands
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1 Data 2	High Low High Low	Quick Commands Quick Commands CAN_LIN_MODE READ CAN_LIN_MODE READ CAN_LIN_MODE reable CAN_LIN_MODE_reable CAN_LIN_MODE_reable DIAG_CAN_LIN_READ DIAG_CAN_READ DIAG_CAN_READ DIAG_CAN_READ
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1 Data 2 Data 3	High Low High Low High Low	Quick Commands Quick Commands CAN_LIN_MODE CAN_LIN_MODE CAN_LIN_MODE_CAN_LIN_MODE CAN_LIN_MODE_CAN_CAN_CAN_CAN_CAN_CAN_CAN_CAN_CAN_CAN
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1 Data 2 Data 3 Data 4	High Low High Low High Low High Low	Quick Commands Quick Commands CAN_LIN_MODE CAN_LIN_MODE_READ CAN_LIN_MODE_READ CAN_LIN_MODE_clear CAN_LIN_MODE_clear CAN_LIN_MODE_x80C0 DIAG_CAN_EAD DIAG_SPI_READ DIAG_SP
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1 Data 2 Data 3 Data 4 Control 0	High Low High Low High Low High Low	Quick Commands Quick Commands CAN_LIN_MODE CAN_LIN_MODE,READ CAN_LIN_MODE,READ CAN_LIN_MODE,clear CAN_LIN_MODE,clear CAN_LIN_MODE,x00C0 DIAG_CAN_EAD DIAG_FS1,READ DIAG_SF1,READ DIAG_SF
<ul> <li>MC33814</li> <li>MC33816</li> <li>MC33909</li> <li>MC33978</li> <li>MC33HB2001</li> </ul>	SPI Word Session Log	Data 0 Data 1 Data 2 Data 3 Data 4 Control 0 Control 1	High Low High Low High Low High Low High Low High Low	Quick Commands CAN_LIN_MODE CAN_LIN_MODE CAN_LIN_MODE_CAN_LIN_MODE CAN_LIN_MODE_cable CAN_LIN_MODE_cable CAN_LIN_MODE_cable CAN_LIN_MODE_sable DIAG_CAN_READ DIAG_SABLEAD DIAG_SABLEAD DIAG_VREG_READ DIA

Figure 9. SPIGen Screen



In order to fill a specific need, it is also possible to edit registers with another value and to save it for further use, either as standalone or inside a batch.

Figure 10 shows a batch called "RST\_counter\_to\_0", as an example. This batch file automatically installs when the configuration file is loaded. To select the batch file, click on the Batch Name box at the bottom right side of the screen.

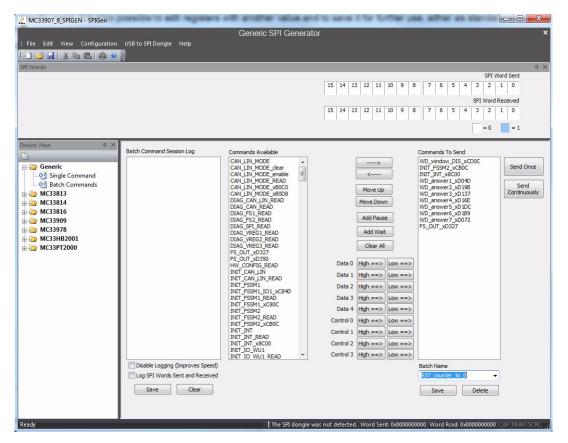


Figure 10. RST\_counter\_to\_0 Batch

At startup or when resuming from LPOFF mode the reset error counter starts at level 1 and FS0B is asserted low. To remove activation of FS0B, the RST error counter must go back to value "0" (seven consecutive good WD refresh decreases the reset error counter down to 0) and a right command is sent to FS\_OUT register. This can be demonstrated with this batch running in debug mode.

The batch shown in Figure 10 executes the following action:

- WD\_Window\_DIS\_xCD0C:
  - Disables normal WD
- INIT\_FSSM2\_xCB0C:
  - IO\_23\_FS bits configured in "NOT SAFETY" mode
- WD\_answer1 to WD\_answer7:
  - If the part is in debug mode, this sends the right first WD answer and allows the reset counter to change to 0
- FS\_OUT\_xD327:
  - · Disables FS0B pin, coming back to high level (D12 turned off)
- INIT\_INT\_x8C00:
- · Closes the init phase of the main state machine
- CAN\_MODE\_B0C0:
  - · Enables CAN transceiver



#### 6.3.2 Running the MC3390X\_GUI

The MC3390X\_GUI allows you to program all SPI features by using a friendly interface. Advanced users can also use MC3390X\_GUI to modify the register table manually.

1. To launch the MC3390X\_GUI application, click on the application icon located either on your desktop or in Program Files menu as shown in Figure 11.



Figure 11. Launching MC3390X\_GUI application

2. When the MC3390X\_GUI launches, click on the dropdown box under "Choose Interface" and select the appropriate device. (See Figure 12.)

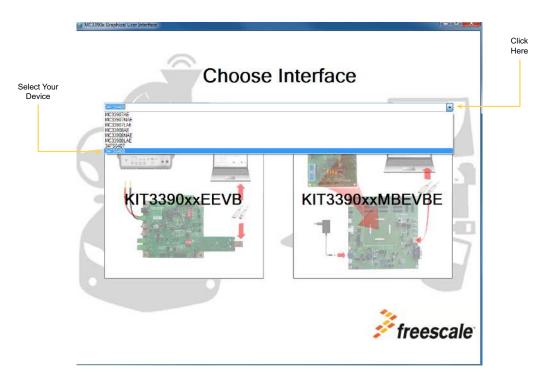


Figure 12. MC3390X\_GUI Device Selection

Click on the "KIT3390xxEEVB" button on the left side of the screen. (See Figure 13.)

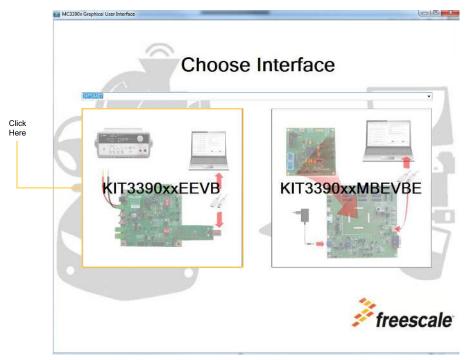


Figure 13. MC3390X\_GUI Configuration Selection

3. A screen similar to the one in Figure 14 appears showing the status of the registers at startup. In this example, register INIT\_FSSM2 has bit IO\_23\_FS configured as SAFETY CRITICAL.

PowersB									o E S
oad registe	onfiguratio	a serie	2 Read r	E entripe	Reading	sters 4	Read redist	era 5 De 1 *	INIT_Supervisor1 INIT_Supervisor2 INIT_Supervisor3 INIT_FSSM1 INIT_FSSM2 WD *
Vieg_LPOP Reserved	1	Reserved	Reserved	Reserved		-		Read	Configue the couple of 10, 32 as cafety reput for Foos monitoring O HOT SAPETY B EAPETY CRITICAL
INIT_Super	1	SPI_F5_ Raq	SPI_FS_P arty	Veens, FS	Vacia 75	Vess 15	Vess 15		Configue the values of the FSTS entorcourse: (a) Intermediate -3; Intel - 6 (b) Intermediate -1; Intel - 3
INIT_Super SP(_F5_6 IT	T	SPL_FS_ Req	SPI_FS_P artly	0	DIS_8s	Yang St	Voux FS	9	Configue the Foox potency  (I) foox_execut_1-0 active HIGH  (I) foox_execut_1-0 active HIGH  (I) foox_execut_1-0 active LOW
INIT_Super	T	SPI_FS_ Raq	spi_Fs_P arty	o	Voore_5D	Vccs_5D	Veux,50	V	Configure the FQ1 FWM (hequency and duty cycle @ ( +1 25 Hz DC +5 %) () ( + 100 Hz DC +10%)
INIT_FSSN SPI_FS_a If	-	SPI_FS_ Reg	SPI_PS_P arity	10_01_FS	10_1_FB	10_45_FS	RST5_low	(V)	P
INIT_FSSN SPI_F3_e E	1	SPLF3 Req	SPLPS_P arty	Aut en	10,22,75	8	F_F\$1	R)	
WD_windo SPI_FS_e II	1	SPLFS_ Req	SPUPS_P alty	WD_wind ow_3	WD_wind ow_2	W0,2eiN cw_1	WD_wind pw_3	Ø	
			Reed a	elected				Select all	RSTD_WI         IO_20_FS         P3         F_FS1         Secure 3         Secur
Generic ST/	ATUS								Laztionmiands
SP1_G	wu	CAN_S	UN_G	10_6	vpr_4		Votiers_		Geologicologicol Received WD_WINDOW Cx0703 06000011100000011

Figure 14. MC3390X\_GUI Main Screen



4. In the right side of the GUI, select NOT SAFETY and send the command as shown in Figure 15.

PowerSE	nc gut								inter Or
File Co	onfiguratio	on Helj	p						
ead registe	na 1 Rea	ed registers	2 Read	registers 3	Read reg	gistors 4	Read register	es 5 Del 1 1	INIT_Supervisor1 INIT_Supervisor2 INIT_Supervisor3 INIT_FSSM1 INIT_FSSM2 WD_1
Vieg_LPO	1	Reserved	Reserved	Reserved	Vera 3/	W00#.341	NR. D	Read	Configue theough of IQ-32 as asfely reputs for Focultantioning NOT SAFETY SAFETY CRITICAL
INIT_Supe SPI_FS_6 17	SPI_FS_ GLK	SPI_FS_ Req	SPL_FS_P arky	Verm_Fil	Vece Pi	Voor #S	Voor,FS	120	Configure the values of the RSTD enco counter (9) Insumadates 43, final = 6 (1) Insumadates +3, final = 3
INIT_Supo SPI_FS_+ II	1	SPI_FS_ Req	SPI_FS_P arty	a	DIS_Ba	Nac B	Wangth		Configure the Focu polarity (a) focus poort_10 polyre HIBH (box_exout_10 polyre HIBH
INIT_Bupe SPI_RS_e IT	1	SPL FS_ Req	SPI_FS_P arty	0	Voore_50	Voce_50	Vmux_50	19	Configure the FB1 FWM beguency and duty optie
INIT_F359	M1								
SPI_FS_t II	SPI_FS_ CLK	SPI_FS_ Req	SPLFS_P arity	10_01_FS	IO_1_FS	10_45_F5	RST0_low	12	
INIT_FSS!	M2								
3P1_F3_4 11	SPI_F3_ CLK	SRLFS_ Reg	SPL_FS_P ality	RST or	10,23,FS	PS	F_FS1	IV.	
WD_winds	ow.				$\sim$				
SPI_FS_0 T	SPI_FS_ CLK	SPLFS_ Heg	SPLFS_P arty	WO_wind ov_2	WD_wind ovr_2	W02.9941 297_2	WU_west DN_U	121	
			Reads	elected				Sciect all	RGTp.err _FS 10_22_FS PS F_FS1 Inver_3 Inver_3 Rearr, Store_5 Store_5
Generic ST/	ATUS								Last commanda
691_G	WU	CAN_S	UN_G	10_6	Vpe G	Voore &	Muthama	2	0b100101100001100 Received INIT_FSSN2 0±0700 0b0000011100000000

Figure 15. MC3390X\_GUI Register

# 7 Initialization and Configuration Mode

## 7.1 INIT Phase

INIT registers are set to their default values after each POR (power-on reset.) This default configuration is compatible with the default EVB settings except for the INIT FSSM2 register. Bit IO\_23\_FS in this register is set by default, which means the fail-safe outputs (FCCU\_x of the MPC5643L or similar device) have to be connected to the IO's 2 and 3 of the MC34FS6407or MC34FS6408. If MPC5643L (or a similar device) is not used, the bit IO\_23\_FS has to be cleared during INIT phase (setting shown in Table 10). The INIT phase of the main part completes with a Write command to the INIT\_INT register. This command closes access to the INIT registers and the device goes into Normal mode. The same sequence (INIT\_FSSM2, INIT\_INT) must occur in both Debug and Standard mode. The only difference is in the timeout constraints used for the Standard mode. In the Standard mode, INIT commands have to be sent before the 256 ms timer (starting from the RST pin release) expires.

#### Table 10. INIT FSSM2 Setting

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	1	Р	RSTB_ err_FS	IO_23_ FS	PS	F_FS1	Secure _3	Secure _2	Secure _1	Secure _0
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0

# 7.2 Normal Operation

During normal operation (after INIT phase), both modes (Normal and Debug) allow you to send to send a WD refresh command. In Debug mode, no action is taken on a bad WD response. In Normal mode, the KITUSBSPIDGLEVMESPI interface dongle cannot guarantee the WD refresh period (Windows XP and Windows 7 are not real-time operating systems.) Nevertheless, WD refresh works in Standard mode using a WD window duration of 512 ms (reconfigured in the INIT phase).

# 7.3 Debug Mode

The KIT34FS6407EVB or KIT34FS6408EVB is mainly intended to be used in Debug mode. In Normal mode you must either use an MCU that is able to manage the WD or you must disable WD. If WD is enabled, you must send a valid WD response at startup. The response must occur within the 256 ms windows after reset release. You must then update WD at the right time. With KIT34FS6407EVB or KIT34FS6408EVB attached to the KITUSBSPIDGLEVME, this must be done manually (which is feasible, depending on the device's register configuration.)



8

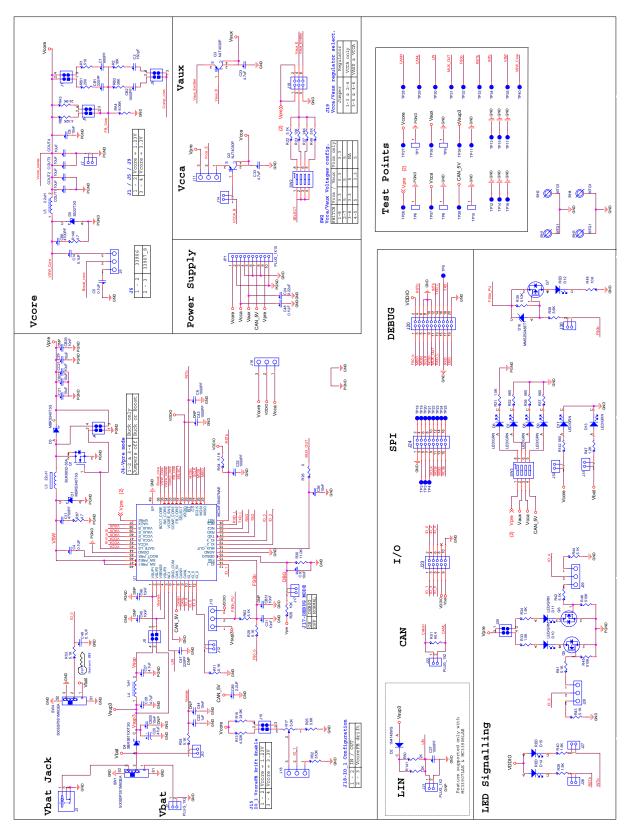


Figure 16. Evaluation Board Schematic



# 9 Board Layout

# 9.1 Assembly Layer Top

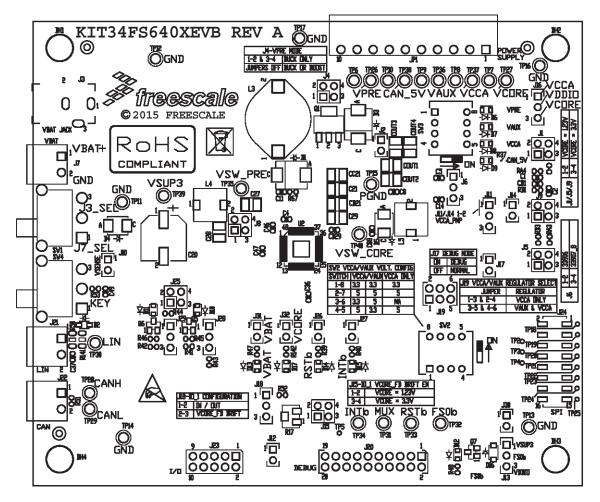
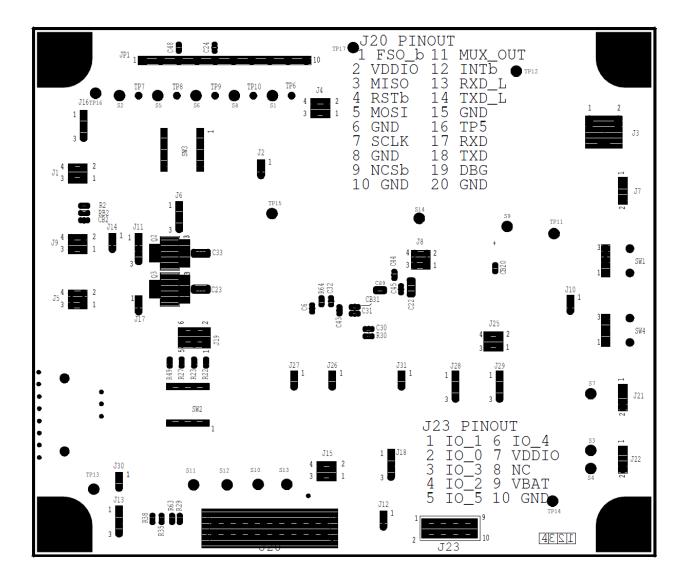


Figure 17. KIT34FS6407EVB/KIT34FS6408EVB Assembly Layer Top



#### 9.2 Assembly Layer Bottom



#### Figure 18. KIT34FS6407EVB/KIT34FS6408EVB Assembly Layer Bottom

#### NOTE:

This image is an exception to the standard top-view mode of representation used in this document. It has been flipped to show a bottom view.



# 9.3 Bill of Materials

#### Table 11. Bill of Materials <sup>(1)</sup>

ltem	Qty	Schematic Label	Value	Manufacturer	Part Number	Assy Op
Active	Compo	nents				
1	1	U1		Freescale Semiconductor	MC34FS6407 or MC34FS6408	(3)
Capaci	tors					-
2	1	C1	680 pF	KEMET	C0603C681J5GAC	
3	1	C2	150 pF	KEMET	C0603C151J5GAC	
4	5	C4, C5, C14, C48, C49	0.1 µF	KEMET	C0603C104K3RAC	
5	4	C6, C32, C37, CB2	1000 pF	AVX	06035U102KAT2A	
6	4	C8, C30, C31, C36	10 nF	AVX	06035C103JAT2A	
7	2	C11, C88	4700 pF	Yageo America	CC0603KRX7R9BB472	
8	1	C20	47 µF	Nippon Chemi-Con Corporation	EMVH500ADA470MJA0G	
9	4	C21, C29, CB21, CC21	10 µF	ток	CGA6M3X7R1C106K	(3)
10	1	C22	1.0 µF	TDK	CGA5L3X7R1H105K160AB	
11	2	C23, C33	4.7 µF	Murata	GCM31CR71C475KA37	
12	1	C24	0.22 μF	KEMET	C0603C224K3RACTU	
13	2	C27, C28	4.7 µF	Murata	GCM32ER71H475KA55L	
14	1	C43	1000 pF	AVX	06035U102KAT2A	(2)
15	6	C44, C45, C46, CB20, CB29, CB31	10 nF	AVX	06035C103JAT2A	(2)
16	1	C47	220 pF	KEMET	C0603C221K5GACTU	(2)
17	1	C89	2.2 µF	AVX	08053C225KAT2A	
18	1	CB1	220 pF	KEMET	C0603C221K5GACTU	
19	4	COUT1, COUT2, COUT3, COUT4	10 µF	Murata	GCM32ER71E106KA57	(3)
Diodes				1		1
20	2	D1, D3	MBRS340T3G	ON Semiconductor	MBRS340T3G	(3)
21	1	D2	1N4148WS	Diodes Inc	1N4148WS-7-F	
22	1	D4	SBRS81100T3G	ON Semiconductor	SBRS81100T3G	(3)
23	1	D5	SS22T3G	ON Semiconductor	SS22T3G	
24	8	D6, D7, D8, D9, D10, D11, D13, D17	LED/GRN	OSRAM	LP M67K-E2G1-25	
25	3	D12, D14, D15	RED	OSRAM	LS M67K-H2L1-1-0-2-R18-Z	
26	1	D16	MMSZ5248ET1	ON Semiconductor	MMSZ5248BT1G	1



## Table 11. Bill of Materials <sup>(1)</sup> (continued)

Item	Qty	Schematic Label	Value	Manufacturer	Part Number	Assy Opt
Conne	ctors					
27	7	J1, J4, J5, J8, J9, J15, J25	HDR 2X2	Samtec	TSW-102-07-G-D	
28	10	J2, J10, J12, J14, J17, J26, J27, J30, J31, J32	HDR 1X2	Samtec	TSW-102-07-T-S	
29	1	J3	CON_1_PWR	CUI Stack	PJ-102AH	
30	7	J6, J11, J13, J16, J18, J28, J29	HDR_1X3	Tyco Electronics	826629-3	
31	3	J7, J21, J22	PLUG_1X2	Phoenix contact	1803277	
32	1	J19	HDR 2X3	Tyco Electronics	1-87215-2	
33	1	J20	HDR_10X2	Samtec	TSW-110-07-S-D	
34	1	J23	HDR 2X5	Samtec	TSW-105-07-G-D	
35	1	J24	NPPC082KFMS-R C	Sullins Electronics Corp	NPPC082KFMS-RC	
36	1	JP1	PLUG_1X10	Phoenix contact	1803358	
Induct	ors		1	I		/
37	1	L3	22µH	EPCOS	B82479G1223M000	(3)
38	1	L4	1.0 µH	EPCOS	B82472G6102M000	(3)
39	1	L5	2.2 µH	EPCOS	B82472G6222M000	
Transis	stors					
40	1	Q1	BUK9832-55A	NXP Semiconductors	BUK9832-55A,115	(3)
41	2	Q2, Q3	NJT4030P	ON Semiconductor	NJT4030PT3G	(3)
42	2	Q5, Q6	MMBF0201NLT1 G	ON Semiconductor	MMBF0201NLT1G	
43	1	Q7	BSS84LT1	ON Semiconductor	BSS84LT1G	
Resist	ors		·			
44	1	R1	510 K	Bourns	CR0603-JW-511ELF	
45	1	R2	18 K	KOA Speer	RK73H1JTTD1802F	
46	10	R11, R24, R29, R41, R42, R43, R44, R53, R63, R64	5.1 K	Vishay Intertechnology	CRCW06035K10JNEA	
47	2	R13, RB3	4.32 K	KOA Speer	RK73H1JTTD4321F	
48	2	R15, RA3	24.9 K	KOA Speer	RK73H1JTTD2492F	
49	1	R17	5.0 K	Bourns	3224W-1-502E	
50	1	R22	5.1 K	KOA Speer	RK73H1JTTD5101F	
51	1	R23	12 K	Bourns	CR0603-JW-123ELF	
52	1	R25	5.6 K	KOA Speer	RK73H1JTTD7151F	
53	1	R26	0	Vishay Intertechnology	CRCW06030000Z0EA	
54	1	R27	24 K	Panasonic	ERJ-3GEYJ243V	
55	2	R28, R48	10 K	KOA Speer	RK73B1JTTD103J	



#### Table 11. Bill of Materials <sup>(1)</sup> (continued)

ltem	Qty	Schematic Label	Value	Manufacturer	Part Number	Assy Opt
56	1	R30	11 K	KOA Speer	RK73H1JTTD1102F	
57	5	R31, R33, R34, R39, R40	1.5 K	Bourns	CR0603-JW-152ELF	
58		R32, R36, R37, R142	560 K	KOA Speer	RK73B1JTTD561J	
59	3	R35, R45, R46, R52	510 K	KOA Speer	RC0603JR-07510KL	
60	1	R38	5.6 K	KOA Speer	RK73B1JTTD562J	
61	1	R47	1.2 K	KOA Speer	RK73H1JTTD1201F	
62	1	R49	51 K	Vishay Intertechnology	CRCW060351K0JNEA	
63	2	R50, R141	2.0 K	Yageo	RC1206JR-072KL	
64	1	R51	60.4	KOA Speer	RK73H1JTTD60R4F	
65	2	R67, R140	4.7	Bourns	CR0603-JW-4R7ELF	
66	1	RA4	8.06 K	KOA Speer	RK73H1JTTD8061F	
67	1	RB1	200 K	KOA Speer	RK73B1JTTD201J	
68	1	RB2	39 K	KOA Speer	RK73H1JTTD3902F	

#### Switches

69	2	SW1, SW4	500SSP3S1M6QE A	E Switch	500SSP3S1M6QEA	
70	2	SW2, SW3	SW_DIP-4_SM	Grayhill	78RB04ST	

#### Test Points

71	12	TP2, TP3, TP4, TP5, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25	TP_PTH	NOT A COMPONENT	NOT A COMPONENT	
72	5	TP6, TP7, TP8, TP9, TP10	5006	Keystone Electronics	5006	(2)
73	7	TP11, TP12, TP13, TP14, TP15, TP16, TP17	TESTLOOP_BLA CK	Keystone Electronics	5011	
74	15	TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40	TESTLOOP_RED	Keystone Electronics	5010	

Notes

1. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

2. Do not populate.

3. Critical components. For critical components, it is vital to use the manufacturer listed.



# 10 References

Following are URLs where you can obtain information on related Freescale products and application solutions:

Freescale.com Support Pages	Description	URL
KIT34FS6407EVB	Tool Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KIT34FS6407EVB
MC34FS6407	Product Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC34FS6407
KIT34FS6408EVB	Tool Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KIT34FS6408EVB
MC34FS6408	Product Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC34FS6408
SPIGen	Software	http://www.freescale.com/files/soft_dev_tools/software/device_drivers/SPIGen.html
KITUSBSPIDGLEVME	Interface Dongle	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KITUSBSPIDGLEVME

### 10.1 Support

Visit www.freescale.com/support for a list of phone numbers within your region.

## 10.2 Warranty

Visit www.freescale.com/warranty to submit a request for tool warranty.



# 11 Revision History

Γ	Revision	Date	Description of Changes
	1.0	6/2015	Initial Release
		8/2015	Corrected typo





How to Reach Us:

Home Page: freescale.com

Web Support: freescale.com/support Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo, Energy Efficient Solutions, and SafeAssure logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. SMARTMOS is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2015 Freescale Semiconductor, Inc.

Document Number: KT34FS6407-34FS6408UG Rev. 1.0 8/2015

