Two Channel SATA 3 Gbps Redriver With Cable Detect

Check for Samples: SN75LVCP412CD

FEATURES

- **Fully Integrated Cable Detect Feature Compliant with SATA 2.6 Spec**
- **Enables System Power Savings of up to 200mW When HDD is Not Detected at eSATA Connector**
- **Low Device Power**
  - **<200mW (Typ) in Active Mode**
  - **<20mW (Typ) in Auto Low Power Mode**
  - **<2mW (Max) in Standby Mode**
- **Supports Common Mode Biasing for OOB Signaling with Fast Turn-On**
- **Channel Selectable Output Pre-Emphasis**
- **Excellent Jitter and Loss Compensation Capability to Over 20" FR4 Trace**
- **High Protection Against ESD Transient**
  - **HBM: 8,000V**
  - **CDM: 1,500V**
  - **MM: 200V**
- **20 Pin QFN 4x4 Package**
- **Pin Compatible to LVCP412/LVCP412A**

APPLICATIONS

- **Notebooks, Desktops, Docking Stations, Servers and Workstations**

DESCRIPTION

The SN75LVCP412CD is a dual channel, single lane SATA redriver and signal conditioner supporting data rates up to 3.0Gbps that complies with SATA spec revision 2.6.

The SN75LVCP412CD operates from a single 3.3V supply. Integrated 100-Ω line termination and self-biasing make the device suitable for AC coupling. The inputs incorporate an OOB detector which automatically turns the differential outputs off while maintaining a stable output common-mode voltage compliant to SATA link. The device is also designed to handle SSC transmission per SATA spec.

The SN75LVCP412CD handles interconnect losses at both its input and output. The built-in transmitter pre-emphasis feature is capable of applying 0dB or 2.5dB of relative amplification at higher frequencies to counter the expected interconnect loss. On the receive side the device applies a fixed equalization of 7dB to boost input frequencies near 1.5GHz. Collectively, the input equalization and output pre-emphasis features of the device works to fully restore SATA signal integrity over extended cable and backplane pathways.

The device is hot-plug capable(1) preventing device damage under device *hot*-insertion such as async signal plug/removal, un-powered plug/removal, powered plug/removal or surprise plug/removal.

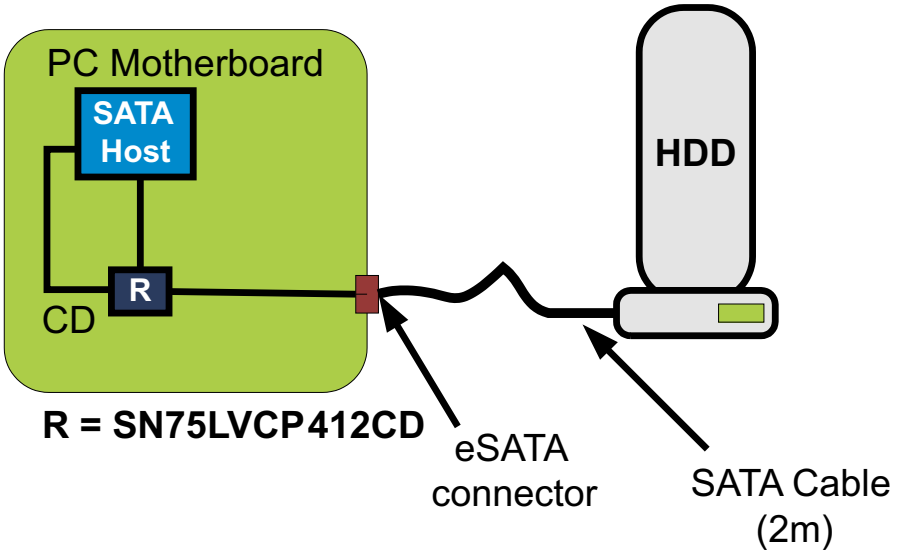
(1) Requires use of AC coupling capacitors at differential inputs and outputs

ORDERING INFORMATION(1)

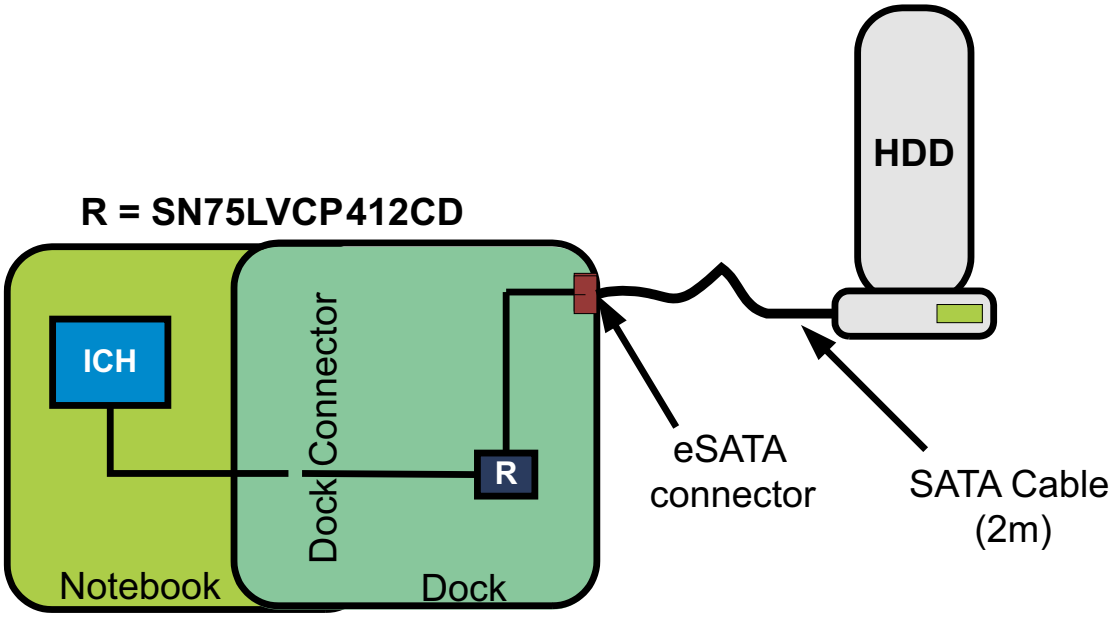
PART NUMBER	PART MARKING	PACKAGE
SN75LVCP412CDRTJR	412CD	20-pin RTJ reel (large)
SN75LVCP412CDRTJT	412CD	20-pin RTJ reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



In Notebook and Desktop Motherboard



In Notebook Dock

Figure 1. Typical Application

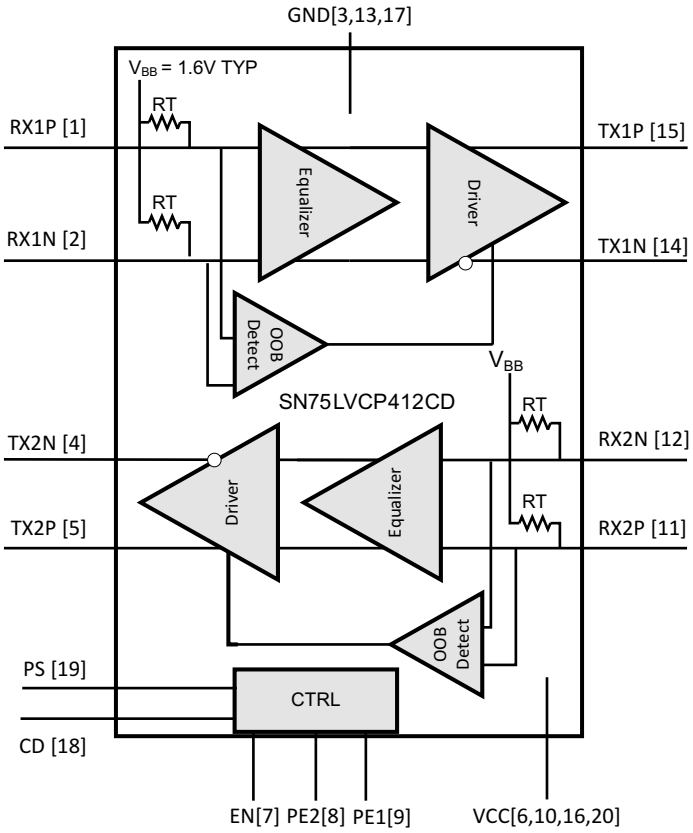
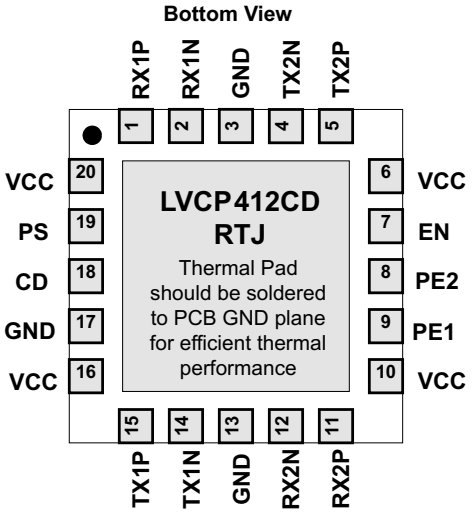
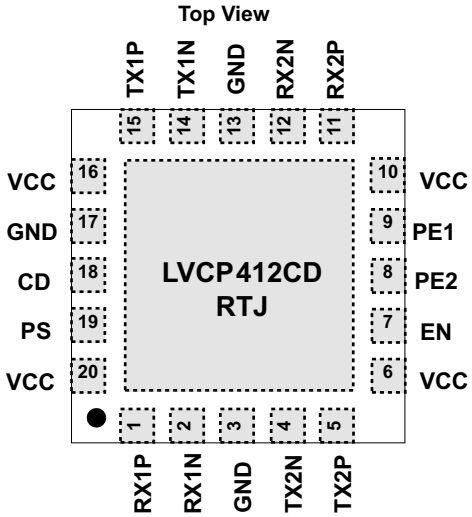


Figure 2. Block Diagram

PIN ASSIGNMENTS





PIN FUNCTIONS

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O			
2	RX1N	I, VML	Non-inverting and inverting CML differential inputs for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit.
1	RX1P	I, VML	
12	RX2N	I, VML	
11	RX2P	I, VML	
14	TX1N	O, VML	Non-inverting and inverting CML differential outputs for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors.
15	TX1P	O, VML	
4	TX2N	O, VML	
5	TX2P	O, VML	
CONTROL PINS			
7	EN	I, LVCMOS	Device enable pin. Internally PU to VCC.
18	CD	O, LVCMOS	Indicates presence or absence of external HDD attachment to LVCP412CD (via eSATA connector).
19	PS	I, LVCMOS	Selects/de-selects cable detect feature of device. Internally PU to VCC.
8, 9	PE1, PE2	I, LVCMOS	Selects pre-emphasis settings for CH 1 and CH 2 per Table 4. Internally PD to GND.
POWER			
6, 10, 16, 20	VCC	Power	Positive supply, should be 3.3V ±10%.
3, 13, 17	GND	Power	Supply ground

DEVICE SETTINGS

Table 1. Device State

EN	DEVICE STATE	DESCRIPTION
H	Active	ALP(1) enabled (default state)
L	Standby	Device in standby mode

(1) ALP = Auto low power mode active

Table 2. Enabling/Disabling Cable Detect via PS Pin

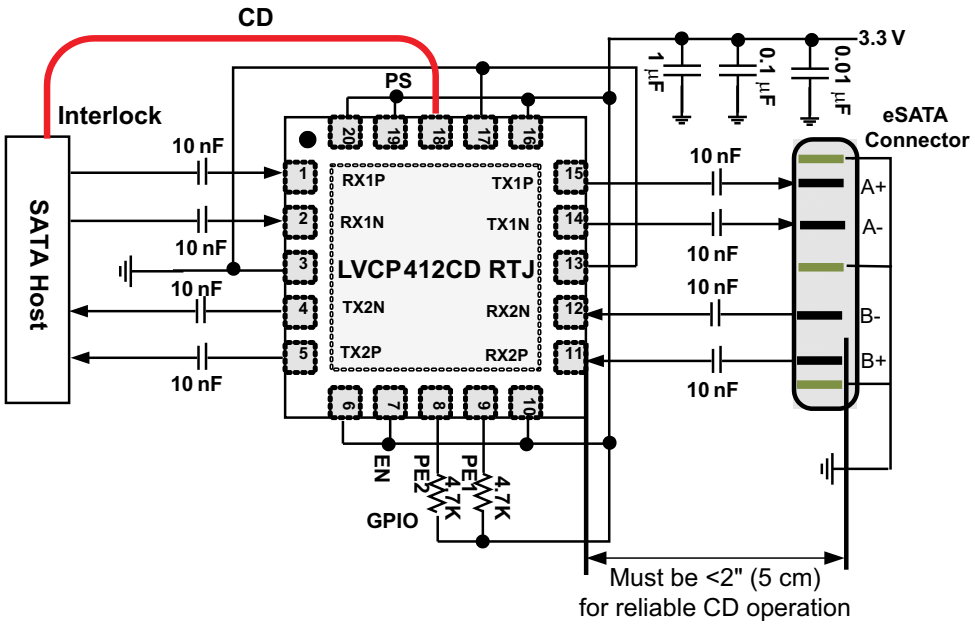
PS	CABLE DETECT FEATURE	DESCRIPTION
L	Disabled	CD feature is not enabled
H	Enabled	CD feature is enabled (default state)

Table 3. Cable Detect Status Indicator Pin

CD	CABLE CONNECTION STATUS	DESCRIPTION
L	Valid connection ***detected*** at eSATA port	Ext HDD attached
H	Valid connection ***NOT*** detected at eSATA port	Ext HDD NOT attached

Table 4. Output Pre-Emphasis (Device in active state)

PE1	PE2	FUNCTION
0	0	***Normal SATA output (default state); CH 1 and CH 2 → 0 dB***
1	0	CH 1 → 2.5 dB pre-emphasis; CH 2 → 0 dB
0	1	CH 2 → 2.5 dB pre-emphasis; CH 1 → 0 dB
1	1	CH 1 and CH 2 → 2.5 dB pre-emphasis



(1) Place supply caps close to device pin.

(2) Device shown with cable detect mode ON (PS=H, EN=H).

(3) Output pre-emphasis (PE1, PE2) is shown enabled. Setting will depend on device placement relative to eSATA connector.

(4) For reliable cable detect operation, CH1 trace length to eSATA connector pin must be within 2" (<5 cm).

Figure 3. Device Implementation

OPERATION DESCRIPTION

INPUT EQUALIZATION

Each differential input of the SN75LVCP412CD has +7dB of fixed equalization in its front stage. The equalization will amplify high frequency signals to correct for loss from the transmission channel. The input equalizer is designed to recover a signal even when no eye is present at the receiver and will affectively support a FR4 trace at the input anywhere from <4 inches to 20 inches or <10 cm to >50 cm.

OUTPUT PRE-EMPHASIS

The SN75LVCP412CD provides single step pre-emphasis from 0dB to 2.5dB at each of its differential outputs. Pre-emphasis is controlled independently for each channel and is set by the control pins PE1 and PE2 as shown in Table 4. The pre-emphasis duration is 0.7 UI or 133ps (typ) at SATA 3.0Gbps speed.

LOW POWER MODES

- Standby Mode (Triggered by EN pin when EN = H→L)

  Standby mode is controlled by enable (EN) pin. In its default state this pin is internally pulled high, pulling this pin LOW will put the device in standby mode within 2us (max). In this mode all active components of the device are driven to their quiescent level and differential outputs are driven to Hi Z (open). Max power dissipation is 2mW. Exiting to normal operation requires a maximum latency of 20 us.

- Auto Low Power Mode (Triggered when a given channel is in electrical idle state for >10us and EN = H, PS = X)

  Device enters and exits low power mode by actively monitoring input signal (VIDp-p) level on each of its channel independently. When input signal on either or both channel is in the electrical idle state, i.e. VIDp-p < 50mV and stays in this state for > 18 µs the associated channel(s) enter low power state. In this state, output of the associated channel(s) is held to TX VCM and device selectively shuts off some circuitry to lower power by >75% of its normal operating power. Exit time from auto low power mode is less than 50ns (max).

Cable Detect Feature (see Figure 4 and Figure 5)

Cable detect mode (for this mode to be active PS and EN must be tied H via a 4.7kΩ or both pins left as NC. Device must be placed < 2" (or <5cm) from eSATA connector).

To use this feature CH 1 input must be connected to SATA host while CH 2 input to eSATA connector. After power up device sets CD = 0, which makes the SATA Host monitoring this pin go into normal SATA OOB state where host will send out COMRESETs (refer to SATA spec ver. 2.6 Gold) to look for a connected device. The LVCP412CD has a detector circuit that monitors voltage level at its CH1 outputs which changes based on a closed or open termination. CD pin polarity at power up is at L and remains L if connection is found. It will transition to H if connection is not found.

In the event that an eSATA host connected to CH1 of LVCP412CD goes to Partial or Slumber mode and the ext HDD is removed, then CD pin of device will continue to remain L until Host wakes up from Partial or Slumber mode and restarts the link by sending out COMWAKE. After the transmission of first valid OOB signal from host the LVCP412CD will detect that no device is attached to esata socket and thereby pull CD pin H indicating to the host that device is removed.

eSATA host can utilize the polarity of CD pin to shutdown (CD = 1) or turn ON (CD = 0). When host is in shutdown mode then no COMRESETs are transmitted thereby saving power. After having established no connection the LVCP412CD switches to listen mode whereby it listens to COMINTS (refer to SATA spec ver. 2.6 Gold) on CH2. Per SATA spec any SATA compliant peripheral PHY, after power-up, will transmit COMINT in the event that it does not receive a valid COMRESET from the host. If COMINT is detected by the LVCP412CD on CH2 it will switch CD status to L indicating a connection has been found. The SATA host that is monitoring the status of CD pin can now turn-ON as a device is connected and the link training is subsequently established.

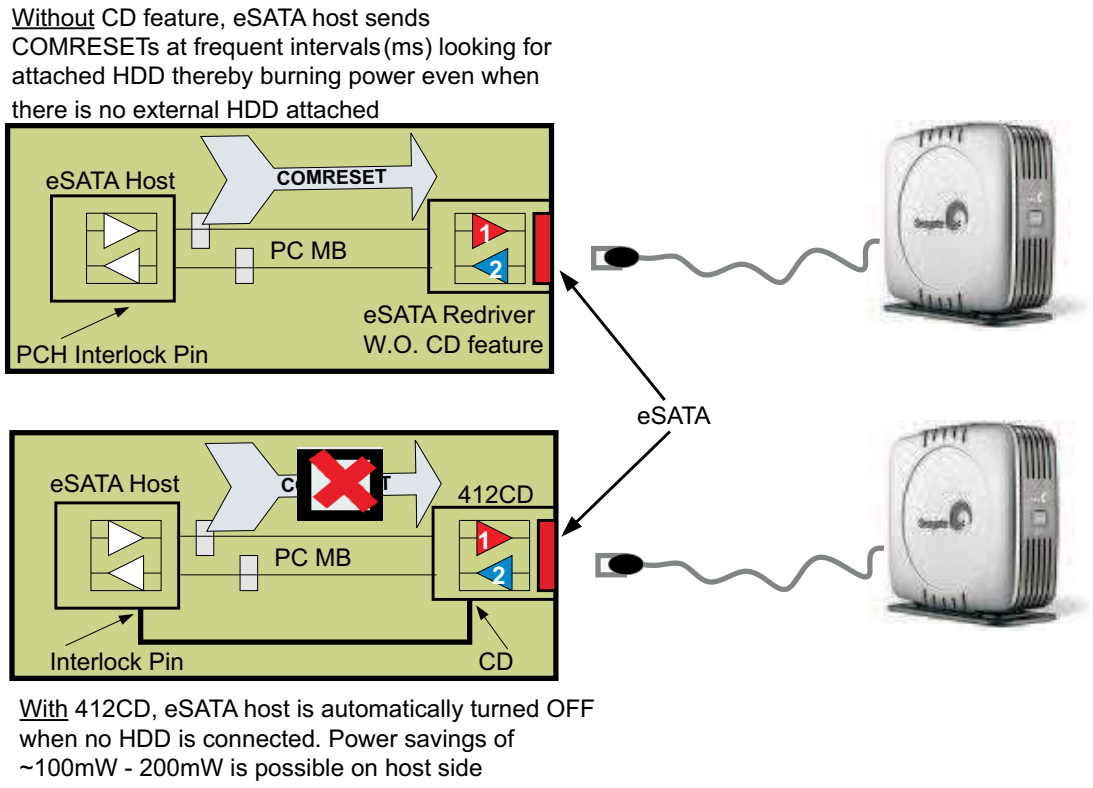


Figure 4. Cable Detect

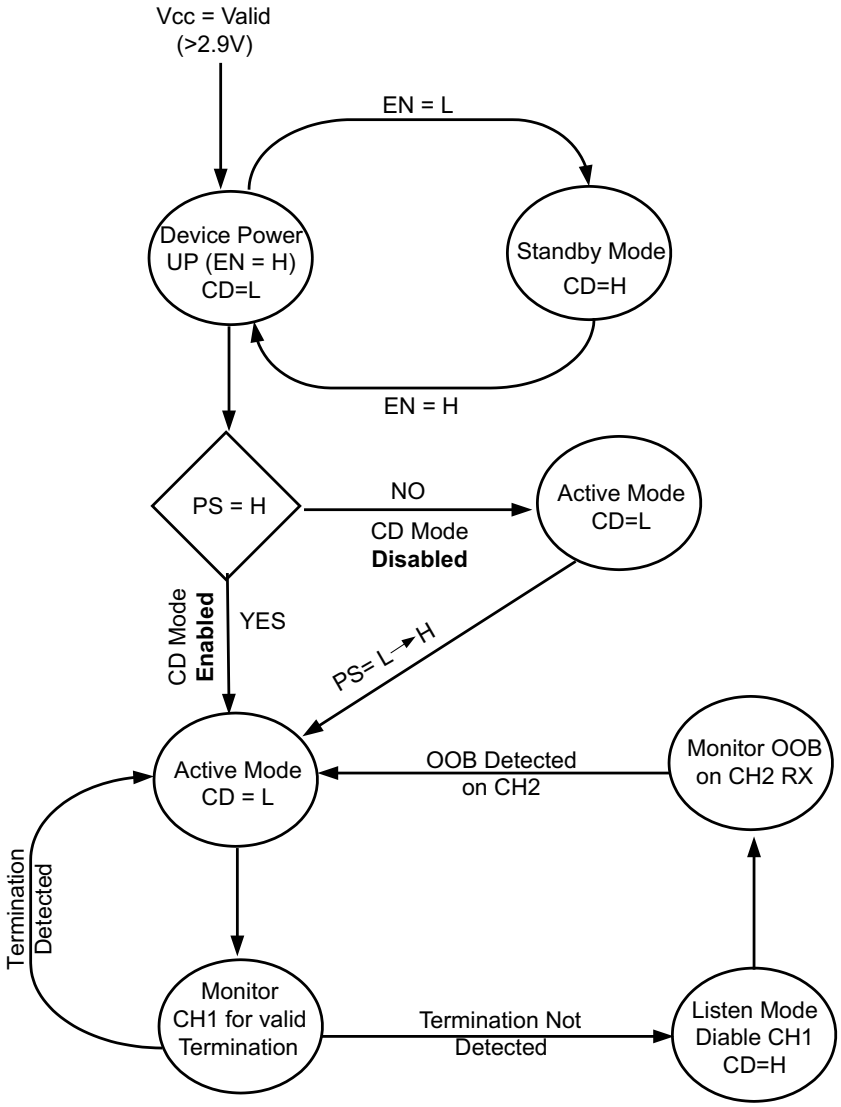


Figure 5. Device Operating States

DEVICE POWER

The SN75LVCP412CD is designed to operate from a single 3.3V supply. Always practice proper power supply sequencing procedures. Apply V_{CC} *first* before any input signals are applied to the device. Power down sequence is in reverse order.

OUT-OF-BAND (OOB) SUPPORT

The squelch detector circuit within the device enables full detection of OOB signaling as specified in SATA spec 2.6. Differential signal amplitude at the receiver input of $50mV_{p-p}$ or less is not detected as an activity and hence not passed to the output. Differential signal amplitude of 150mVp-p or more is detected as an activity and therefore passed to the output indicating activity. Squelch circuit ON/OFF time is 5ns max. While in squelch mode outputs are held to VCM.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 4	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to V_{CC} + 0.5	V
Electrostatic discharge	Human body model(3)	±8000	V
	Charged-device model(4)	±1500	V
	Machine model(5)	±200	V
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

THERMAL INFORMATION

THERMAL METRIC(1)		SN75LVCP412CD RTJ (20) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	47.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.9	
θ_{JB}	Junction-to-board thermal resistance	24.4	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	24.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

typical values for all parameters are at V_{CC} = 3.3V and T_A = 25°C. All temperature limits are specified by design.

			MIN	NOM	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$T_{Vcc0-90\%}$	Supply ramp time	Supply ramp 0V – 0.9V_{CC}		1	10	ms
$C_{COUPLING}$	Coupling capacitor			12		nF
	Operating free-air temperature		0		85	°C

DEVICE ELECTRICAL CHARACTERISTICS

under recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
P_{Active}	Device power dissipation	EN, PE1, PE2 in default state, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}		185	280	mW
I_{CC}	Active Supply Current			56	78	mA
P_{SDWN}	Standby Power	EN = 0 V		1.3	2.1	mW
I_{CCSDWN}	Standby Current			380	560	uA
I_{CC-ALP}	ALP (auto low power) supply current	Auto low power conditions met		5.0	6.5	mA
P_{ALP}	ALP (auto low power) supply power	Auto low power conditions met		17	24	mW
	Maximum data rate				3.0	Gbps
t_{PDelay}	Propagation delay	Measured using K28.5 pattern (see Figure 8)		320	450	ps
t_{ENB}	Device enable time	EN = 0 → 1			5	us
t_{DIS}	Device disable time	EN = 1 → 0			2	us
$AutoLP_{ENTRY}$	ALP entry time	Electrical idle at input, See Figure 11		18	30	us
$AutoLP_{EXIT}$	ALP exit time	After first signal activity, See Figure 11		28	50	ns
V_{OOB}	Input OOB threshold		50	90	150	mV_{pp}
t_{OOB1}	OOB mode enter	See Figure 9		4	8	ns
t_{OOB2}	OOB mode exit			5	8	ns

CONTROL LOGIC ELECTRICAL CHARACTERISTICS

under recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input high voltage (EN, PS, PE)		1.4			V
V_{IL}	Input low voltage (EN, PS, PE)				0.5	V
VIN_{HYS}	Input hysteresis (EN, PS, PE)			100		mV
I_{IH}	Input high current (EN, PS, PE)				10	µA
I_{IL}	Input low current (EN, PS, PE)				10	µA
V_{OH}	High level output voltage (CD)	I_O = -500 µA	2.7		3.6	V
V_{OL}	High level output voltage (CD)	I_O = 500 µA			0.1	V

RECEIVER AC/DC ELECTRICAL CHARACTERISTICS

under recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Z_{DIFFRX}	Differential-input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.6		V
RL_{DiffRX}	Differential mode return Loss	f = 150 MHz – 300 MHz	18	24		dB
		f = 300 MHz – 600 MHz	14	20		
		f = 600 MHz – 1.2 GHz	10	20		
		f = 1.2 GHz – 2.4 GHz	8	11		
		f = 2.4 GHz – 3.0 GHz	3	11		
RL_{CMRX}	Common-mode return Loss	f = 150 MHz – 300 MHz	5	11		dB
		f = 300 MHz – 600 MHz	5	14		
		f = 600 MHz – 1.2 GHz	2	17		
		f = 1.2 GHz – 2.4 GHz	1	16		
		f = 2.4 GHz – 3.0 GHz	1	8		
V_{diffRX}	Differential input voltage PP	f = 750 MHz and 1.5 GHz	200		2000	mVppd
IB_{RX}	Impedance balance	f = 150 MHz – 300 MHz	30	42		dB
		f = 300 MHz – 600 MHz	30	40		
		f = 600 MHz – 1.2 GHz	20	36		
		f = 1.2 GHz – 2.4 GHz	10	27		
		f = 2.4 GHz – 3.0 GHz	4	23		
$T_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal	67		136	ps
T_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX– signal falling/rising edge			50	ps

TRANSMITTER AC/DC ELECTRICAL CHARACTERISTICS

under recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Z_{diffTX}	Pair differential impedance		85		115	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
RL_{DiffTX}	Differential mode return Loss	f = 150 MHz – 300 MHz	14	24		dB
		f = 300 MHz – 600 MHz	8	21		
		f = 600 MHz – 1.2 GHz	6	21		
		f = 1.2 GHz – 2.4 GHz	6	14		
		f = 2.4 GHz – 3.0 GHz	3	15		
RL_{CMTX}	Common-mode return Loss	f = 150 MHz – 300 MHz	5	31		dB
		f = 300 MHz – 600 MHz	5	23		
		f = 600 MHz – 1.2 GHz	2	13		
		f = 1.2 GHz – 2.4 GHz	1	11		
		f = 2.4 GHz – 3.0 GHz	1	6		
IB_{TX}	Impedance balance	f = 150 MHz – 300 MHz	30	43		dB
		f = 300 MHz – 600 MHz	20	39		
		f = 600 MHz – 1.2 GHz	10	34		
		f = 1.2 GHz – 2.4 GHz	10	28		
		f = 2.4 GHz – 3.0 GHz	4	26		
$Diff_{VppTX}$	Differential output voltage PP	f = 1.5 GHz, PE1/PE2 = 0, See Figure 10	400	510	700	mVppd
$Diff_{VppTX\_DE}$	Differential output voltage PP	f = 1.5 GHz, PE1/PE2 = 1 See Figure 10	600	720	965	
	Output pre-emphasis	at 1.5GHz (when enabled)		2.5		dB
t_{DE}	Pre-emphasis width	At 3Gbps, Also see Figure 10		0.5		UI
VCM_{TX}	Common-mode voltage			1.97		V
VCM_{TX_AC}	AC CM voltage active mode	Maximum amount of AC CM signal at TX		20	50	mVpp
$T_{20\text{-}80TX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. PE2/PE1 = 0	67	90	136	ps
T_{skewTX}	Differential skew	Difference between the SE mid-point of the TX+ signal rising/falling edge, and the SE mid-point of the TX– signal falling/rising edge;		7	20	ps
Jitter (with pre-emphasis disabled at device pin + 2" loadboard trace)						
TJ_{TX}	Total jitter(1)	UI = 333ps, ±K28.5 control character; PE2/PE1 = 0 V		35	63	ps-pp
DJ_{TX}	Deterministic jitter(1)	UI = 333ps, ±K28.5 control character; PE2/PE1 = 0 V		8	33	ps-pp
RJ_{TX}	Random jitter(1)	UI = 333ps, ±K28.7 control character; PE2/PE1 = 0 V		1.9	2.1	ps-rms
Jitter (with pre-emphasis enabled and measured as shown in Figure 6)						
TJ_{TX}	Total jitter(1)	UI = 333ps, ±K28.5 control character; PE2/PE1 = VCC		35	97	ps-pp
DJ_{TX}	Deterministic jitter(1)	UI = 333ps, ±K28.5 control character; PE2/PE1 = VCC		8	67	Uip-p
RJ_{TX}	Random jitter(1)	UI = 333ps, ±K28.7 control character; PE2/PE1 = VCC		1.9	2.1	ps-rms

(1) TJ = (14.1×RJSD + DJ) where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. TJ measurement is at the SATA connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect.

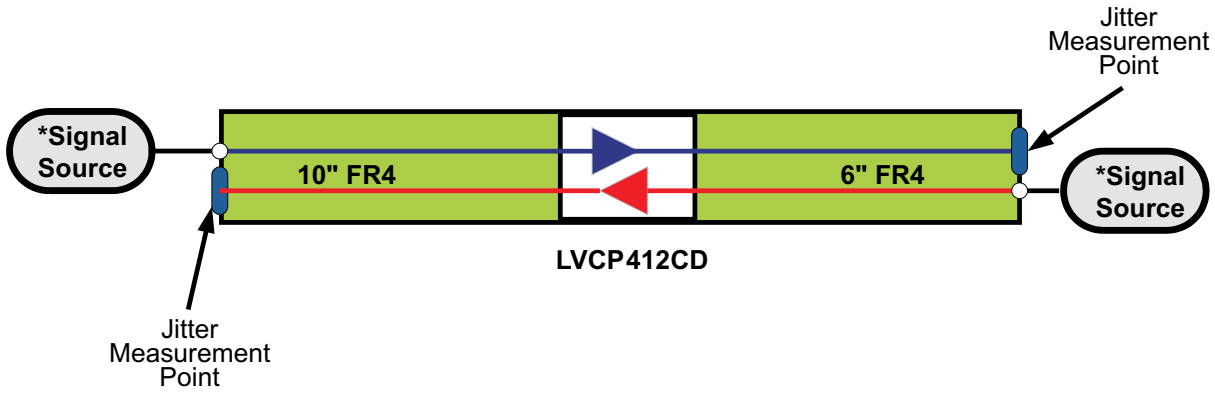
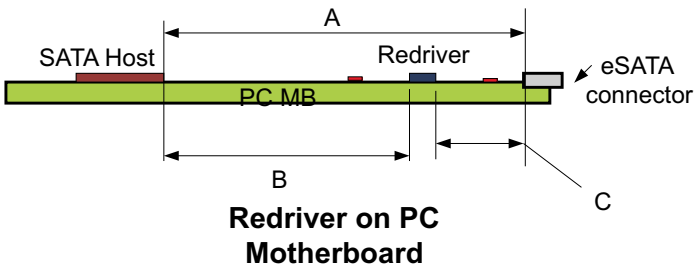


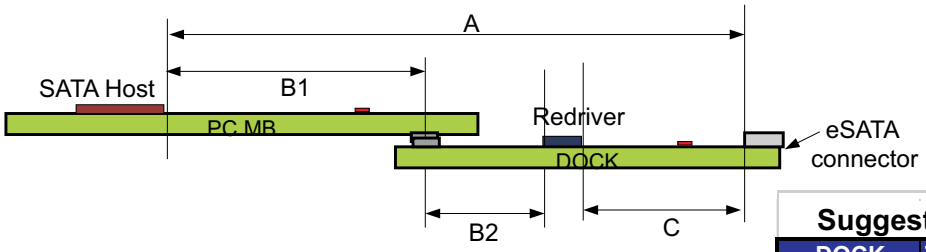
Figure 6. Jitter Measurement Setup



Redriver on PC Motherboard

Suggested Trace Lengths(1)

PC MB	TYP (inch)	MAX (inch)
B	4 to 16	18
C	0.5	2
A	4.5	20



Redriver on Dock Board

Suggested Trace Lengths(1)

DOCK	TYP (inch)	MAX (inch)
B = (B1+B2)	8 to 14	16
C	0.5	2
A	10 to 18	18

(1) Trace lengths are suggested values based on TI lab measurements (taken with output pre-emphasis enabled on both channels) to meet SATA loss and jiter spec.

Actual trace length supported by the LVCP412CD may be more or less than suggested values and will depend on board layout, number of connectors used in the SATA signal path, and SATA host and eSATA connector design.

Figure 7. Suggested Trace Length for LVCP412CD in PC M B and Dock

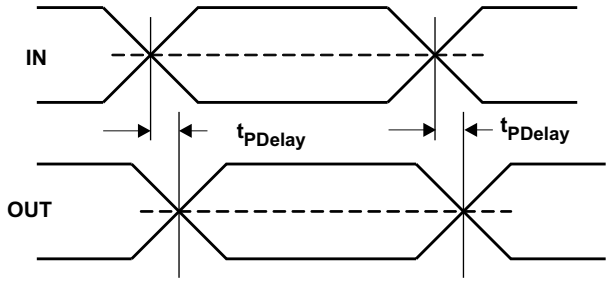


Figure 8. Propagation Delay Timing Diagram

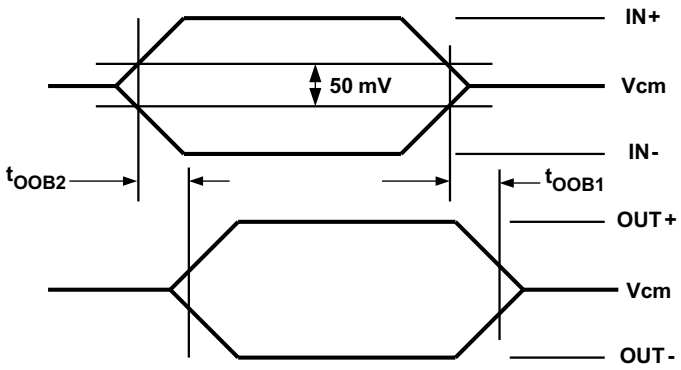


Figure 9. OOB Enter and Exit Timing

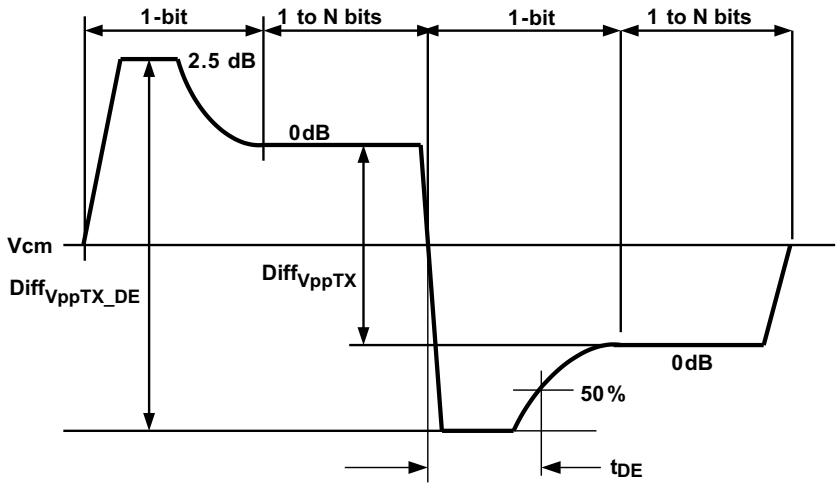


Figure 10. TX Differential Output with 2.5 dB Pre-Emphasis Step

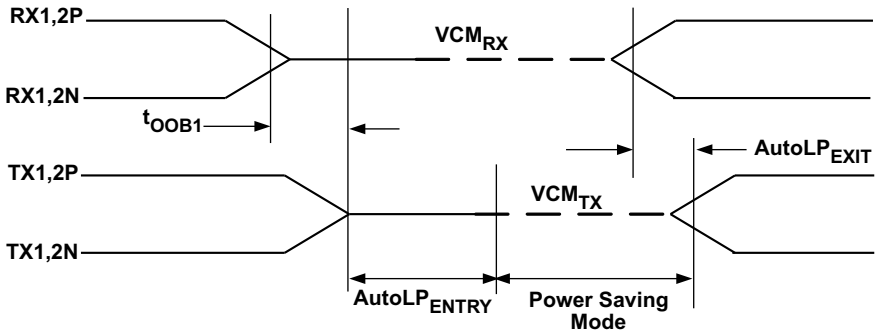


Figure 11. Auto Low Power Mode Timing

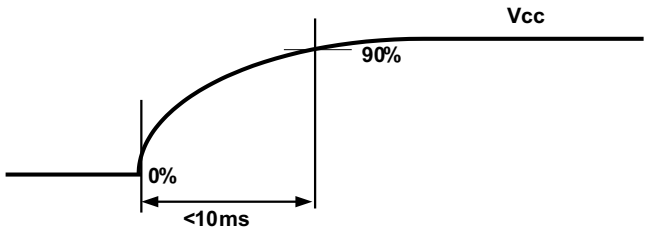


Figure 12. Vcc Waveform Rise Time

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP412CDRTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	412CD	Samples
SN75LVCP412CDRTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	412CD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

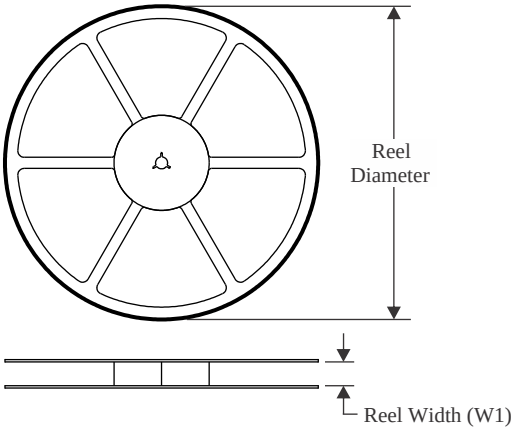
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

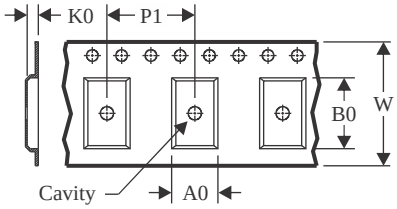
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

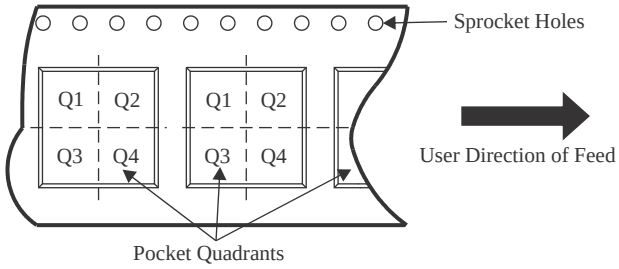


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

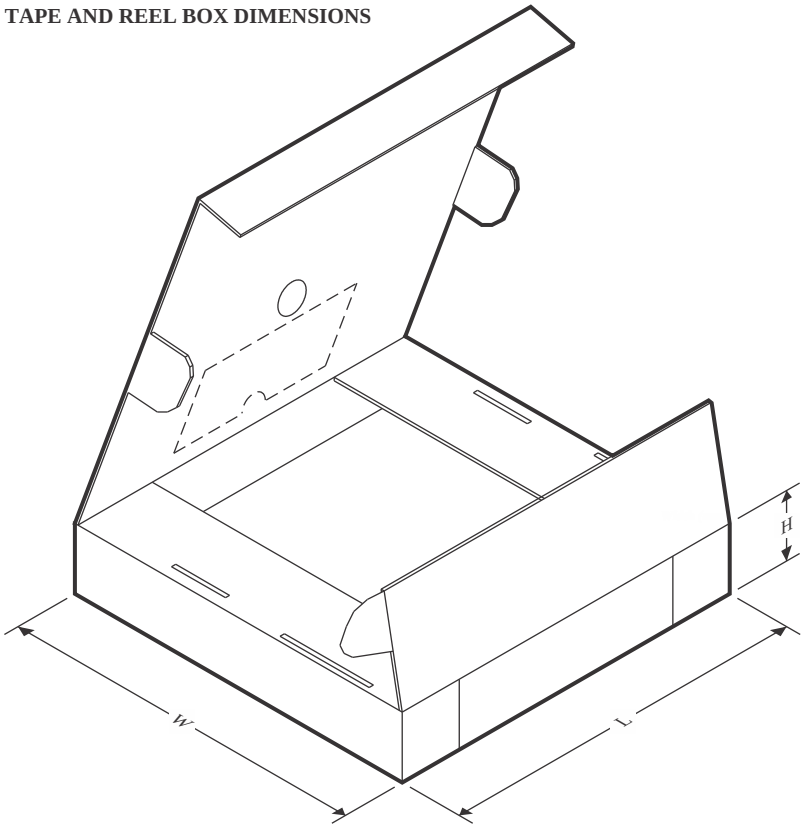
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP412CDRTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LVCP412CDRTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP412CDRTJR	QFN	RTJ	20	3000	346.0	346.0	33.0
SN75LVCP412CDRTJT	QFN	RTJ	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

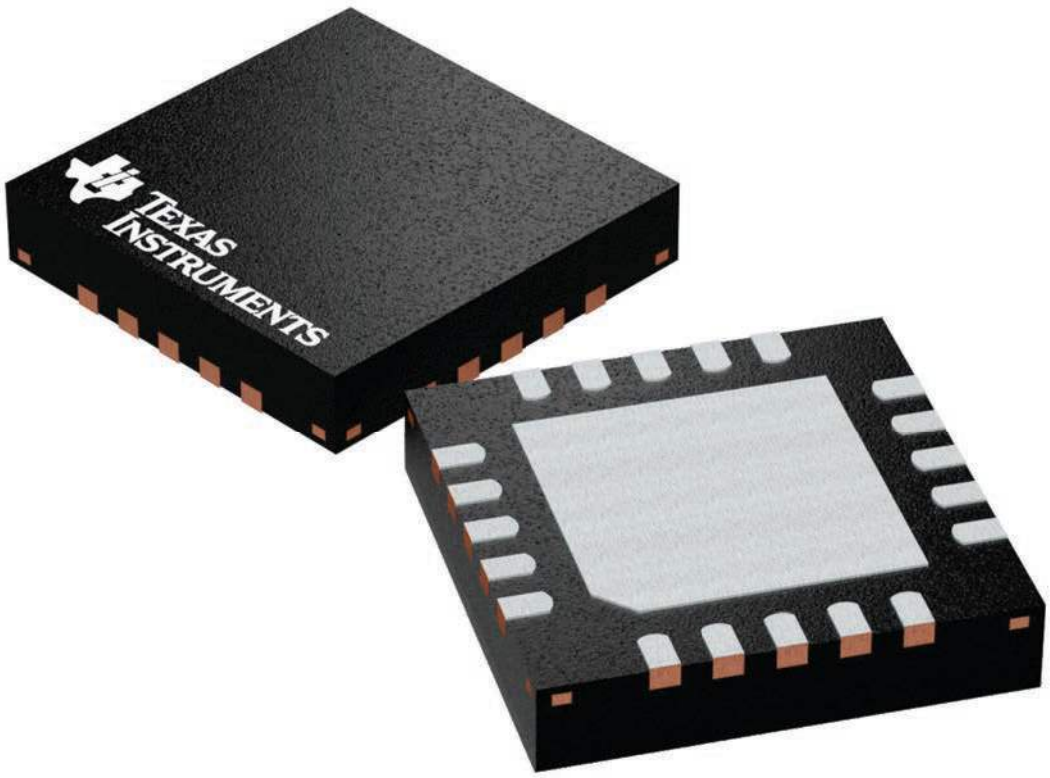
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

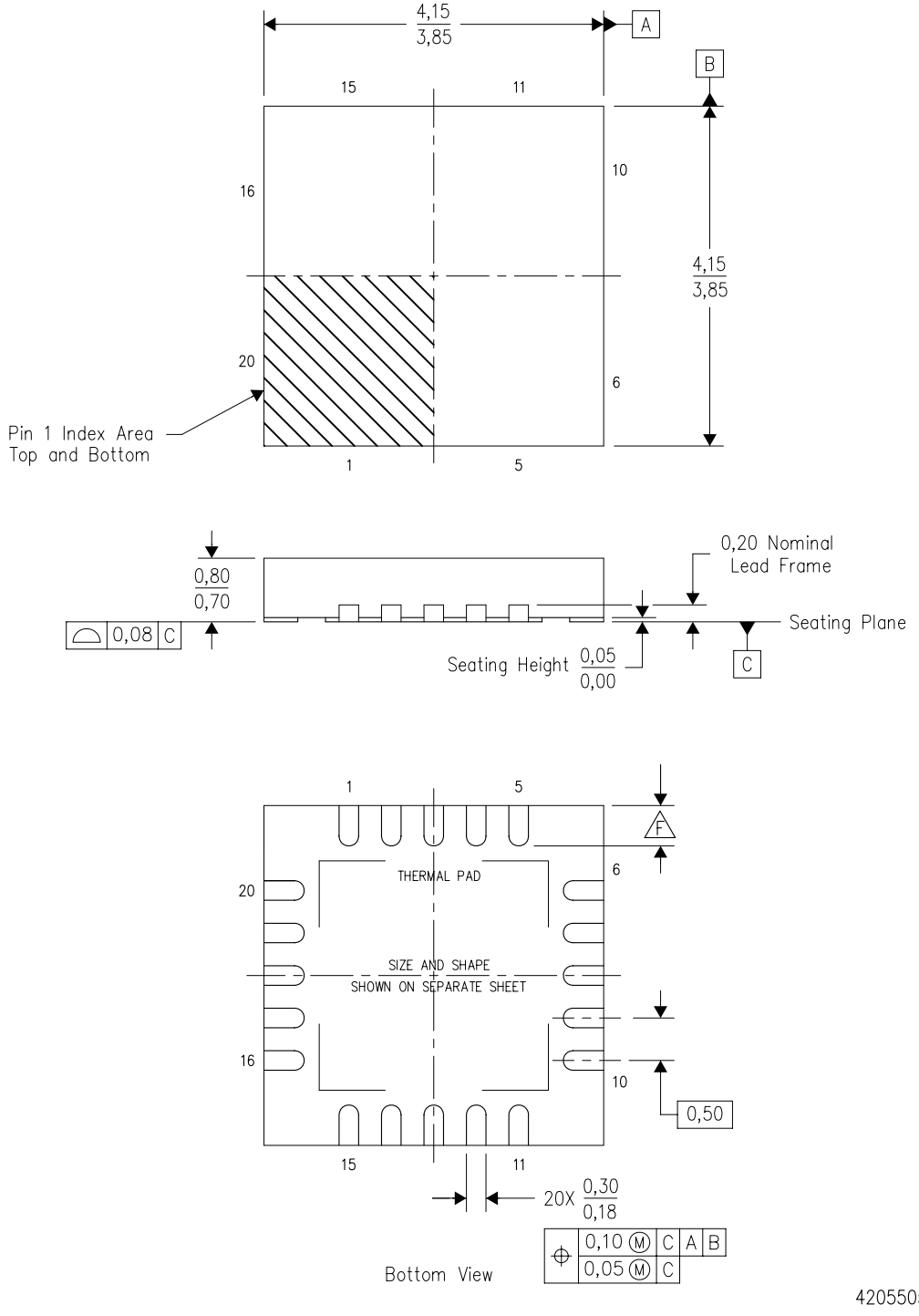
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

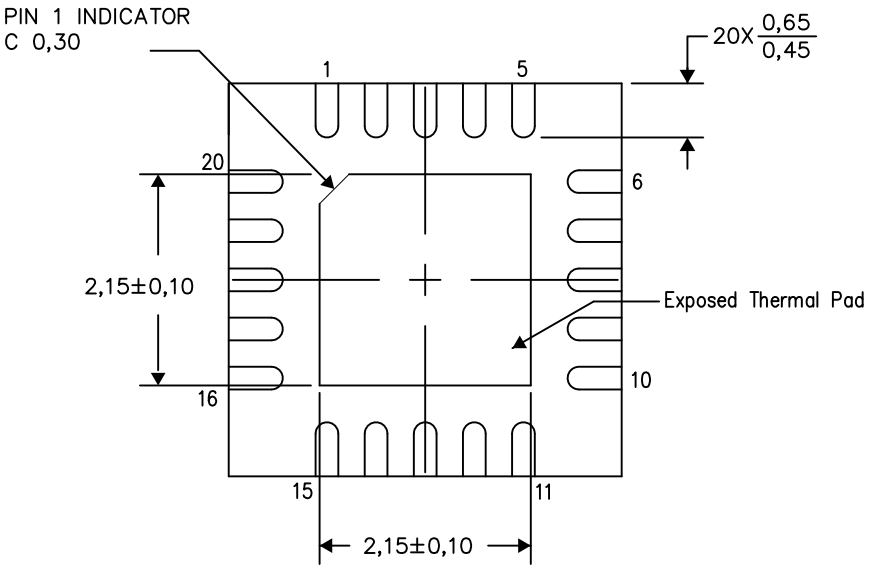
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206256–3/V 05/15

NOTE: All linear dimensions are in millimeters

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