

N-channel 100 V 7.8 m Ω standard level MOSFET with improved SOA in TO220 package

11 August 2014

Product data sheet

1. General description

Standard level N-channel MOSFET with improved SOA in a TO220 package. Part of Nexperia "NextPower Live" portfolio, the PSMN7R8-100PSE is robust enough to withstand substantial in-rush and fault condition currents during turn on/off, whilst offering a low RDS(on) characteristic to keep temperatures down and efficiency up in continued use. Ideal for telecommunication systems based on 48 V backplanes / supply rails.

2. Features and benefits

- Enhanced safe operating area (SOA) for superior protection during linear mode operation
- Low RDS(on) for low conduction losses

3. Applications

- Electronic fuse
- Hot-swap / Soft-start
- Uninterruptible power supplies
- Motor control

4. Quick reference data

Table 1. Qui	ck reference data							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V	
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 10 V; <u>Fig. 2</u>		-	-	83	А	
P _{tot} total power dissipation		T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	294	W	
Static characteristics								
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 12</u>		-	6.7	7.8	mΩ	
Dynamic char	acteristics	·					,	
Q _{GD}	gate-drain charge	V_{GS} = 10 V; I _D = 25 A; V _{DS} = 50 V;		-	41	-	nC	
Q _{G(tot)}	total gate charge	<u>Fig. 14; Fig. 15</u>		-	128	-	nC	

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain- source avalanche energy			-	-	315	mJ

5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain		
3	S	source		G-UF4
mb	D	mounting base; connected to drain		mbb076 S
			TO-220AB (SOT78)	

6. Ordering information

Table 3. Ordering in	Table 3. Ordering information							
Type number	Package							
	Name	Description	Version					
PSMN7R8-100PSE	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78					

7. Marking

Table 4. Marking codes	
Type number	Marking code
PSMN7R8-100PSE	PSMN7R8-100PSE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V

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Symbol	Parameter	Conditions		Min	Мах	Unit
V _{DGR}	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	100	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	294	W
I _D	drain current	V _{GS} = 10 V; T _j = 25 °C; <u>Fig. 2</u>	[1]	-	100	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>		-	83	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^\circ C$; Fig. 3		-	473	Α
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-dra	in diode					
I _S	source current	T _{mb} = 25 °C	[1]	-	100	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^\circ C$		-	473	А
Avalanche	ruggedness		1			
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; unclamped; Fig. 4		-	315	mJ

[1] Continuous current limited by package

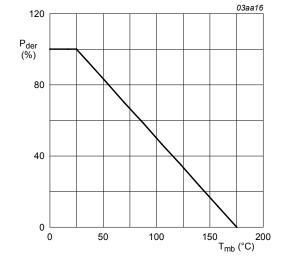


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100 \%$$

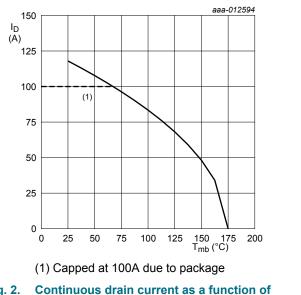
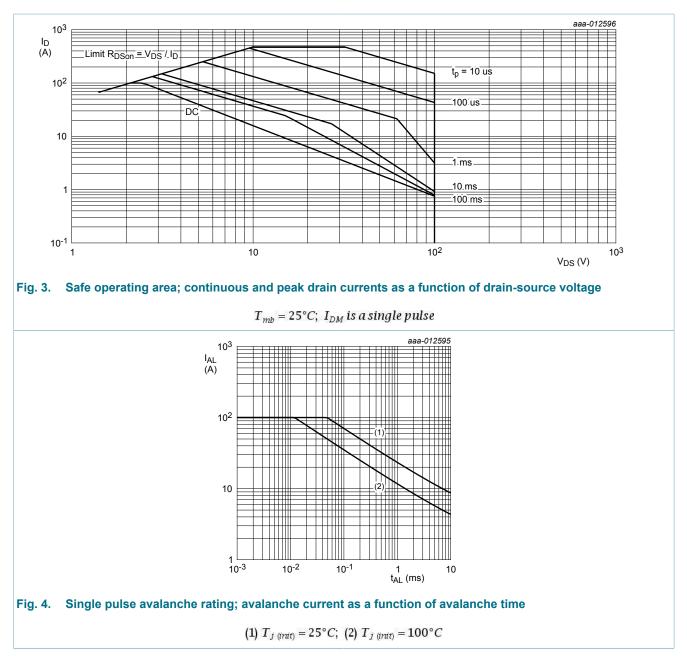


Fig. 2. Continuous drain current as a function of mounting base temperature

 $V_{GS} \ge 10V$

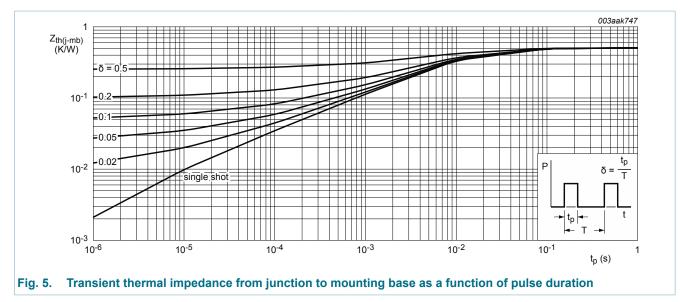




9. Thermal characteristics

Table 6. Thermal characteristics							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. <u>5</u>		-	0.42	0.51	K/W
R _{th(j-a)} thermal resistance from junction to ambient		Minimum footprint; mounted on a printed circuit board		-	50	-	K/W





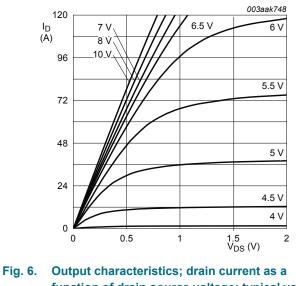
10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
Static chara	acteristics	· · ·				
V _{(BR)DSS}	drain-source	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
	breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 10; Fig. 11	2	3	4	V
V _{GSth} gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 11	1	-	-	V	
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 11	-	-	4.6	V
I _{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	0.1	2	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	-	6.7	7.8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 12; Fig. 13	-	-	14	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 13	-	-	21	mΩ
R _G	gate resistance	f = 1 MHz	0.42	0.83	1.66	Ω

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Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
Dynamic cl	haracteristics					
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14; Fig. 15	-	128	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	110	-	nC
Q _{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V;	-	33	-	nC
Q _{GD}	gate-drain charge	<u>Fig. 14; Fig. 15</u>	-	41	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; <u>Fig. 14; Fig. 15</u>	-	5.3	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; <u>Fig. 16</u>	-	7110	-	pF
C _{oss}	output capacitance		-	450	-	pF
C _{rss}	reverse transfer capacitance		-	310	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V;	-	31	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	48	-	ns
t _{d(off)}	turn-off delay time	-	-	82	-	ns
t _f	fall time		-	47	-	ns
Source-dra	in diode	· · · ·			1	
V _{SD}	source-drain voltage	I_{S} = 25 A; V_{GS} = 0 V; T_{j} = 25 °C; Fig. 17	-	0.8	1.2	V
t _{rr}	reverse recovery time	I_{S} = 25 A; dI _S /dt = -100 A/µs; V _{GS} = 0 V;	-	69	-	ns
Q _r	recovered charge	V _{DS} = 50 V	-	210	-	nC





 $T_j = 25^{\circ}C$

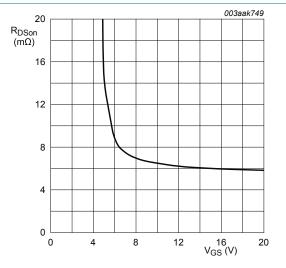
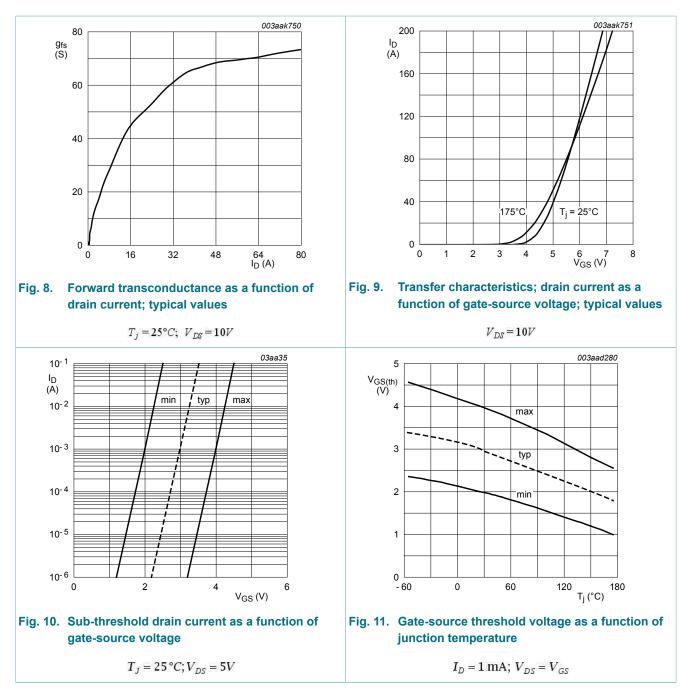


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

 $T_j = 25^{\circ}C; \ I_D = 25A$

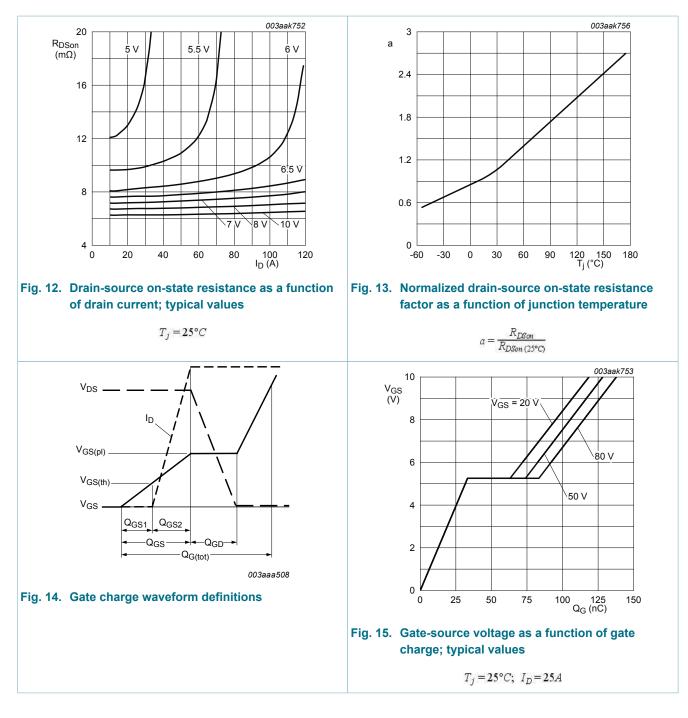
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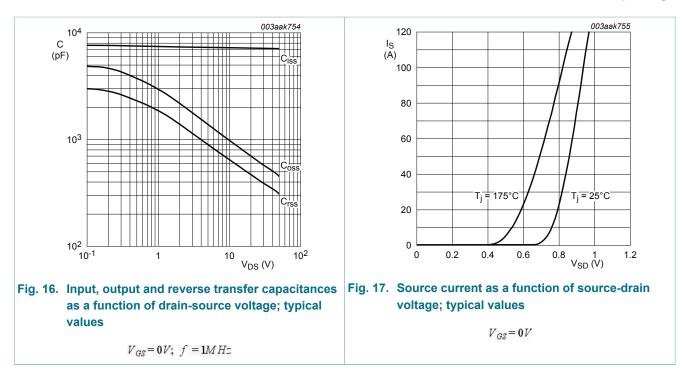
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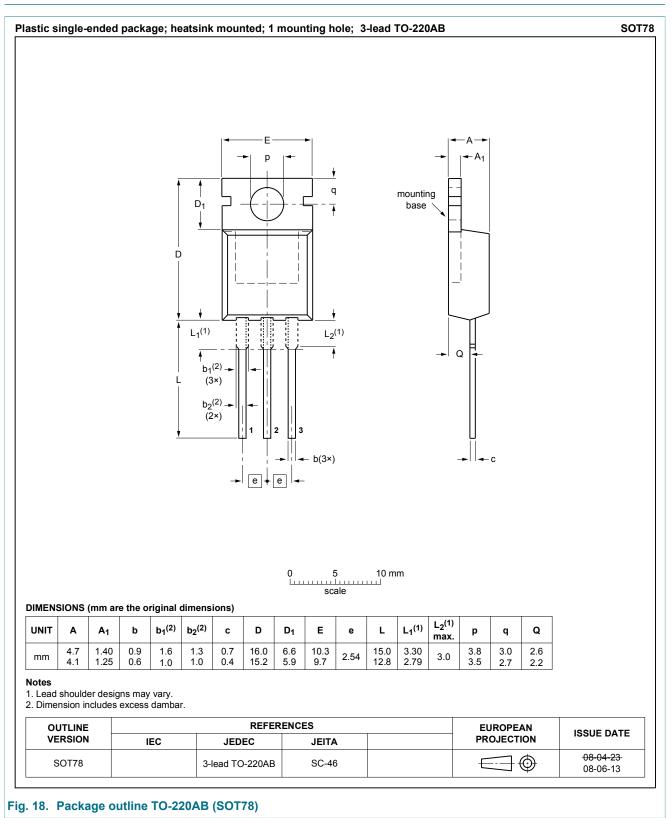
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11. Package outline



PSMN7R8-100PSE

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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