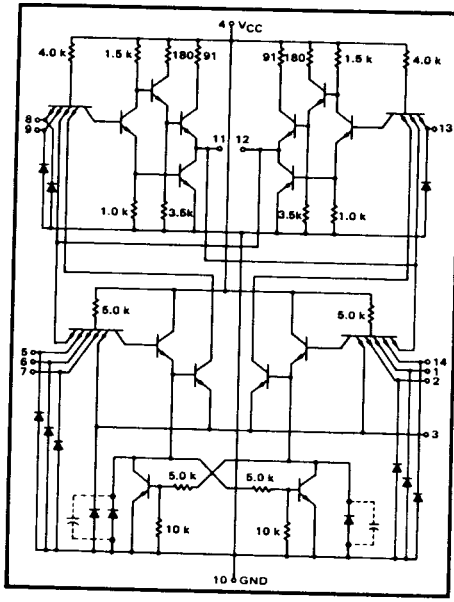
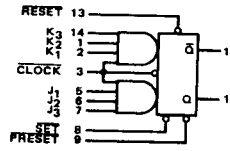
MC515 · MC565
MC415 · MC465



The MC415, MC465, MC515, and MC565 are clocked flip-flops that trigger on the negative edge and perform the J-K logic function. Each flip-flop has an AND input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ are also available.

In normal operation, information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is read into a temporary memory when the clock is in the high state. When the clock goes low, the information is transferred to the bistable section and the Q and $\overline{Q}$ outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct $\overline{SET}$, $\overline{PRESET}$, or $\overline{RESET}$ inputs.

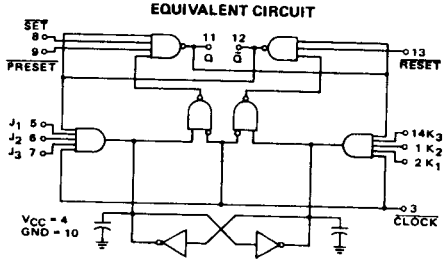
Since each flip-flop is a charge-storage device, there is a restriction on the clock fall time that must be observed.



J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where $J = J_1 \cdot J_2 \cdot J_3$
$K = K_1 \cdot K_2 \cdot K_3$

EQUIVALENT CIRCUIT



Total Power Dissipation = 40 mW typ/pkg
Switching Times:
t_{pd-} = 25 ns typ
t_{pd+} = 13 ns typ

TYPE NO.	INPUT LOADING FACTOR (I_F)				OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	CLOCK	ALL OTHER	CLOCK	ALL OTHER		
MC515 MC565	1.5	1	(−2.0 mA)	(−1.33 mA)	15 MC500 series Gates (20 mA) 7 MC500 series Gates (10 mA)	−55°C to +125°C
MC415 MC465	1.5	1	(−2.5 mA)	(−1.66 mA)	12 MC400 series Gates (20 mA) 6 MC400 series Gates (10 mA)	0°C to +75°C

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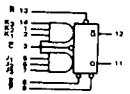
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and K input, plus the **SET**, **PRESET**, and **RESET** inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	@ Test Temperature	TEST CONDITIONS													
		mA						Volts						
		I_{OL}		I_{OH}		I_{in}	$2\ I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}
		Pr*	Std	Pr*	Std									
MC515*, MC565	−55°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
	+25°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
MC415*, MC465	0°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
	+25°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

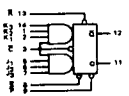
Characteristic	Symbol	Pin Under Test	MC515, MC565 Test Limits						MC415, MC465 Test Limits						Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
			−55°C		+25°C		+125°C		0°C		+25°C		+75°C			I_{OL}	I_{OH}	I_{in}	$2\ I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	Gnd
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max													
Input Forward Current	I_F	1	-	1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	2,3,5,6, 7,9,13,14	-	-	-	4	1,8,10
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	1,2,3,6, 7,8,9,14	-	-	-	↓	5,10,13
		8	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,12
		9	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,8,14	-	-	-		9,10,13
		13	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5, 6,7,9,14	-	-	-		8,10,13
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	1	-	-	-	4	2,3,5,6,7,9,10,12,14
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	5	-	-	-	↓	1,2,3,6,7,8,10,12,14
		8	-		-		-		-		-		-			-	-	-	-	-	-	8	-	-	-		1,2,3,5,6,7,9,10,12,14
		9	-		-		-		-		-		-			-	-	-	-	-	-	9	-	-	-		1,2,3,5,6,7,8,10,12,14
		13	-		-		-		-		-		-			-	-	-	-	-	-	13	-	-	-		1,2,3,5,6,7,9,10,12,14
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	-	-	4	10
		5	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	13	-	-	-	↓	↓
		8	-		-		-		-		-		-			-	-	-	-	-	-	↓	-	-	-		
		9	-		-		-		-		-		-			-	-	-	-	-	-		-	-	-		
		13	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	-	-	-	-	-	-	↓	-	-	-	↓	
Breakdown Voltage	$BV_{in,0}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	8	-	-	-	4	10
		5	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	5	-	-	-	13	-	-	-	↓	↓
		8		-		-		-		-		-		-		-	-	8	-	-	-	↓	-	-	-		
		9		-		-		-		-		-		-		-	-	9	-	-	-		-	-	-		
		13	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	13	-	-	-	↓	-	-	-	↓	
	$BV_{in,1}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	1	-	-	-	-	-	-	-	4	2,3,5,6,7,10,12,14
		5	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	5	-	-	-	-	-	-	-	↓	1,2,3,6,7,8,10,12,14
		8		-		-		-		-		-		-		-	-	8	-	-	-	-	-	-	-		1,2,3,5,6,7,9,10,12,14
		9		-		-		-		-		-		-		-	-	9	-	-	-	-	-	-	-		1,2,3,5,6,7,8,10,12,14
		13	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	-	13	-	-	-	-	-	-	-	↓	1,2,3,5,6,7,9,10,12,14

* Prime Fan-Out

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



@ Test Temperature		I_{OL} mA		I_{OH} mA		I_{in}	$2\ I_{in}$	V_{IL} Volts	V_{IH}	V_R	$V_{th\ 1}$	$V_{th\ 0}$	V_{out}	V_{CC}
		Pr*	Std	Pr*	Std									
MC515°, MC565	−55°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	2.0	1.0	5.5	5.0
	+25°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.7	1.2	5.5	5.0
	+125°C	20	10	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	1.4	0.9	5.5	5.0
MC415°, MC465	0°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.9	1.1	5.5	5.0
	+25°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.8	1.2	5.5	5.0
	+75°C	20	10	-1.2	-0.6	1.0	2.0	0.45	3.0	4.5	1.7	1.1	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC515, MC565 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC415, MC465 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2\ I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\ 1}$	$V_{th\ 0}$	V_{out}	V_{CC}	Gnd
Clock Input Forward Current	I_F	3	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc	-	-	-	-	-	-	1,2,5,6, 7,8,9,13,14	-	-	-	4	3,10
Leakage Current	I_R	3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	-	-	3	-	-	-	4	1,2,5,6,7,10,14
Inverse Beta Current	I_L	3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	13	-	3	-	-	-	4	10
		3	-	150	-	150	-	150	-	150	-	150	-	150	μAdc	-	-	-	-	8	-	3	-	-	-	4	10
Breakdown Voltage	BV_{in} "0"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	13	-	-	-	-	-	4	10
		9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	8	-	-	-	-	-	4	10
	BV_{in} "1"	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	-	3	-	-	-	-	-	-	4	1,2,5,6,7,10,14
Output Output Voltage	V_{out} "0"	12	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	12	-	-	-	-	-	-	13	-	-	4	3,8,10
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	-	-	9	-	-	↓	3,10,13
		11	-	-	-	-	-	-	-	-	-	-	-	-		-	-	-	-	-	-	-	8	-	-		3,10,13
	V_{out} "1"	12	2.5	-	2.4	-	2.7	-	2.5	-	2.4	-	2.5	-	Vdc	-	12	-	-	-	-	-	-	13	-	4	8,10
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	-	-	-	-	9	-	↓	10,13
		11	-	-	-	-	-	-	-	-	-	-	-	-		-	11	-	-	-	-	-	-	8	-		10,13
Leakage Current	I_{OLK}	12	-	2.25	-	2.25	-	2.25	-	2.25	-	2.25	-	2.25	mAdc	-	-	-	-	-	-	-	-	-	12	4	1,2,3,5,6,7,8,9,10,13,14
		11	-	2.25	-	2.25	-	2.25	-	2.25	-	2.25	-	2.25	mAdc	-	-	-	-	-	-	-	-	-	11	4	1,2,3,5,6,7,8,9,10,13,14
Short-Circuit Current	I_{SC}	12	-	-45	-90	-	-	-	-	-	-45	-90	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,12,13,14
		11	-	-45	-90	-	-	-	-	-	-45	-90	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	4	1,2,3,5,6,7,8,9,10,11,13,14
Output Voltage	V_{OL}	12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	12	-	-	-	-	13	-	-	-	-	4	3,8,10
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	9	-	-	-	-	↓	3,10,13
		11	-	-	-	-	-	-	-	-	-	-	-	-		-	-	-	-	-	8	-	-	-	-		3,10,13
	V_{OH}	12	2.80	-	3.20	-	3.35	-	3.00	-	3.10	-	3.15	-	Vdc	-	12	-	-	13	-	-	-	-	-	4	8,10
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	9	-	-	-	-	-	↓	10,13
		11	-	-	-	-	-	-	-	-	-	-	-	-		-	11	-	-	8	-	-	-	-	-		10,13
Power Requirements (Total Device) Power Supply Drain	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	4	3,10,13
	I_{PD}	4	-	12	-	12	-	12	-	14	-	14	-	14	mAdc	-	-	-	-	-	-	-	-	-	-	4	3,8,10

* Prime Fan-Out.

OPERATING CHARACTERISTICS

Clock fall time ≤ 150 ns.

Triggers on clock pulse widths ≥ 20ns.

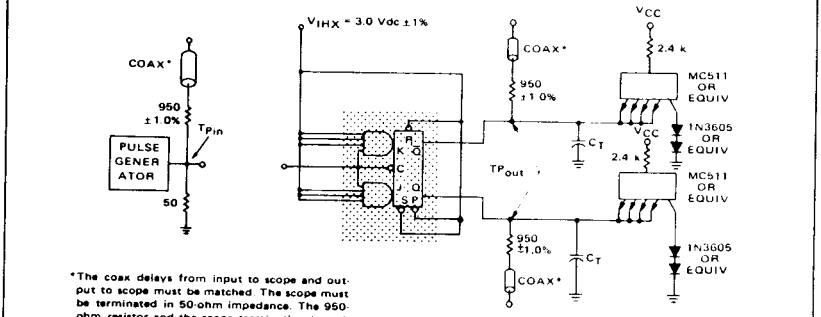
Provides direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. The application of a "0" state to 8 or 9, sets Q high; "0" state to 13, resets Q low. The clock must be in the low state when these functions are performed.

Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 300 ns to recognize a "1" state to "0" state information change on the J and K terminals. The flip-flop will require typically 10 ns to recognize a "0" state to "1" state change.

Negative edge triggering – When the clock goes from the high state to the low state, the information in the temporary storage section is transferred and the Q and $\overline{Q}$ outputs will respond accordingly. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to 2.0 to 5.0 Vdc. $\overline{PRESET}$ and $\overline{SET}$ are tied to $\overline{Q}$; $\overline{RESET}$ is tied to Q.

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

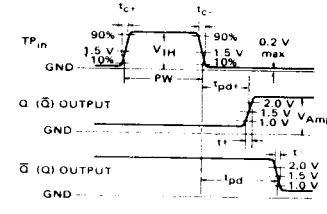
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{pd+}	V		20	ns
Delay Time On	t_{pd-}	V		40	ns
Rise Time	t_{+}	V		8.0	ns
Fall Time	t_{-}	V		5.0	ns
Amplitude	V_{Amp}	V	3.2		Volt

WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	20 MHz max	W
Pulse Width	PW	20 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_{c-}	150 ns max	Z

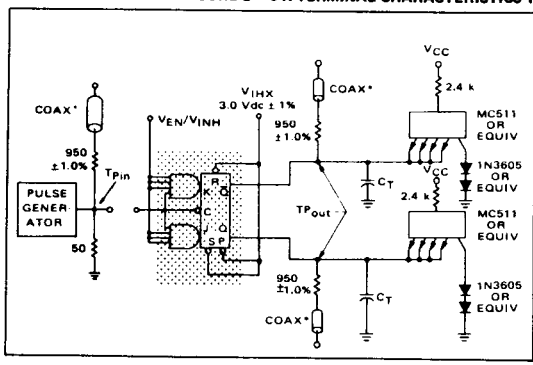
VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	W	V	X	Y	Z	UNIT
PRF	20	5.0	5.0	5.0	1.0	MHz
PW	20	100	20	100	200	ns
t_{c+}	≤ 10	≤ 10	≤ 10	≤ 10	≤ 50	ns
t_{c-}	≤ 10	≤ 10	≤ 10	≤ 10	150	ns
V_{IH}	3.5	3.5	3.5	1.8	3.5	Volt

FIGURE 2 – J-K TERMINAL CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

Enable Mode Test:
The device under test shall toggle when V_{EN} = 1.8 Vdc ± 1.0% is applied.

Inhibit Mode Test:
The device under test shall NOT toggle when V_{INH} = 1.2 Vdc ± 1.0% is applied.

INPUT VOLTAGE WAVEFORMS AND DEFINITIONS

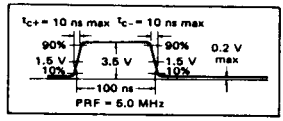
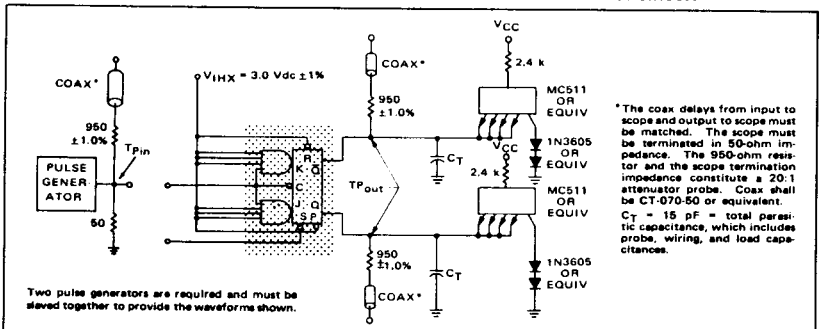


FIGURE 3 – SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



Two pulse generators are required and must be slaved together to provide the waveforms shown.

*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

TEST PARAMETERS

SYMBOL	VALUE	UNIT
t_{Post}	120	ns min
t_{sd-}	40	ns max
t_{sd+}	20	ns max

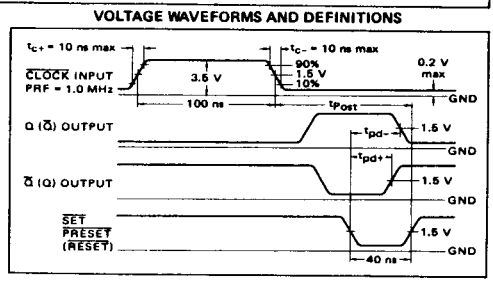
t_{Post} = Post Time

When t_{Post} is 120 ns, SET, PRESET or RESET pulses must actuate the device.

SET, PRESET, and RESET pulse cannot return to the high state before the required post time.

Connections shown for measuring times related to SET terminal only. To measure times at PRESET terminal apply input pulse to Pin 9 in place of Pin 8. To measure times at RESET terminals, apply the input pulse to Pin 13.

VOLTAGE WAVEFORMS AND DEFINITIONS



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