Triple Channel Synchronous Step-Down Switcher with Integrated FET

Advanced Datasheet

IDTP9120

Features

- **Input Voltage Range: 2.7V to 5.5V**
- **Three step-down converters with integrated FETs**
  - **Buck1: 2A**
  - **Buck2: 2A**
  - **Buck3: 3A**
- **Buck 3 to operate in Buck or Switch mode**
- **Factory Programmable Output Voltage: 0.8 - 3.4V**
- **Automatic PFM/PWM or forced PWM mode**
- **Switching frequency 2MHz**
- **Optional Programmable Sequence Mode**
- **Power Good and/or Power On Reset Output**
- **-40°C to +85°C operating temperature range**
- **Package: QFN 24-ld 4 x 4mm x 0.8mm (NBG24)**

Applications

Point of Load Regulation in a variety of low power applications:

- **Solid State Disk Drive (SSD) Power Management**
- **Low Power USB powered applications**
- **Set Top Box / TV Power Supply**
- **Portable Gaming**

Description

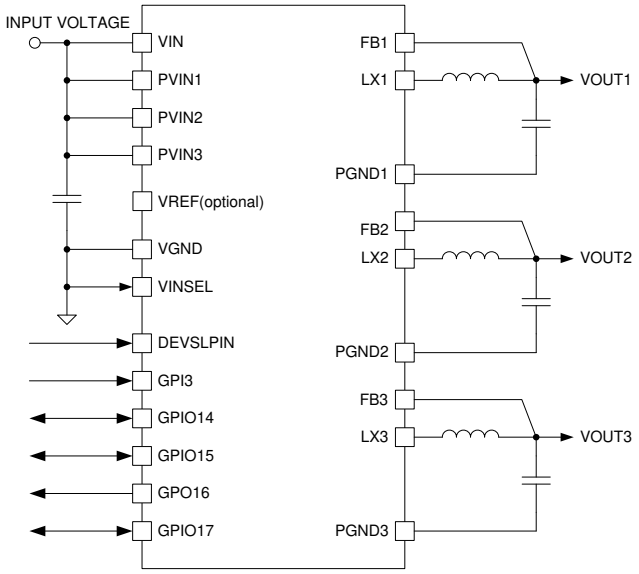
IDTP9120 is a fully integrated power management IC designed to provide three programmable voltage rails from a single 5V or 3.3V input rail with high efficiency and low quiescent currents in sleep mode or no-load condition.

The device offers selectable direct buck enable inputs or programmable sequencing with power good and power on reset generation.

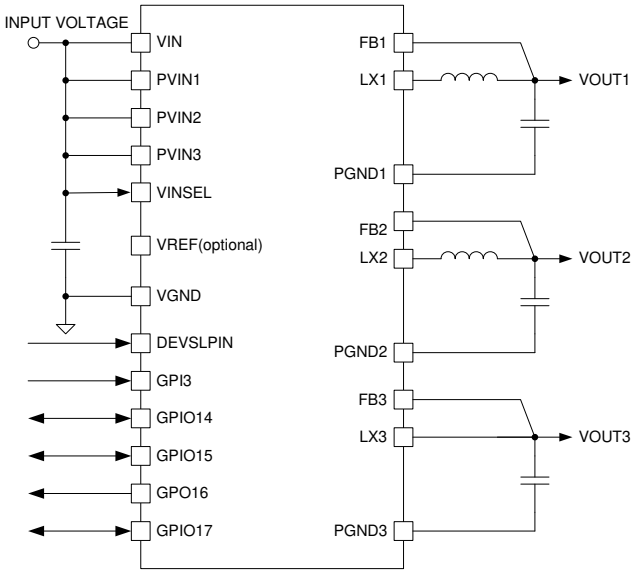
To support low power operation, the IDTP9120 supports both sleep and standby modes.

The IDTP9120 is available in a 4mm x 4mm, 24-ld, QFN package and is guaranteed to operate over the ambient temperature range -40°C to +85°C.

Simplified Application Diagram



IDTP9120 with VINSEL (pin 4) in Buck Configuration for VOUT3

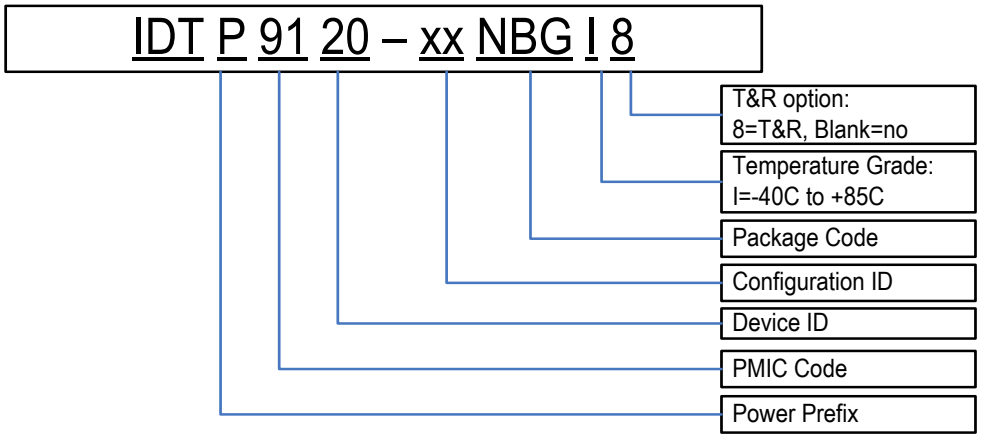


IDTP9120 with VINSEL (pin 4) in Switch Configuration for VOUT3

ORDERING GUIDE

Table 1 – Ordering Summary

PART NUMBER	MARKING	PACKAGE[1]	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9120-00NBGI	P9120-00NBGI	QFN-24 4x4x0.75mm 24-ld	-40°C to +85°C	Tray	490
P9120-xxNBGI	P9120-xxNBGI	QFN-24 4x4x0.75mm 24-ld	-40°C to +85°C	Tray	490
P9120-xxNBGI8	P9120-xxNBGI	QFN-24 4x4x0.75mm 24-ld	-40°C to +85°C	Tape and Reel	2,500



Additional Ordering Information:

The IDTP9120 will be sampled in "-00" configuration, with all user configurable OTP registers at default state (0). Once a final customer configuration has been defined, a configuration specific "-xx" ID will be assigned and used for order and marking.

ABSOLUTE MAXIMUM RATINGS

Stresses above the ratings listed below can cause permanent damage to the IDTP9120. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2 – Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3 to PGND	Regulator input voltage	-0.3	6.0	V
VIN to GND	Supply for device	-0.3	6.0	V
LX1, LX2, LX3	Regulator Switch Nodes	-0.3	6.0	V
FB1, FB2, FB3	Regulator Feedback pins	-0.3	3.6	V
All other pins		-0.3	6.0	V
T_J	Operating Junction Temperature		125	°C
T_S	Storage Temperature		150	°C
T_{SOLDER}	Soldering Temperature (10 seconds)		260	°C

[1] See Package Information (Page 24) for additional details.

Table 3- Package Thermal Resistivity

SYMBOL	DESCRIPTION	CONDITIONS	Value	Units
θ_{JA}	Thermal Resistance (QFN-24)	Junction to Ambient	40	°C/W
Ψ_{JB}	Thermal Characterization Parameter (QFN-24)	Junction to Board	23	°C/W
P_D	Maximum Package Power Dissipation		2.5	W
ESD Rating	(HBM) Human Body Model (all pins except 20, 21)	±2000V		
	(HBM) Human Body Model (only pins 20, 21)	± 500V		
	(CDM) Charged Device Model (all pins)	± 500V		

Per JEDEC spec, the QFN-24 package is rated at MSL3. This thermal rating was calculated based on a JEDEC standard 4-layer board with dimensions 3in x 4.5in in still air conditions. Actual thermal resistance will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables. For the QFN-24 package, the 2.8mm X 2.8mm EP is connected to ground plane with a matrix of 3x3 PCB thermal VIAs plated through from Top to Bottom layers. Actual thermal resistance will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables.

ELECTRICAL CHARACTERISTICS

Table 4 – General Electrical Characteristics

Typical values at 25°C, unless noted. $V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = Vin = 5V$. $C_{O(BUCK1)} = C_{O(BUCK2)} = 10\mu F$, $C_{O(BUCK3)} = 20\mu F$, L1=L2=L3 =1.0µH.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VIN}	Input voltage range		2.7		5.5	V
	UVLO threshold, VIN rising	VINSEL>1V, Buck3 in Switch (3.3V) Mode	2.95	3	3.05	V
	UVLO threshold, VIN falling		2.65	2.7	2.75	V
	UVLO threshold, VIN rising	VINSEL=0V, Buck3 in Buck (5V) Mode	4.35	4.4	4.45	V
	UVLO threshold, VIN falling		3.95	4.0	4.05	V
$I_{Q(VIN)}$	VIN quiescent current	Device in sleep mode (Vref disable, Devslpin floating).		<1		µA
		Device in active mode, all Bucks = OFF		108		µA
V_{IL}	Low Level Input Voltage	All inputs	0.65	0.85		V
V_{IH}	High Level Input Voltage	All inputs		1.25	1.45	V
I_{PD}	Pull Down Current	GPIO14,15,17, and GPI3		1		µA
I_{PU}	Pull Up Current	DEVSLPIN @ VIN=5V	5	8	10	µA
R_{PU}	Pull Up Resistor	Selectable for GPIO14,15,17, GPO16 and GPI3		50		kΩ
T_{SD}	Thermal Shutdown			135		°C
V_{PG}	PG Detection Threshold	% of selected output voltage in Buck Mode, % of V_{PVIN3} in Switch mode		10		%
I_{OD}	Max Drive Output	In push-pull configuration, V_{OL}=0.4V, $V_{FBx} \geq 1.8V$	4			mA
		In open drain configuration, V_{OL}=0.4V	12			mA
V_{REF}	Reference Voltage Output Voltage			$V_{FB(BUCK1)}/2$		V
C_{VREF}	Output Capacitor V_{REF}			0.1		µF
I_{VREF}	Reference Voltage Output Current				1.0	mA

ELECTRICAL CHARACTERISTICS

Table 5 – Buck1 Electrical Characteristics

$V_{O(BUCK1)}$ = 1.8V.

Typical values at 25°C, unless noted. $V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = Vin = 5V$. $C_{O(BUCK1)} = C_{O(BUCK2)} = 10\mu F$, $C_{O(BUCK3)} = 20\mu F$, L1=L2=L3 =1.0µH.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVIN1}	Input voltage range		2.7		5.5	V
$V_{O(BUCK1)}$	Output voltage range		0.8		3.4	V
	Regulation voltage accuracy		-2		2	%
	Line Regulation	V_{PVIN1} = 3.0V to 5V		0.01	0.04	%/V
	Load Regulation	I_{OUT1} = 0.2A to 2A, PWM mode			0.5	mV/A
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM mode		15		mV
$I_{Q(BUCK1)}$	Quiescent Current Adder	Enabled, No load, PFM mode		25		µA
$I_{OP(BUCK1)}$	Continuous operating DC current	T_J < 115°C			1.8	A
$I_{LIM(BUCK1)}$	Peak Inductor Current		2	2.5		A
$R_{(on)}$	High side switch			110	153	mΩ
	Low side switch			56	78	mΩ
$R_{DIS(BUCK1)}$	Output discharge resistance		500	650	900	Ω
$f_{SW(BUCK1)}$	Switching frequency	PWM mode	1.89	2	2.1	MHz
$T_{ssr(BUCK1)}$	Soft-start ramp rate		4	8	12	mV/µs
I_{FB1}	FB1 input bias current			6	8	µA
$C_{O(BUCK1)}$	Output Capacitor			10		µF
$L_{O(BUCK1)}$	Output Inductor			1		µH

ELECTRICAL CHARACTERISTICS

Table 6 – Buck2 Electrical Characteristics

$V_{O(BUCK2)}$ = 1.2V.

Typical values at 25°C, unless noted. V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = Vin= 5V. $C_{O(BUCK1)}$ = $C_{O(BUCK2)}$ = 10µF, $C_{O(BUCK3)}$ = 20µF, L1=L2=L3 =1.0µH.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVIN2}	Input voltage range		2.7		5.5	V
$V_{O(BUCK2)}$	Output voltage range		0.8		3.4	V
	Regulation voltage accuracy		-2		2	%
	Line Regulation	V_{PVIN2} = 3.0V to 5V		0.01	0.04	%/V
	Load Regulation	I_{OUT2} = 0.2A to 2A, PWM mode			0.5	mV/A
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{offset}$	PFM mode		15		mV
$I_{Q(BUCK2)}$	Quiescent Current Adder	Enabled, No load, PFM mode		25		µA
$I_{OP(BUCK2)}$	Continuous operating DC current	T_J < 115°C			1.8	A
$I_{LIM(BUCK2)}$	Peak Inductor Current		2	2.5		A
$R_{(on)}$	High side switch			110	153	mΩ
	Low side switch			56	78	mΩ
$R_{DIS(BUCK2)}$	Output discharge resistance		500	650	900	Ω
$f_{SW(BUCK2)}$	Switching frequency	PWM mode	1.89	2	2.1	MHz
$T_{ssr(BUCK2)}$	Soft-start ramp rate		4	8	12	mV/µs
I_{FB2}	FB2 input bias current			6	8	µA
$C_{O(BUCK2)}$	Output Capacitor			10		µF
$L_{O(BUCK2)}$	Output Inductor			1		µH

ELECTRICAL CHARACTERISTICS

Table 7– Buck3 –Electrical Characteristics

$V_{O(BUCK3)}$ = 3.3V

Typical values at 25°C, unless noted. V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = Vin= 5V. $C_{O(BUCK1)}$ = $C_{O(BUCK2)}$ = 10µF, $C_{O(BUCK3)}$ = 20µF, L1=L2=L3 =1.0µH.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
In Buck Mode (VINSEL=LOW)						
V_{PVIN3}	Input voltage range		2.7		5.5	V
$V_{O(BUCK3)}$	Output voltage range		0.8		3.4	V
	Regulation voltage accuracy		-2		2	%
	Line Regulation	V_{PVIN3} = 3.6V to 5V		0.01	0.15	%/V
	Load Regulation	I_{OUT3} = 0.2A to 2.4A, PWM mode		0.4	0.5	mV/A
	Offset voltage in PFM mode $V_{O(PFM)}$ = $V_{O(PWM)}$ + V_{offset}	PFM mode		15		mV
$I_{Q(BUCK3)}$	Quiescent Current Adder	Enabled, No load, PFM mode		28		µA
$I_{OP(BUCK3)}$	Continuous operating DC current	T_J < 115°C			2.3	A
$I_{LIM(BUCK3)}$	Peak Inductor Current		2.6	3		A
$R_{(on)}$	High side switch			64	93	mΩ
	Low side switch			45	61	mΩ
$R_{DIS(BUCK3)}$	Output discharge resistance		500	650	900	Ω
$f_{SW(BUCK3)}$	Switching frequency	PWM mode	1.89	2	2.1	MHz
$T_{ssr(BUCK3)}$	Soft-start ramp rate			8	12	mV/µs
I_{FB3}	FB3 input bias current			9	11	µA
$C_{O(BUCK3)}$	Output Capacitor			20		µF
$L_{O(BUCK3)}$	Output Inductor			1		µH
In Switch Mode (VINSEL=HIGH), $C_{O(BUCK3)}$ = 10µF, V_{PVIN3} = 3.3V						
V_{PVIN3}	Input voltage range		2.7		3.6	V
$I_{SHDN(BUCK3)}$	Shutdown current			1		µA
$I_{Q(BUCK3)}$	Quiescent Current	No load		10		µA
$I_{OP(BUCK3)}$	Continuous operating DC current	T_J < 115°C			2.4	A
$I_{LIM(BUCK3)}$	Current Limitation		2.8	3		A
$R_{(on)}$	High side switch			64	93	mΩ
$R_{DIS(BUCK3)}$	Output discharge resistance		300		800	Ω
$T_{ssr(BUCK3)}$	Soft-start ramp rate			16		mV/µs
$C_{O(BUCK3)}$	Output Capacitor			2		µF

PIN CONFIGURATION AND DESCRIPTION

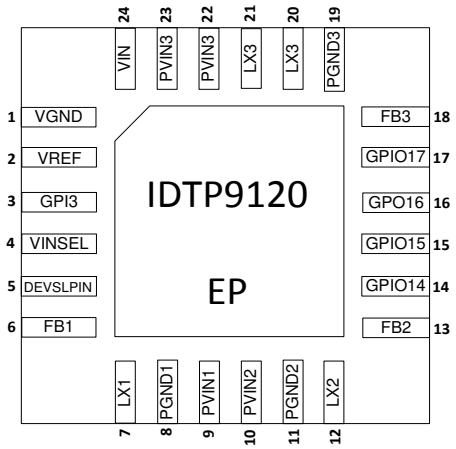


Figure 1, Device Pinout (Top View), 0.5mm pitch QFN-24, 4x4x0.75mm

Table 8 – Pin Functions by Pin Number

#	Label	Type	Description
1	VGND	GND	Device ground connection
2	VREF	A	Reference output [VREF=VOUT(Buck1)/2]
3	GPI3	DI	General Purpose Input (see Modes of Operation, page 9)
4	VINSEL	DI	Logic input to select function of Channel 3 (Logic Low = Buck operation, High = Switch operation) and UVLO thresholds.
5	DEVSLPIN	DI	Logic input to activate sleep mode (Logic Low = Normal operation, Floating = Sleep operation).
6	FB1	A	Feedback connection Buck 1
7	LX1	A	Inductor connection Buck 1
8	PGND1	GND	Power ground Buck 1
9	PVIN1	PWR	Power supply input Buck 1
10	PVIN2	PWR	Power supply input Buck 2
11	PGND2	GND	Power ground Buck 2
12	LX2	A	Inductor connection Buck 2
13	FB2	A	Feedback connection Buck 2
14	GPIO14	DIO	General Purpose Input / Output (see Modes of Operation, page 9)
15	GPIO15	DIO	General Purpose Input / Output (see Modes of Operation, page 9)
16	GPO16	DO	General Purpose Output (see Modes of Operation, page 9)
17	GPIO17	DIO	General Purpose Input / Output (see Modes of Operation, page 9)
18	FB3	A	Feedback connection Buck 3 (Buck Mode) or Output (Switch Mode)
19	PGND3	GND	Power ground Buck 3
20	LX3	A	Inductor connection Buck 3 (Buck Mode) or Output (Switch Mode)
21	LX3	A	
22	PVIN3	PWR	Power supply input Buck 3
23	PVIN3	PWR	
24	VIN	PWR	Device supply input
EP	EP	GND	Exposed pad, connect to heat sink ground plane

FUNCTIONAL DESCRIPTION:

Overview

The IDTP9120 support several modes to control the 3 Buck regulators and to generate status information like PG (power good) or POR (power on reset).

Various device features can be configured during production using one time programmable fuse memory (OTP). During evaluation, the options can be evaluated using the IDTP9120 Evaluation Kit (IDTP9120-EVAL).

The IDTP9120 OTP memory is organized into four fuse banks with 34 bits each. Bank0 and 1 are used for IDT internal trimming and calibration. Bank2 and 3 are used for customer specific device configuration.

Modes of Operation

Device Power States

Device operates in three basic power states controlled by the DEVSLPIN pin and one optional state (standby) when in Mode 3.

Regulator Control Options (Mode 0..3)

The IDTP9120 supports four different control options for the Buck regulator. The functionality of GPI3, GPIO14,15,17 and GPO16 is different for each of the options. (MODE[1:0] = OTP Bank3[1:0])

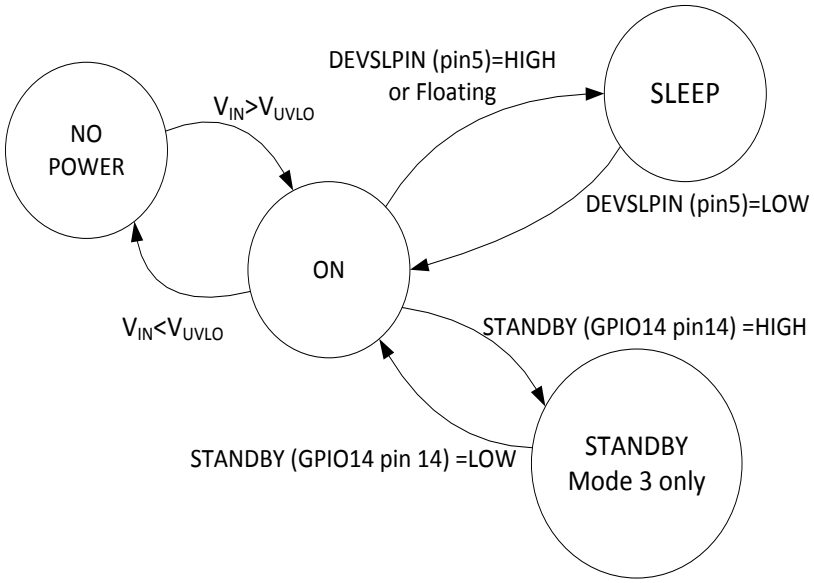


Figure 2. Device Power States

Table 9 – Buck Control Options

MODE[1:0]	DESCRIPTION	GPI3	GPIO14	GPIO15	GPO16	GPIO17
0 (Default)	Buck regulators controlled by individual enable pins (EN1, EN2, EN3)	NC	EN1	EN2	PORB	EN3
1	Special Sequencing Option.	NC	COLDBOOT	SOCREADY	PORB	DEVSLPRLY
2	Buck regulators controlled by master enable pin (MEN) w/ sequence	MEN	PORB	PG1	PG2	PG3
3	Buck regulators controlled by master enable pin (MEN) w/ sequence and standby mode support	MEN	STANDBY	PG1	PG2	PG3/PORB

Mode0 – Individual Buck control

With IDTP9120 configured for mode0, all three regulators are individually controlled via ENx input pin. The PORB output can be configured to indicate various power up conditions.

Mode1 – Special Sequencing Option

With IDTP9120 configured for mode1, a specific state machine will control the regulators. The sequence has been implemented for specific controllers used in solid state disk (SSD) applications. The sequencing details are documented in the following state diagrams. For further details on the "Special Sequencing Option", please contact IDT.

Device Start Up:

(1) Input supply ramps-up.
(2) DEVSLPIN is pulled low, device starts-up.
(3) Device started-up, VOUT2 starts-up.
(4) VOUT2 ramped-up, VOUT3 starts-up.
(5) VOUT3 ramped-up, VOUT1 starts-up.
(6) PORB de-asserts high.
(7) SOCREADY (from controller) asserts high.

Note: Buck Voltages and Sequence shown is default and can be re-programmed.

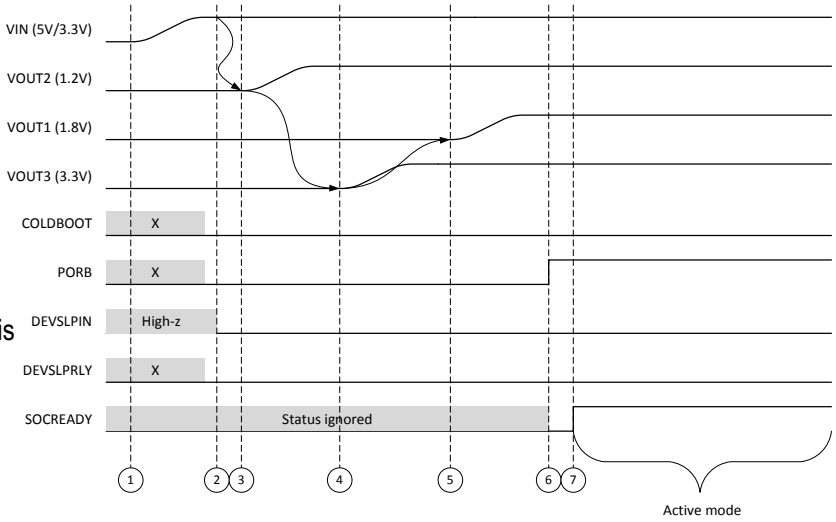


Figure 3, Mode1 - Device Start Up

Device enters DevSlp:

(1) DEVSLPIN asserts high.
(2) If SOCREADY is high, DEVSLPRLY is asserted high. Otherwise DEVSLPIN is ignored, DEVSLPRLY remains low.
(3) Device is waiting for SOCREADY to de-assert low. SOCREADY is expected to go low within 500ms.
(4) PORB is asserted low.
(5) DEVSLPRLY de-asserts low.
(6) VOUT2 shuts down.
(7) VOUT2 ramped-down. VOUT3 shuts down.
(8) VOUT1 shuts down.

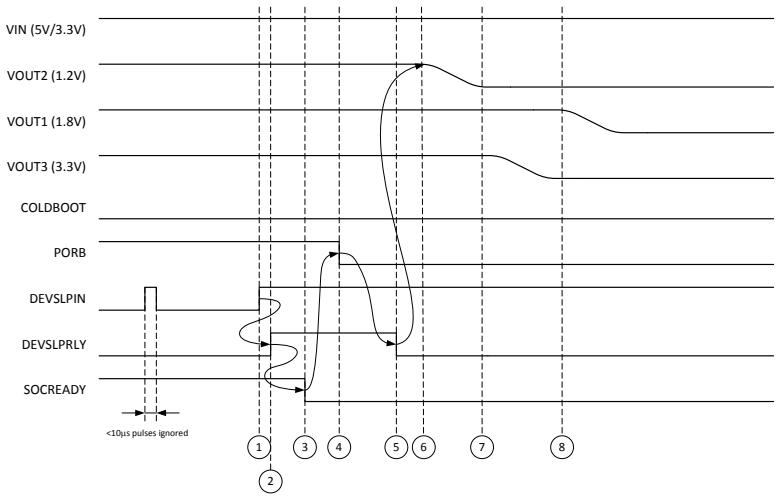


Figure 4, Mode1 - Device enters DevSlp

Device exits DevSlp:

(1) DEVSLPIN de-asserts low.
(2) COLDBOOT de-asserts high, VOUT2 starts-up.
(3) VOUT2 ramped-up, VOUT3 starts-up.
(4) VOUT3 ramped-up, VOUT1 starts-up.
(5) VOUT1 ramped-up, PORB de-asserts high.
(6) Device is waiting for SOCREADY to assert high.
(7) COLDBOOT asserts low.

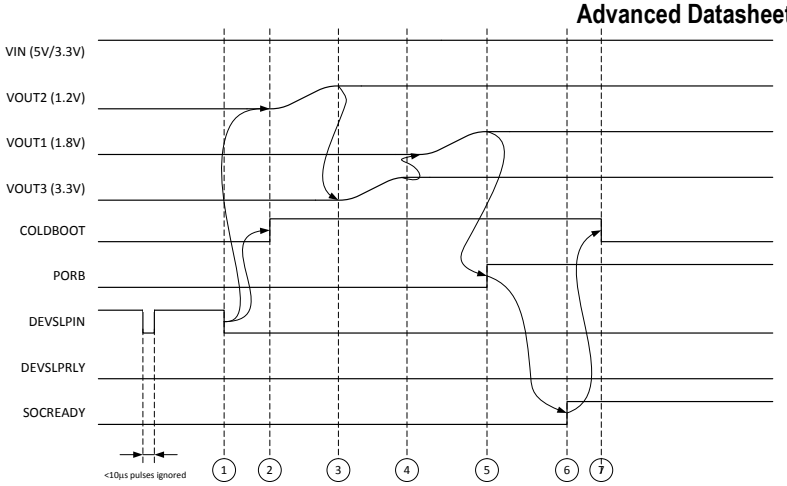


Figure 5. Mode1 - Device enters DevSlp

Device shut-down:

(1) VIN falls below the UVLO threshold, PORB asserts low.
(2) After 2ms delay, VOUT1 ramps down.
(3) VOUT3 ramps down.
(4) VOUT2 and VREF ramp down.

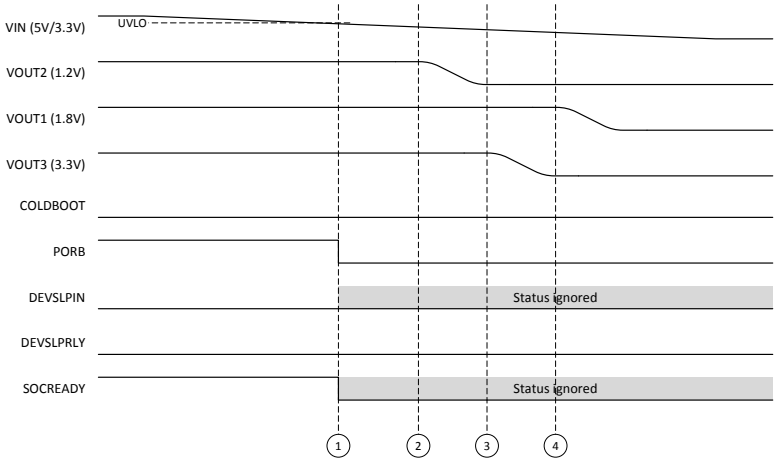


Figure 6. Mode1 - Device shut-down

Mode2 – Master Enable pin (MEN) with sequence

With IDTP9120 configured for mode2, a configurable state machine will ramp up/down all 3 regulators controlled by the MEN pin. The PORB output can be configured to indicate various power up conditions. Individual Power Good output pins indicate the regulator output being established.

Mode3 – Master Enable pin (MEN) with sequence and Standby Mode

With IDTP9120 configured for mode3, a configurable state machine will ramp up/down all 3 regulators controlled by the MEN pin. The PORB output can be configured to indicate various power up conditions. Individual Power Good output pins indicate the regulator output being established.

In addition to mode2, mode3 supports the STANDBY mode entered by asserting the STANDBY pin. During standby, Buck1,2 and/or 3 will be turned off without sequencing. The configuration is programmable via OTP.

Pin Description

DEVSLPIN

This pin allows the IC to enter and exit SLEEP mode. Sleep mode is the lowest power state of the device and is activated when DEVSLPIN is logic HIGH. The device will be in "normal operation" when DEVSLPIN is logic LOW. See figure 2 – Device Power States. For 1uA sleep mode operation, leave this pin floating. In floating operation, it is internally pulled up to ~1.5V. If pulled to Vin (between 3.0V and 6.0V), leakage current will flow between ~10uA to ~18uA respectively.

VINSEL

This pin allows the function of Buck 3 to be changed to a Switch function. Logic LOW on this pin puts the channel into Buck configuration, and a Logic HIGH on this pin puts the channel into Switch configuration. The UVLO threshold is also dependent on the VINSEL configuration. See **Table 4 – General Electrical Characteristics** for details.

PVIN1, PVIN2, PVIN3

PVINx is each buck converters' respective power supply input. They provide power to the internal MOSFETs for the switch mode regulator. Their operating range is 2.7V to 5.5V, and a 10µF capacitor must be placed as close as possible to each of the respective pins. A second 10µF capacitor should be used with PVIN3 because of the greater current sourcing capability of this channel. Because the capacitance value decreases with voltage, a 10V rated X7R ceramic capacitors must be used. X7R is preferred over X5R because the derating with X7R is less. For best performance, each of these power supply inputs is to be connected together on a dedicated circuit board power plane, and the trace going from these pins, to the dedicated power plane, must be made as short as possible. Y5V capacitors are not recommended because of their general low performance with respect to temperature, voltage derating, and higher resistance at high frequencies, minimizing their ability to filter out high frequency noise.

VIN

VIN is the power supply input for the bias and control portion of the integrated circuit. It too has an operating range of 2.7V to 5.5V, and a 2.2µF 10V rated X7R capacitor must be placed as close as possible to its pin. VIN should also be tied to the same power plane that the PVINx pins are tied to with as short a trace as possible. Do not use Y5V capacitors.

PGND1, PGND2, PGND3

These are the dedicated ground pins for each of the respective power supplies. The traces from these pins, to a dedicated ground plane must be made as short and wide as possible.

VGND

VGND is the ground pin for the bias and control portion of the integrated circuit. The trace from this pin, to a dedicated ground plane, should be made as short as possible.

EP

This is the exposed pad on the bottom side of the IC. It must be connected to a top or bottom circuit board ground plane to maximize the thermal dissipation performance of the IC.

VREF

The Vref pin tracks the output voltage of Buck 1, at half its value. A 2.2µF 6.3V rated X7R capacitor must be connected at this pin when enabled. This feature should be disabled in the OTP setting and left floating when not needed.

FB1, FB2, FB3

FB1, FB2, FB3 are the respective feedback pins of the output voltage for each buck converter. The LSB of the outputs for each channel is 25mV from 0.8000V to 3.3375V. In the layout, the feedback traces should be kept as short as possible and should never run parallel to the inductors nor to the inductor trace leading to the inductor switching pin. Feedback traces should always cross inductors and inductor traces on separate planes and at right angles.

LX1, LX2, LX3

LX1, LX2, LX3 are the switching pins of the respective buck converters. The IDTP9120 is optimized for 1µH small footprint chip inductors, and connect to the switching pins. The inductors must be placed as close as possible to the LX pins themselves.

GPI3, GPIO14, GPIO15, GPO16, GPIO17

These pins have multiple functions, see Table 9 for device mode depended mode function.

Component Selection

The IDTP9120 is a high performance triple DC-DC step down converter that satisfies the solution size demands of miniature portable electronic devices. It has two 2A outputs and one 3A output in a 4mm x 4mm QFN package. Only three external components are required per channel (Cin, Cout, L). Because it is designed to automatically switch to a pulse frequency modulation scheme at light loads, the IDTP9120 is able to maintain high efficiency across the entire load range while providing ultra-fast load transient response.

Input Capacitor

A 10µF ceramic capacitor or greater must be placed close to each PVIN pin for each channel for bypassing. For the VIN pin, a 2.2µF 10V capacitor is sufficient because the VIN pin is powering the low power internal circuitry of the IC.

Output Capacitor

A 10µF or greater ceramic capacitor must be placed close to each output inductor. Increasing the output capacitance will lower output ripple and improve load transient response but could also increase solution size or cost. The voltage rating of the output capacitor must be at least 6.3V.

Inductor Selection

The IDTP9120 has been designed for use with a 1.0µH inductor. A larger value inductor will produce lower output voltage ripple, but a slightly smaller inductor value will produce faster transient response. The best compromise is a 1.0µH inductor. The inductor must be rated for the maximum peak current. Selection of the inductor needs to ensure maximum operating current not just the DC current, and can be rated for a 40°C temperature rise. This maximum operating current or peak current for a buck converter can be calculated using equation 1

– eq (1);

where r is the inductor current ripple ratio and equal to eq (2).

eq (2);

where L and f are the inductor and switching frequency.

Simplifying gives equation 3:

eq (3).

Equation 3 shows that the peak inductor current is inversely related to the switching frequency and inductance. In other words, the lower the switching frequency or inductance, the higher the peak current. Peak current also increases as input voltage increases. The value of the inductor depends on the application. A validated inductor is the Toko 1239AS-H-1R0M.

Typical Operating Characteristics

Typical values at 25°C, unless noted. $V_{PVIN1} = V_{PVIN2} = V_{PVIN3} = Vin = 5V$. $C_{O(BUCK1)} = C_{O(BUCK2)} = 10\mu F$, $C_{O(BUCK3)} = 20\mu F$, L1=L2=L3 =1.0µH.

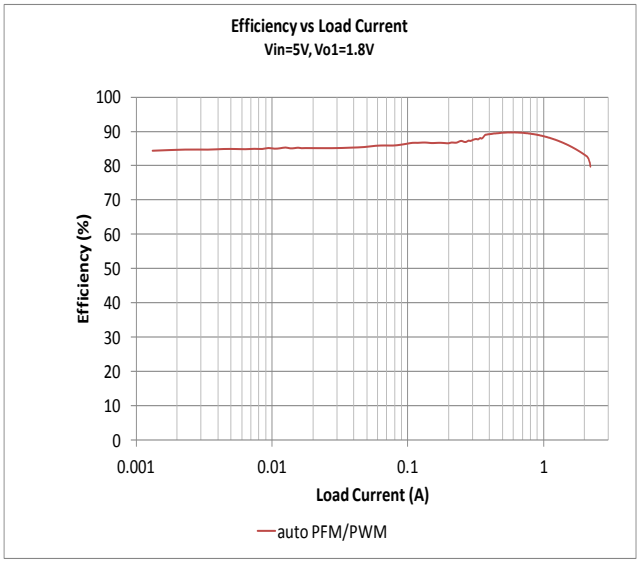


Figure 7. Channel 1 Efficiency

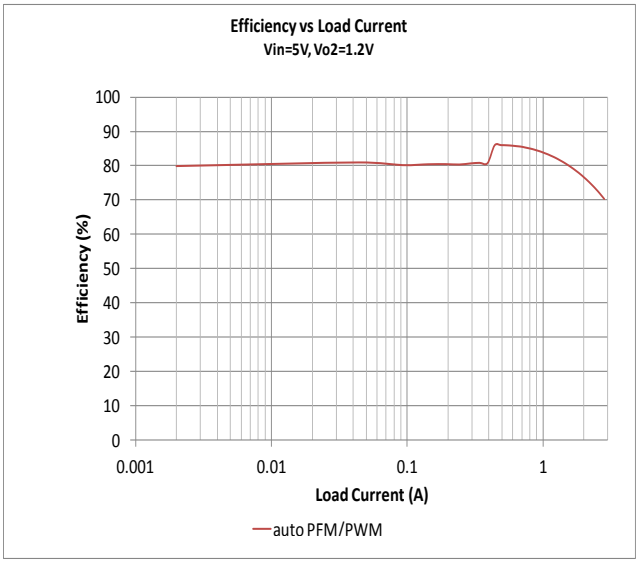


Figure 8. Channel 2 Efficiency

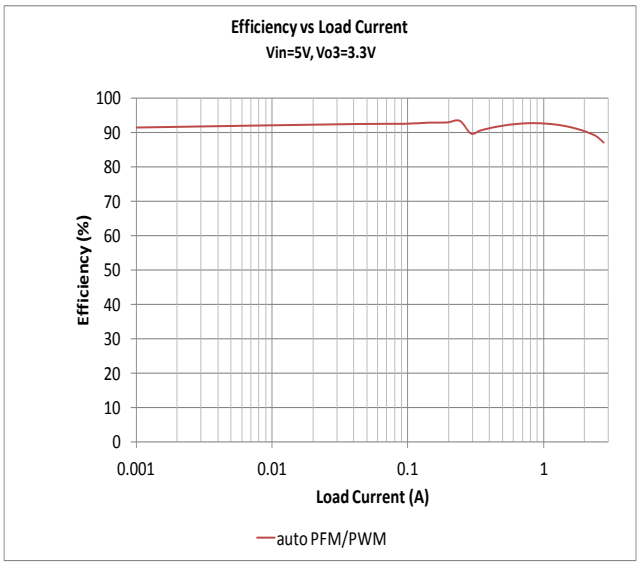


Figure 9. Channel 3 Efficiency

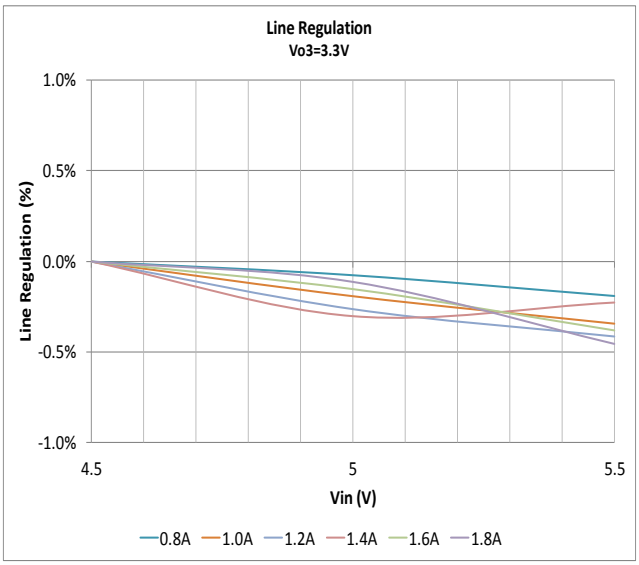


Figure 10. Channel 3 Line Regulation

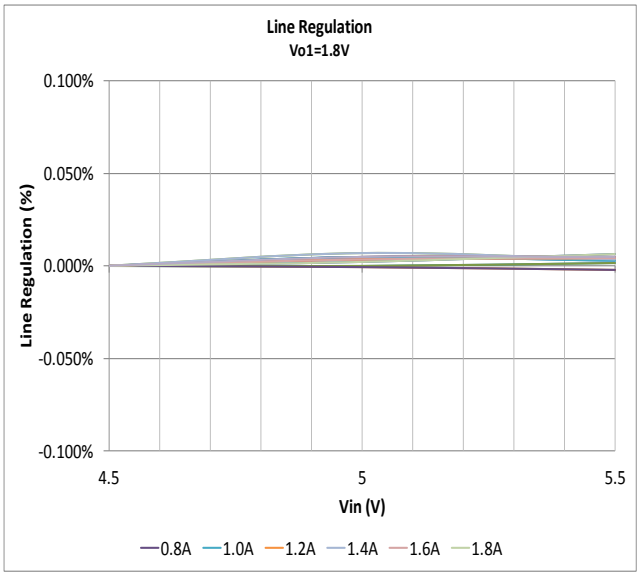


Figure 11. Channel 1 Line Regulation

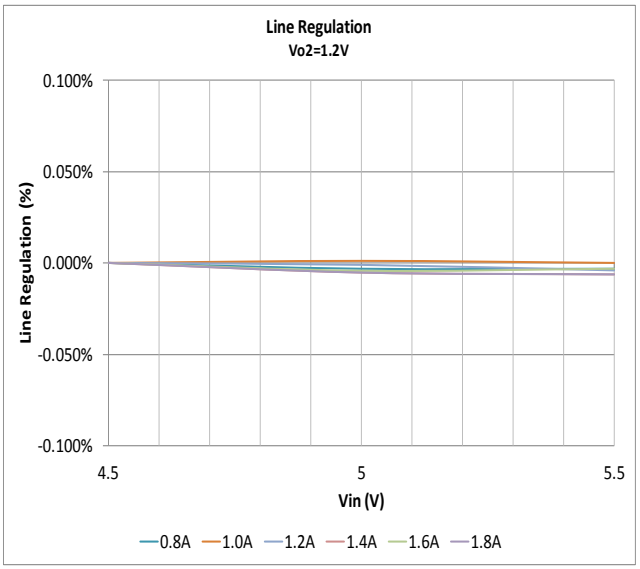


Figure 12. Channel 2 Line Regulation

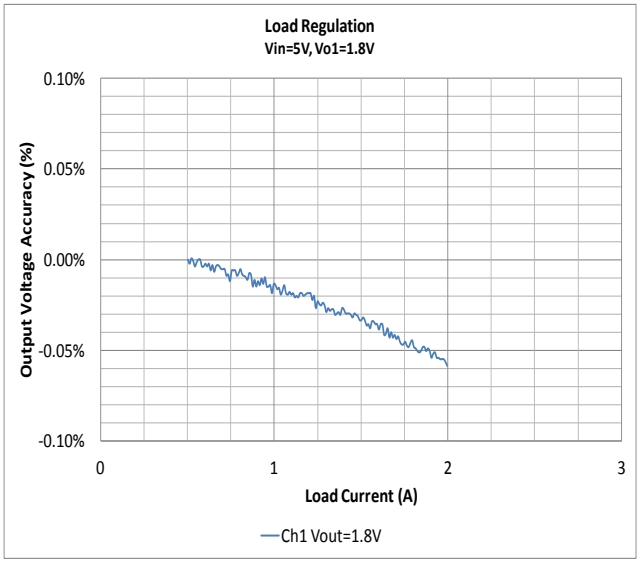


Figure 13. Channel 1 Load Regulation

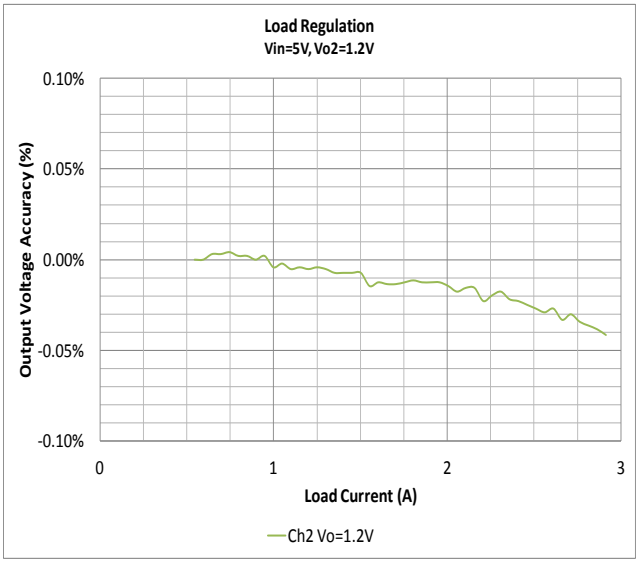


Figure 14. Channel 2 Load Regulation

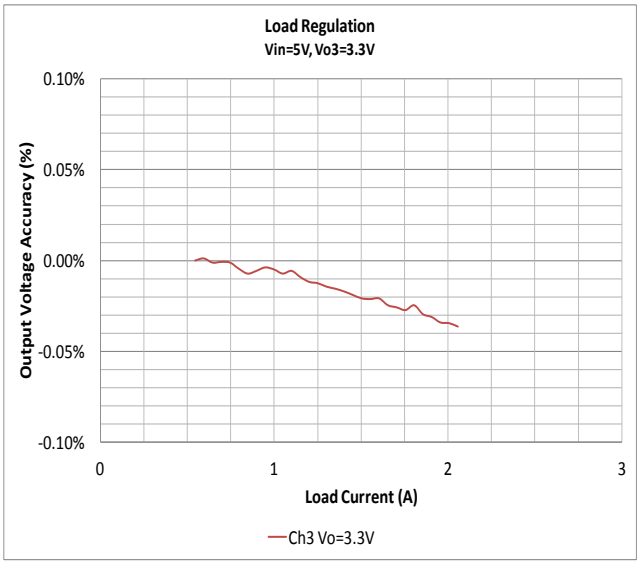


Figure 15. Channel 3 Load Regulation

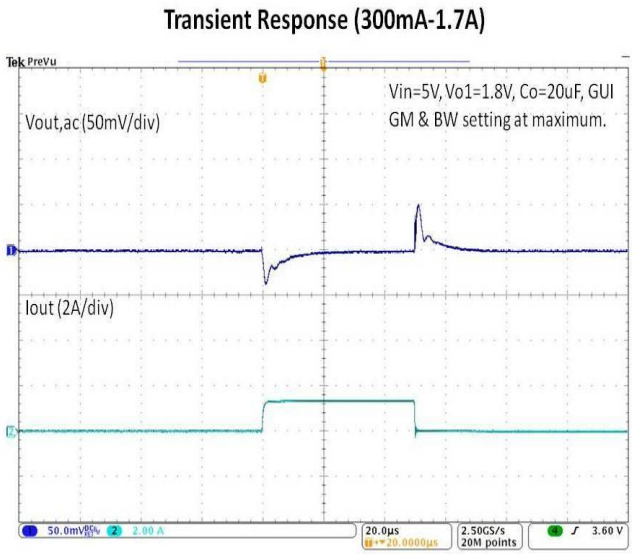


Figure 16. Channel 1 Load Transient Response

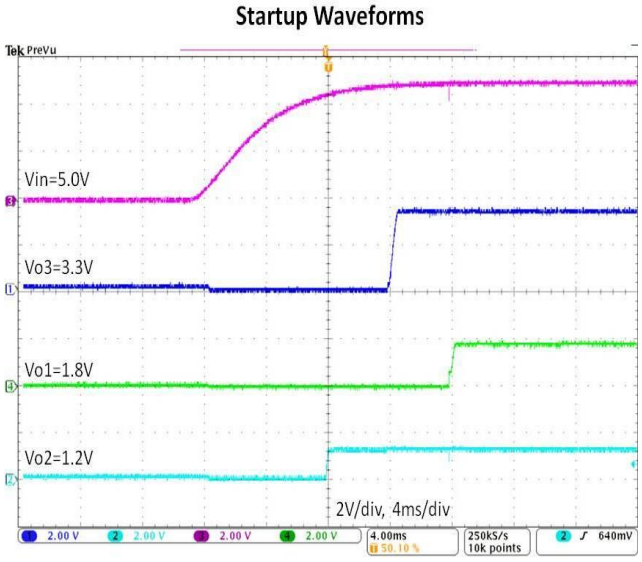


Figure 17. All Channel Startup Waveforms

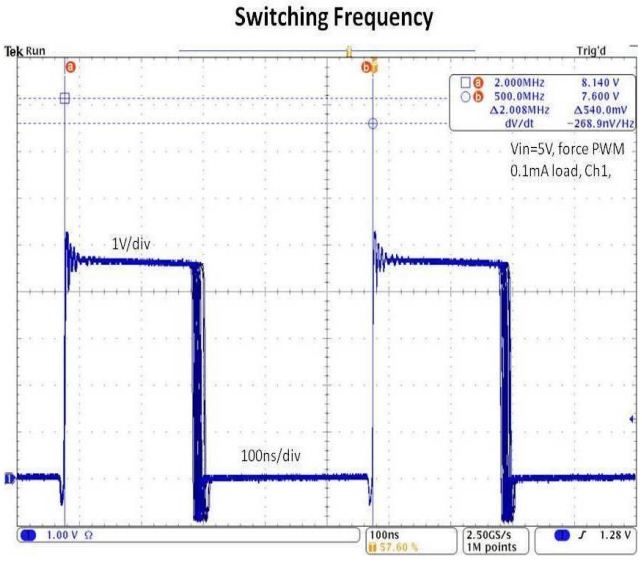


Figure 18. Channel 1 Switch Node Switching Frequency

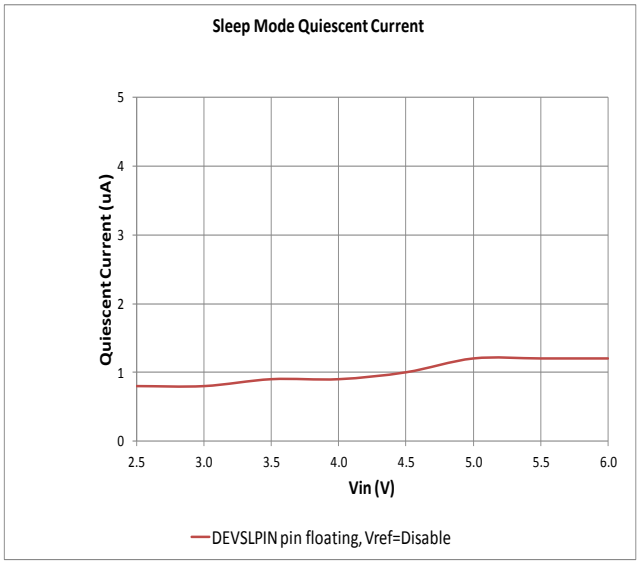


Figure 19. Sleep Quiescent Current

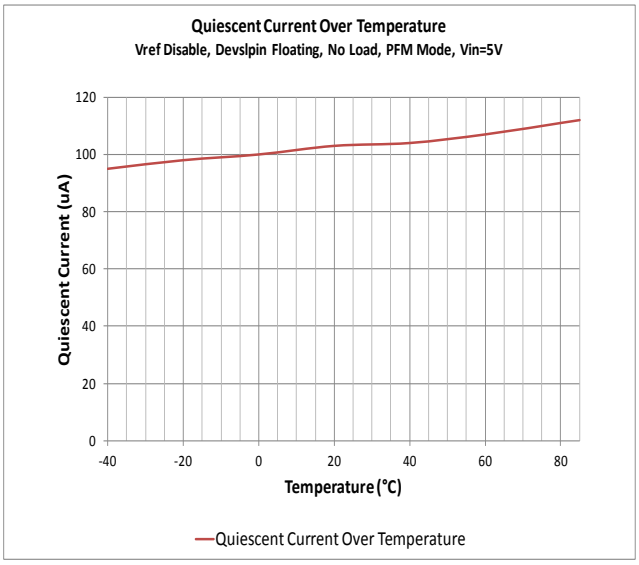


Figure 20. Quiescent Current Over Temperature

OTP Register Mapping

The following table lists all configurable OTP registers available in the IDTP9120.

The registers can be programmed for evaluation purpose using the IDTP9120 Evaluation Kit (IDTP9120-EVAL) with the included GUI software. The final production configuration will be programmed by IDT during final test.

(Bank T0)

Trim Bits (Default)	Parametric Trim Descriptions
T0[29] (0)	DEVSLP Mode Support: Sets device behavior when supply is initially applied. 0 : Device always powers up independent of DEVSLPIN pin state. SSD (Solid State Disk) application mode. 1 : Device powers up only when DEVSLPIN is low.

(Bank T1)

Trim Bits (Default)	Parametric Trim Descriptions
T1[22:21] (00)	Buck1 Slope Compensation Select: Device option for Buck 1. To be selected based on inductor value and expected PWM duty cycle. 00 : Slope comp=Nominal 01 : Slope comp=+20% 10 : Slope comp=+100% 11 : Slope comp=+40%
T1[24:23] (00)	Buck2 Slope Compensation Select: Device option for Buck 2. To be selected based on inductor value and expected PWM duty cycle. 00 : Slope comp=Nominal 01 : Slope comp=+20% 10 : Slope comp=+100% 11 : Slope comp=+40%
T1[26:25] (00)	Buck3 Slope Compensation Select: Device option for Buck 3. To be selected based on inductor value and expected PWM duty cycle. 00 : Slope comp=Nominal 01 : Slope comp=+20% 10 : Slope comp=+100% 11 : Slope comp=+40%

(Bank T2)

Trim Bits (Default)	Parametric Trim Descriptions
T2[0] (0)	Buck1 Transconductance Selection: Relevant for all modes 0 : Nominal 1 : 3x transconductance
T2[1] (0)	Buck1 Bandwidth Selection: Relevant for all modes 0 : Nominal 1 : 2x bandwidth
T2[2] (0)	Buck1 Forced PWM Mode: Relevant for all modes 0 : Auto-switching between PWM & PFM modes 1 : Forced PWM mode
T2[3] (0)	Buck2 Transconductance Selection: 0 : Nominal 1 : 3x transconductance
T2[4] (0)	Buck2 Bandwidth Selection: 0 : Nominal 1 : 2x bandwidth
T2[5] (0)	Buck2 Forced PWM Mode: 0 : Auto-switching between PWM & PFM modes 1 : Forced PWM mode
T2[6] (0)	Buck3 Transconductance Selection: 0 : Nominal 1 : 3x transconductance
T2[7] (0)	Buck3 Bandwidth Selection: 0 : Nominal 1 : 2x bandwidth
T2[8] (0)	Buck3 Forced PWM Mode: 0 : Auto-switching between PWM & PFM modes 1 : Forced PWM mode
T2[10:9] (00)	Power-Off Sequencer Delay 1: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms
T2[12:11] (00)	Power-Off Sequencer Delay 2: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms

(Bank T2)

Trim Bits (Default)	Parametric Trim Descriptions
T2[15:13] (000)	Buck Power-Off Sequence Selection: Relevant only when mode[1:0]≠'00' 000 : Buck2 → Buck3 → Buck1 001 : Buck2 → Buck1 → Buck3 010 : Buck1 → Buck2 → Buck3 011 : Buck1 → Buck3 → Buck2 100 : Buck3 → Buck1 → Buck2 101 : Buck3 → Buck2 → Buck1 110 : Buck1 → Buck2 & Buck3 111 : Buck2 → Buck1 & Buck3
T2[18:16] (000)	PORB Output Boolean Operator Selection: PG=Power Good 000 : PG1 & PG2 & PG3 001 : PG1 010 : PG2 011 : PG3 100 : PG1 & PG2 101 : PG1 & PG3 110 : PG2 & PG3 111 : reserved
T2[19] (0)	GPI3 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND) 1 : Enable (100kΩ pull-up to VIN)
T2[20]	Unused
T2[21] (0)	GPIO14 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND when pin configured as input) 1 : Enable (50kΩ pull-up to supply voltage selected by gpio14_vio)
T2[22] (0)	GPIO14 Open-Drain Output Select: Relevant only when pin configured as output. 0 : Push-pull output 1 : Open-drain output
T2[23] (0)	GPIO14 I/O Voltage Select: For both input buffer and push-pull output driver. 0 : VOUT3 (FB3) 1 : VOUT1 (FB1)
T2[24] (0)	GPIO15 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND when pin configured as input) 1 : Enable (50kΩ pull-up to supply voltage selected by gpio15_vio)
T2[25] (0)	GPIO15 Open-Drain Output Select: Relevant only when pin configured as output. 0 : Push-pull output 1 : Open-drain output
T2[26] (0)	GPIO15 I/O Voltage Select: For both input buffer and push-pull output driver. 0 : VOUT3 (FB3) 1 : VOUT1 (FB1)
T2[27] (0)	GPO16 Internal Pull-up Enable: 0 : Disable 1 : Enable (50kΩ pull-up to supply voltage selected by gpo16_vo)

T2[28] (0)	GPO16 Open-Drain Output Select: 0 : Push-pull output 1 : Open-drain output
T2[29] (0)	GPO16 Output Voltage Select: For push-pull output driver. 0 : VOUT3 (FB3) 1 : VOUT1 (FB1)
T2[30] (0)	GPIO17 Internal Pull-up Enable: 0 : Disable (1μA pull-down to VGND when pin configured as input) 1 : Enable (50kΩ pull-up to supply voltage selected by gpio17_vio)
T2[31] (0)	GPIO17 Open-Drain Output Select: Relevant only when pin configured as output. 0 : Push-pull output 1 : Open-drain output
T2[32] (0)	GPIO17 I/O Voltage Select: For both input buffer and push-pull output driver. 0 : VOUT3 (FB3) 1 : VOUT1 (FB1)
T2[33] (0)	VREF Output Disable: 0 : VREF = 0.5 x VOUT1(FB1) 1 : VREF output disabled

(Bank T3)

Trim Bits (Default)	Parametric Trim Descriptions
T3[1:0] (00)	Device I/O Configuration and Control: 00 : Individual regulator enable via pins 01 : Special Sequence mode 10 : Master enable control with programmable sequencing 11 : Master enable control with programmable sequencing + SLEEP mode support
T3[2] (0)	TSD & UVLO Fault Disable: Used for device characterization and burn-in only. 0 : Fault event shuts down all Buck regulators (programmed sequence) 1 : Fault ignored
T3[5:3] (000)	Buck Power-On Sequence Selection: Relevant only when mode[1:0]≠'00' 000 : Buck2 → Buck3 → Buck1 001 : Buck3 → Buck1 → Buck2 010 : Buck3 → Buck2 → Buck1 011 : Buck1 → Buck3 → Buck2 100 : Buck2 → Buck1 → Buck3 101 : Buck1 → Buck2 → Buck3 110 : Buck2 & Buck3 → Buck1 111 : Buck1 & Buck3 → Buck2
T3[6] (0)	Buck1 SLEEP Mode Support: Relevant only when mode[1:0]='11' 0 : Buck1 not affected by SLEEP mode 1 : Buck1 supports SLEEP mode control

(Bank T3)

Trim Bits (Default)	Parametric Trim Descriptions	
T3[7] (0)	Buck2 SLEEP Mode Support: Relevant only when mode[1:0]='11' 0 : Buck2 not affected by SLEEP mode 1 : Buck2 supports SLEEP mode control	
T3[8] (0)	Buck3 SLEEP Mode Support: Relevant only when mode[1:0]='11' 0 : Buck3 not affected by SLEEP mode 1 : Buck3 supports SLEEP mode control	
T3[10:9] (00)	Power-On Sequencer Delay 1: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms	
T3[12:11] (00)	Power-On Sequencer Delay 2: Relevant only when mode[1:0]≠'00' 00 : 0.5ms 01 : 1ms 10 : 2ms 11 : 4ms	
T3[19:13] (0x00)	Vout1: (1.800V)	000d : 1.800V(Vout1) / 1.200V(Vout2) / 3.300V(Vout3) 001d : 0.800V 002d : 0.825V 003d : 0.850V : : : : 100d : 3.275V 101d : 3.300V 102d : 3.325V ≥103d : 3.3375V
T3[26:20] (0x00)	Vout2: (1.200V)	
T3[33:27] (0x00)	Vout3: (3.300V)	

APPLICATION INFORMATION

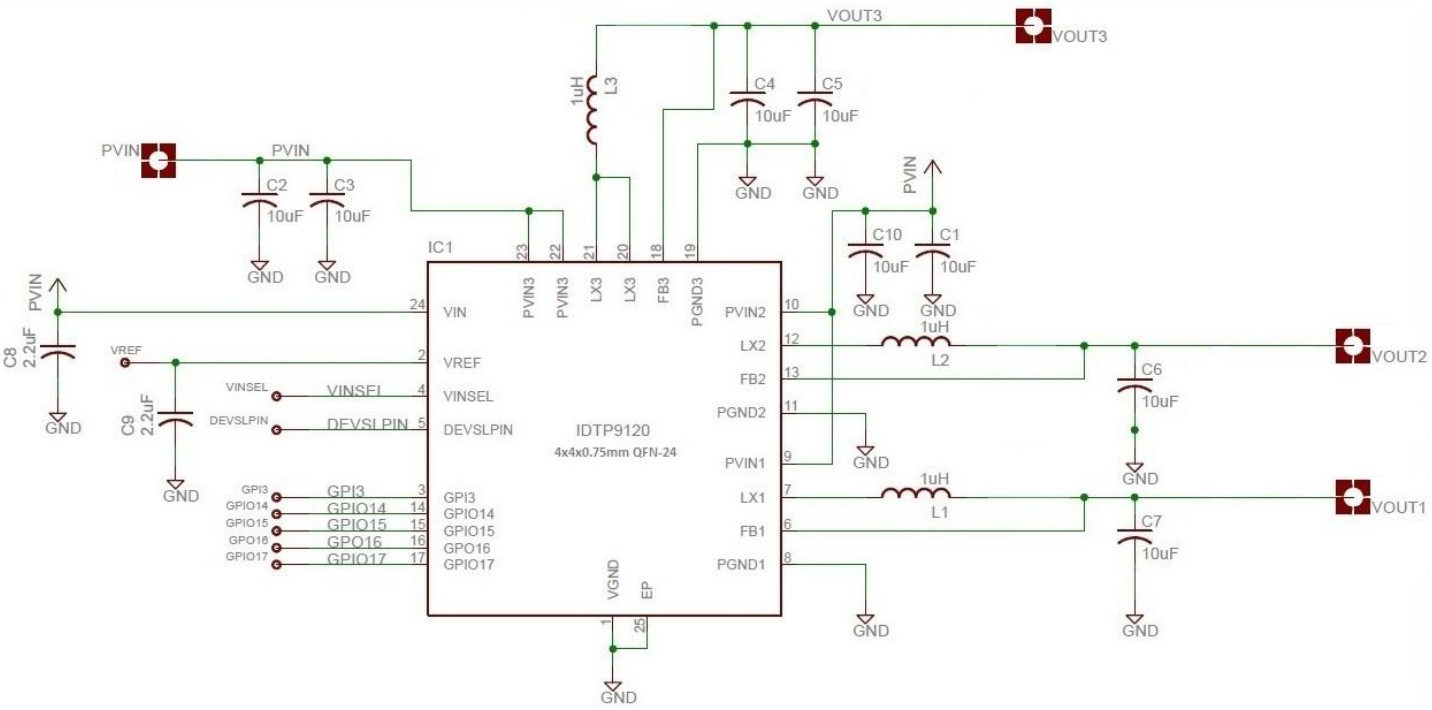


Figure 21. Minimum component schematic of IDTP9120.

BILL OF MATERIALS

#	Description	Package	Manufacturer Part Number
IC1	IDTP9120-00NBGI	4X4QFN	IDT
L1-L3	1uH	2520/1008	TOKO 1239AS-H-1R0M
C1-C3, C10	10uF, 10v, X7R	0805/2012	C0805C106K8RACTU
C4-C7	10uF, 6.3v, X7R	1206/3216	C1206C106K9RACTU
C8-C9	2.2uF, 10v, X7R	0603/1608	06036C225KAT2A

PACKAGE INFORMATION

Please refer to the documents located under http://www.idt.com/package/nbg24 for detailed package outline, recommended footprint, carrier and RoHS information. IDTP9120 is using the P1-NBG24 package option (EP size: 2.8mm)

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.