User's Guide
SLVU244–June 2008

TPS65136EVM-265

This user's guide describes the characteristics, operation, and use of the TPS65136EVM evaluation module (EVM). This EVM contains the Texas Instruments TPS65136 positive and negative output supply integrated circuit. This user's guide includes EVM specifications, recommended test setup, bill of materials, a schematic diagram, and the board layout.

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1 Introduction

The Texas Instruments TPS65136EVM evaluation module uses a TPS65136 single-inductor, multiple output regulator to provide both a positive and negative power rail. The goal of the EVM is to facilitate evaluation of the TPS65136.

1.1 Performance Specification Summary

Table 1 provides a summary of the TPS65136EVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYP	MAX	MIN	TYP	MAX
VIN		2.3		5.5			1000
VPOS	V_I = 3.7 V	4.55	4.6	4.56	80		
VNEG	V_I = 3.7 V	-5.1	-5	-4.9	80		

2 Input/Output Connector Descriptions

J1–VIN and GND This is the positive and return connections (three pins each) to the input power supply. Twist the leads to the input supply and keep them as short as possible.

J2–OUTP and GND This is the positive output of the device and some GND pins (two pins each).

J3–EN This is the enable pin for both converters. Placing a jumper across pins 1 and 2 shorts the EN pin to GND (OFF), thereby disabling the device. Placing a jumper across pins 2 and 3 shorts the EN pin to VIN (ON), thereby enabling the converter.

J4–OUTN and GND This is the negative output of the device and some GND pins (two pins each). The load in most applications is connected between OUTP and OUTIN, not to GND.

3 Bill of Materials and Schematic

3.1 Bill of Materials

Table 2. HPA265 Bill of Materials

COUNT	Ref Des	Value	DESCRIPTION	SIZE	Part Number	MFR
1	C1	10 µF	Capacitor, Ceramic, 10V, X7R, 10%	0805	STD	Murata
2	C2, C3	4.7 µF	Capacitor, Ceramic, 10V, X7R, 10%	0805	STD	Murata
1	C4	100 nF	Capacitor, Ceramic, 10V, X7R	0603	STD	Murata
1	J1	PTC36SAAN	Header, Male 6-pin, 100mil spacing, (36-pin strip)	0.100 inch × 6	PTC36SAAN	Sullins
1	J2, J4	PTC36SAAN	Header, Male 4 pin, 100mil spacing, (36-pin strip)	0.100 inch × 4	PTC36SAAN	Sullins
1	J3	PTC36SAAN	Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 inch × 3	PTC36SAAN	Sullins
1	L1**	4.7 µH	Inductor, SMT, 1.0A, 175mΩ	0.116 × 0.116 inch	LPS3008-222ML	Coilcraft
1	R1	100	Resistor, Chip, 1/10W, 1%	0805	STD	STD
1	R2	162k	Resistor, Chip, 1/10W, 1%	0805	STD	STD
1	R3	909k	Resistor, Chip, 1/10W, 1%	0805	STD	STD
1	U1**	TPS65136	IC, Single inductor multiple output reg. for AMOLED	QFN-16	TPS65136RTE	TI
1	--		Shunt, 100 mil, Black	0.100	929950-00	3M
	--		PCB		HPA265	Any

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted.
All other components can be substituted with equivalent MFG's components.

3.2 Schematic

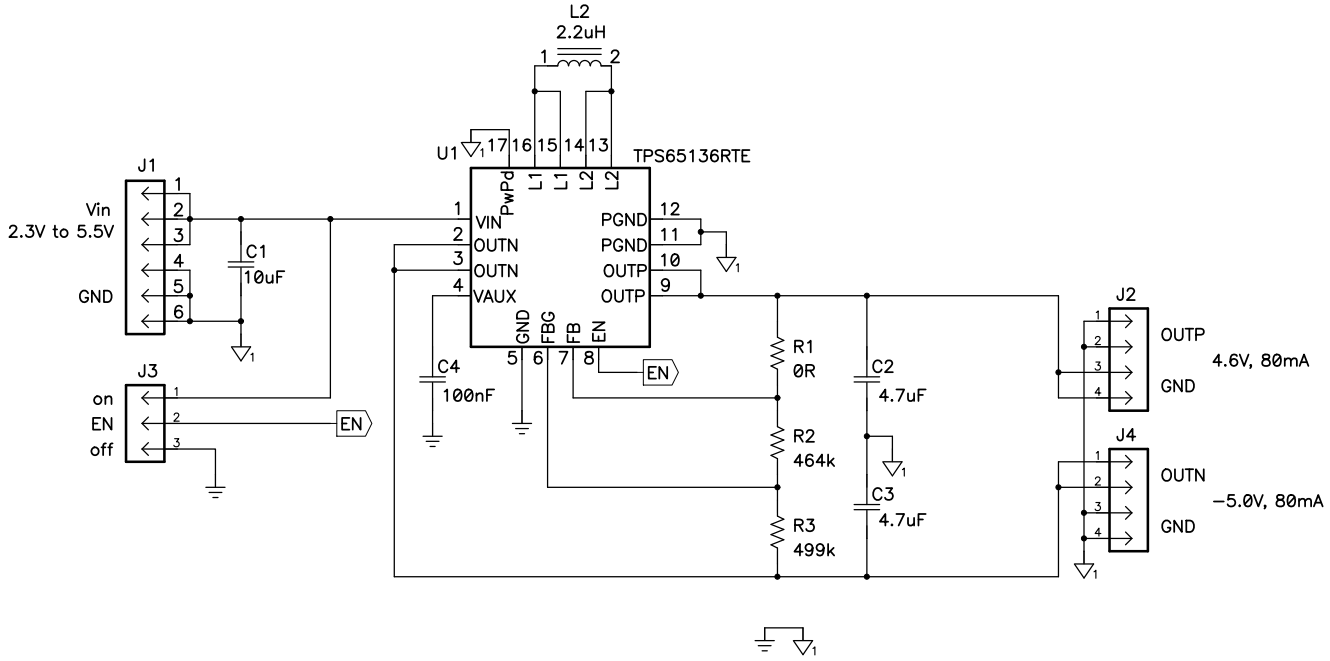

Figure 1. TPS65136EVM Schematic

4 Board Layout

Board layout is critical for all switch mode power supplies. Figure 2, Figure 3, and Figure 4 show the board layout for the HPA265 PCB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry, and careful attention has been given to the routing of high-frequency current loops. See the data sheet for more specific layout guidelines.

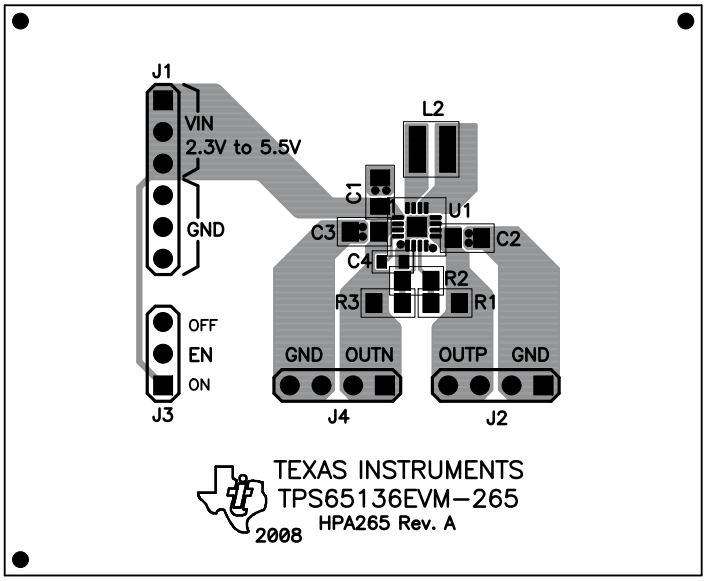

Figure 2. Top Assembly Layer

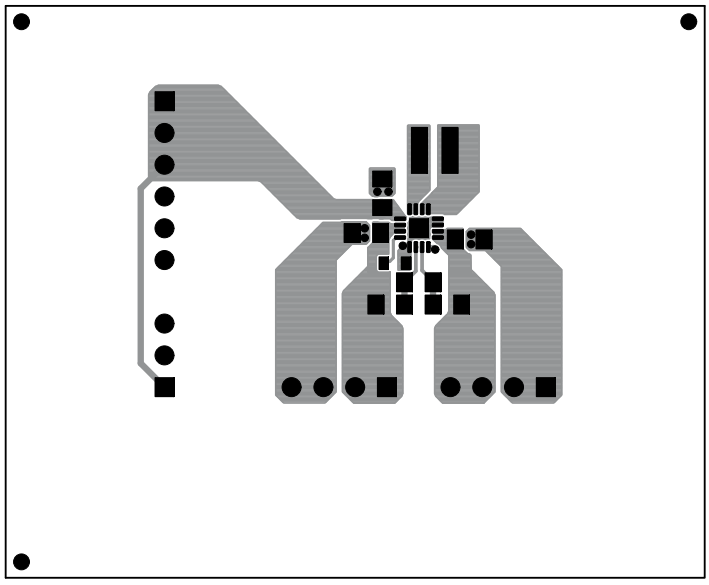

Figure 3. Top Layer

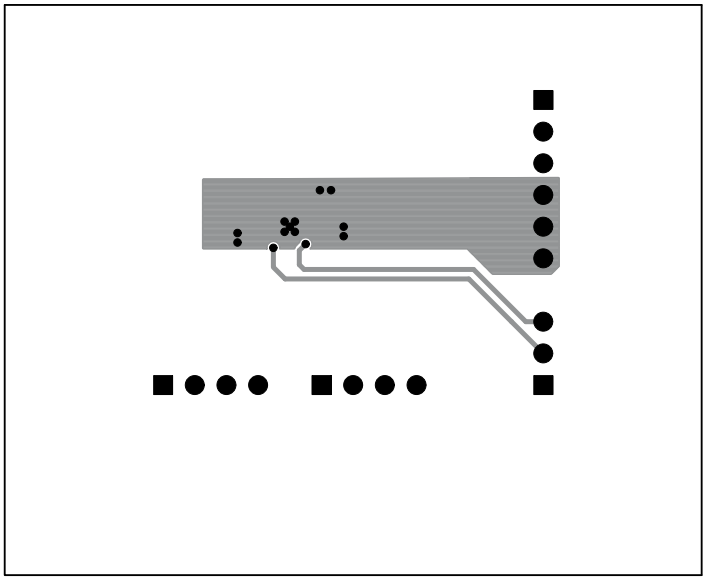

Figure 4. Bottom Layer

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Data Sheets:	**Literature Number:**
TPS65136	SLVS831

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7 V to 5.5 V and the output voltage range of -15 V to 15 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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