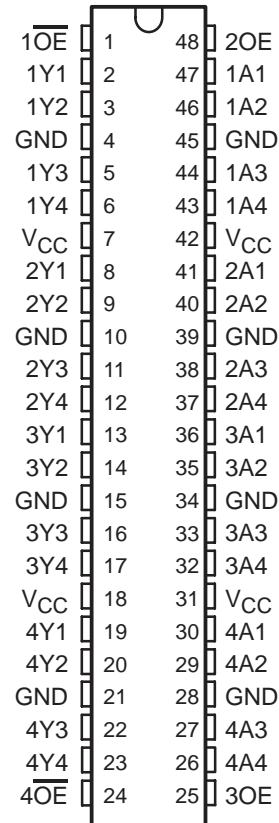


54ACT16241, 74ACT16241 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS189A – MARCH 1990 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

54ACT16241 . . . WD PACKAGE
74ACT16241 . . . DL PACKAGE
(TOP VIEW)



description

The 'ACT16241 are 16-bit buffers or line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and complementary output-enable (OE and \overline{OE}) inputs.

The 74ACT16241 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16241 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74ACT16241 is characterized for operation from -40°C to 85°C .



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54ACT16241, 74ACT16241
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

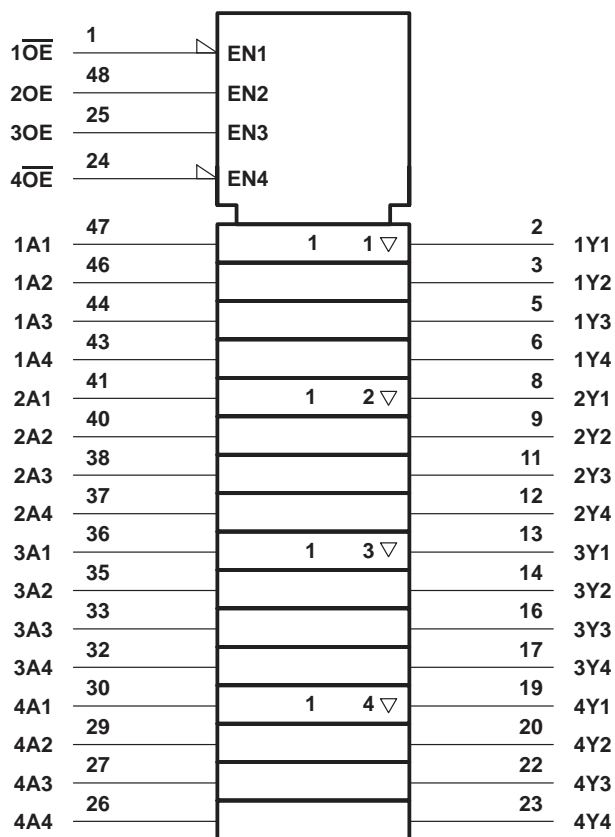
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FUNCTION TABLES

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

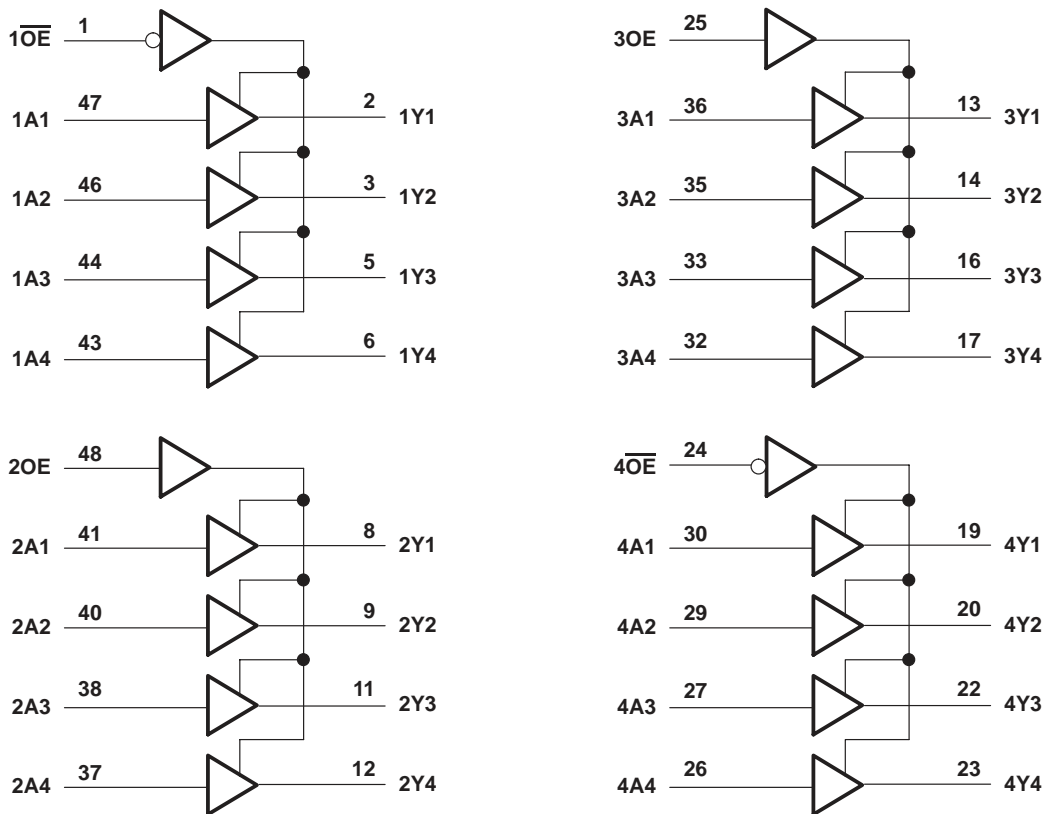
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 400 mA
Maximum package power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package	1.2 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

54ACT16241, 74ACT16241 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		54ACT16241			74ACT16241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
I _{OH}	High-level output current			-24			-24	mA
I _{OL}	Low-level output current			24			24	mA
Δt/Δv	Input transition rise or fall rate	0		10	0		10	ns/V
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT16241		74ACT16241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		4.4	V	
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
		5.5 V				3.85		3.85		
V _{OL}	I _{OL} = 50 μA	4.5 V		0.1		0.1		0.1	V	
		5.5 V		0.1		0.1		0.1		
	I _{OL} = 24 mA	4.5 V		0.36		0.44		0.44		
		5.5 V		0.36		0.44		0.44		
		5.5 V				1.65		1.65		
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1	μA	
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5		±5		±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8		80		80	μA	
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V		0.9		1		1	mA	
C _i	V _I = V _{CC} or GND	5 V		4.5					pF	
C _o	V _O = V _{CC} or GND	5 V		13					pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

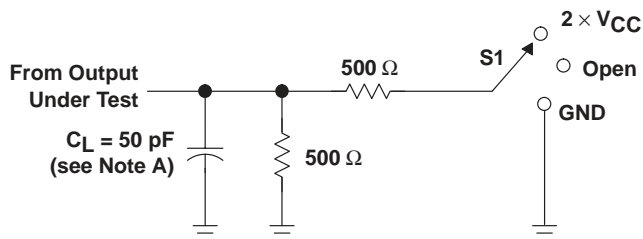
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT16241		74ACT16241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.3	6.5	8.4	3.3	9.5	3.3	9.5	ns
t_{PHL}			2.3	6.3	8.2	2.3	9.1	2.3	9.1	
t_{PZH}	\overline{OE} or OE	Y	2.3	6.5	8.3	2.3	9.4	2.3	9.4	ns
t_{PZL}			2.9	7.3	9.3	2.9	10.5	2.9	10.5	
t_{PHZ}	\overline{OE} or OE	Y	4.3	8.9	10.6	4.3	11.6	4.3	11.6	ns
t_{PLZ}			4	8.1	9.8	4	10.7	4	10.7	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	43	pF
		Outputs disabled	10	

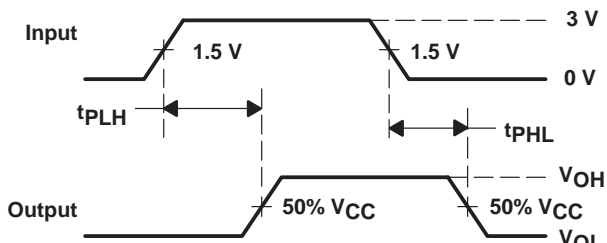
$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$

PARAMETER MEASUREMENT INFORMATION

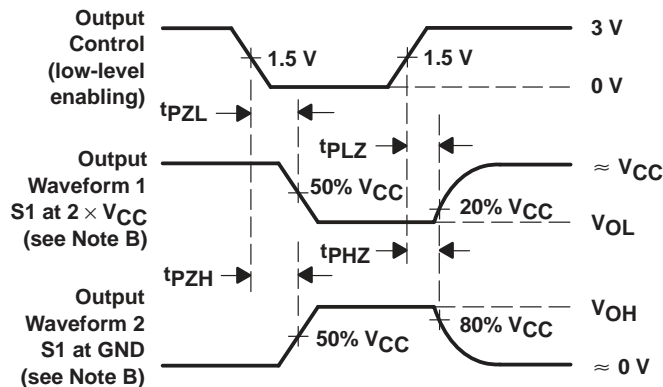


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT16241DL	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
74ACT16241DLR	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

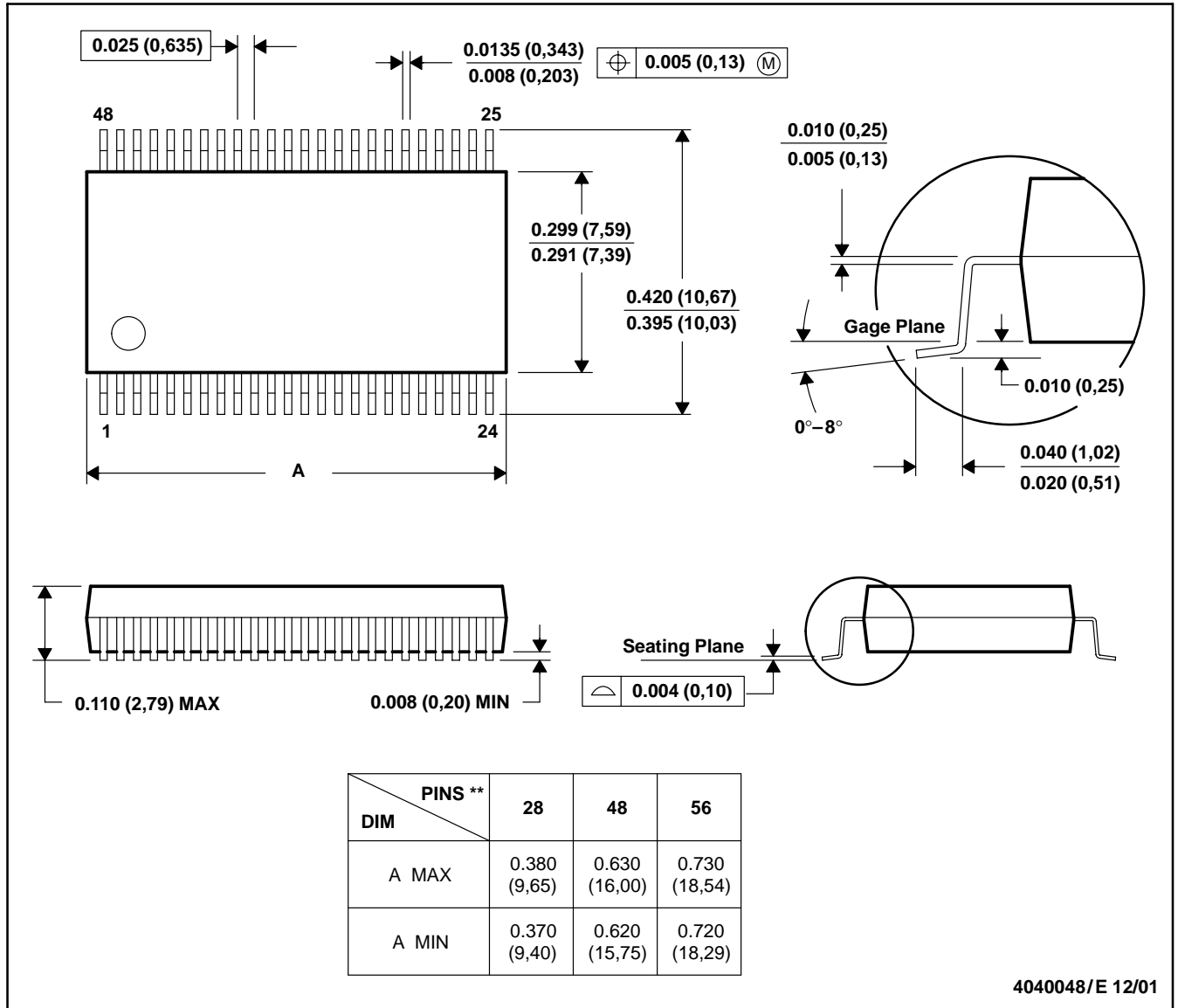
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DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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