

N-channel 500 V, 0.299 Ω typ., 11 A MDmesh™ DM2 Power MOSFET in a DPAK package

Datasheet - production data

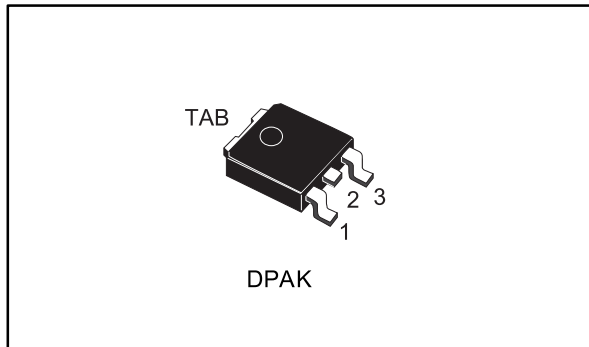
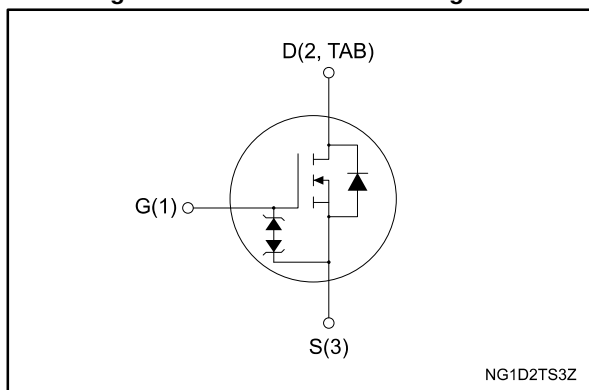


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STD12N50DM2	500 V	0.350 Ω	11 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh DM2 fast recovery diode series. It offers very low recovery charge and time (Q_{rr}, t_{rr}) combined with low R_{DS(on)}, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD12N50DM2	12N50DM2	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±25	V
I _D	Drain current (continuous) at T _C = 25 °C	11	A
I _D	Drain current (continuous) at T _C = 100 °C	8	
I _{DM} ⁽¹⁾	Drain current (pulsed)	44	A
P _{TOT}	Total dissipation at T _C = 25 °C	110	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	40	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/ns
T _{stg}	Storage temperature range	-55 to 150	°C
T _j	Operating junction temperature range		

Notes:

(1) Pulse width limited by safe operating area.

(2) I_{SD} ≤ 11 A, di/dt ≤ 400 A/μs; V_{DS peak} < V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}

(3) V_{DS} ≤ 400 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	1.14	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	50	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 oz Cu board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	2.5	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	320	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		0.299	0.350	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	628	-	pF
C_{oss}	Output capacitance		-	38	-	pF
C_{rss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}$, $V_{GS} = 0\text{ V}$	-	69	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	7	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 11\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	16	-	nC
Q_{gs}	Gate-source charge		-	4.6	-	nC
Q_{gd}	Gate-drain charge		-	7	-	nC

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 5.5\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	12.5	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off-delay time		-	28	-	ns
t_f	Fall time		-	9.8	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 11\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	140		ns
Q_{rr}	Reverse recovery charge		-	0.707		μC
I_{RRM}	Reverse recovery current		-	10.1		A
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	190		ns
Q_{rr}	Reverse recovery charge		-	1.111		μC
I_{RRM}	Reverse recovery current		-	11.7		A

Notes:

(1) Pulse width is limited by safe operating area

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

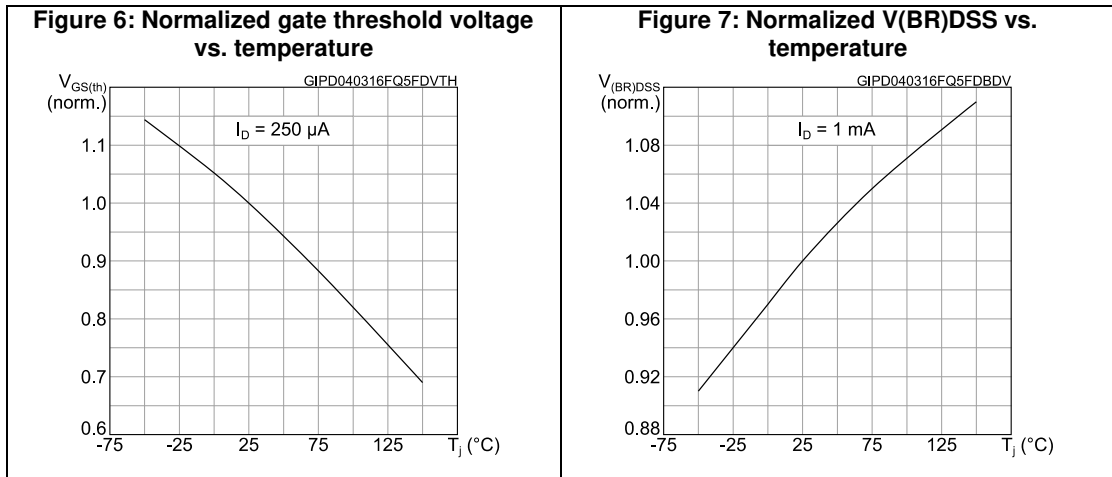
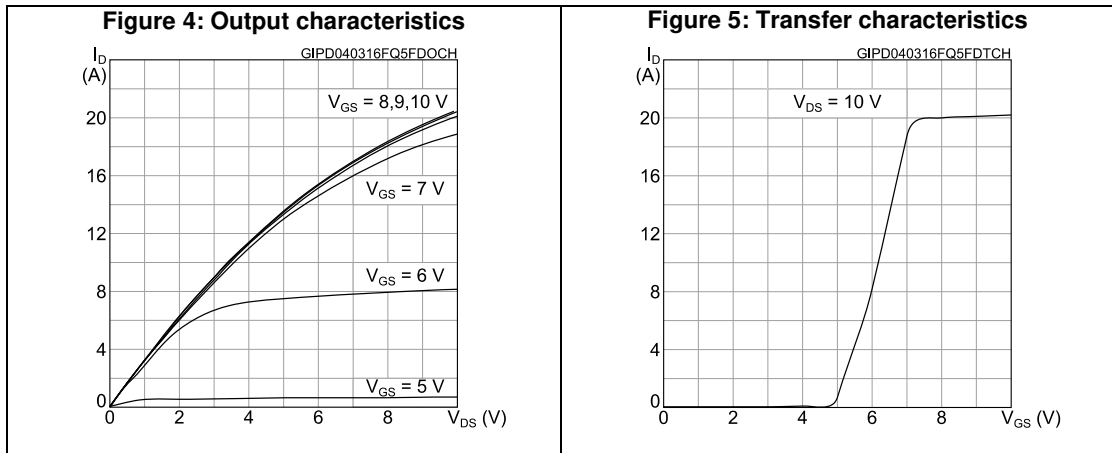
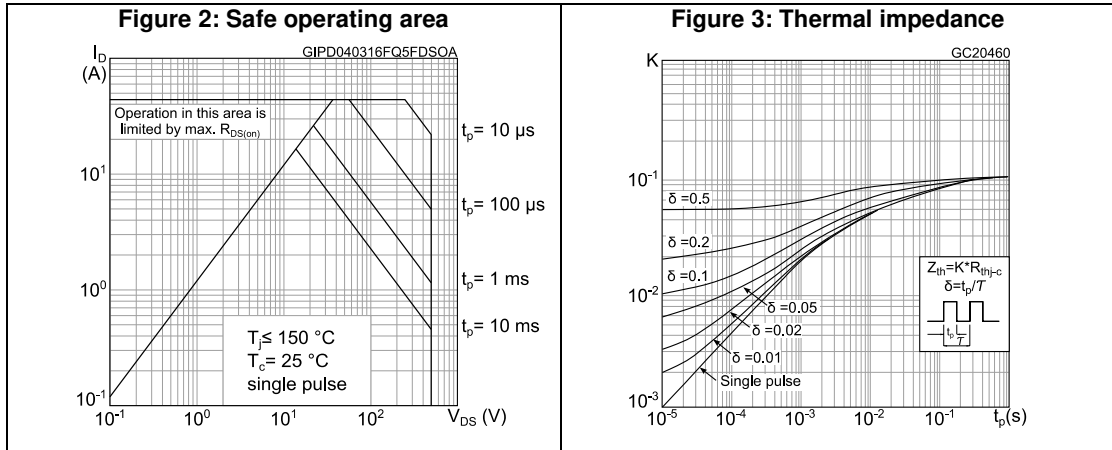


Figure 8: Static drain-source on-resistance

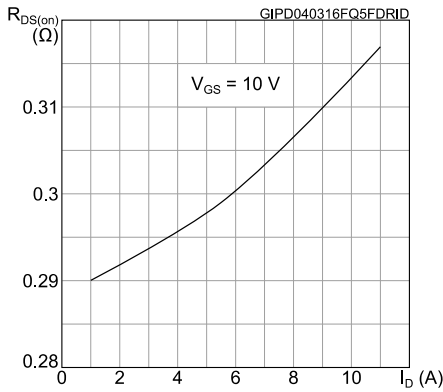


Figure 9: Normalized on-resistance vs. temperature

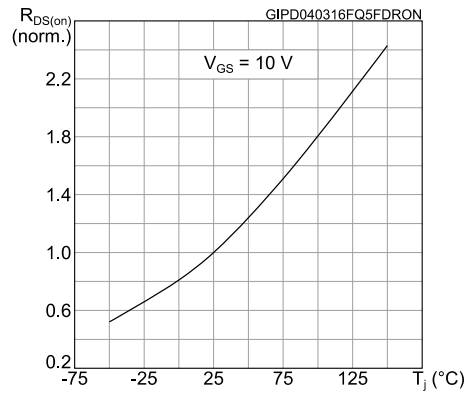


Figure 10: Gate charge vs. gate-source voltage

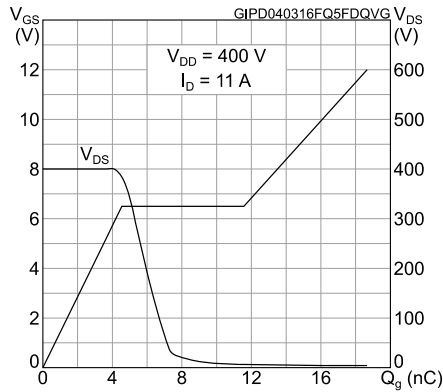


Figure 11: Capacitance variations

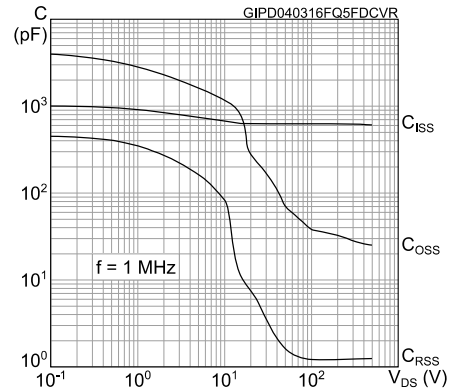


Figure 12: Output capacitance stored energy

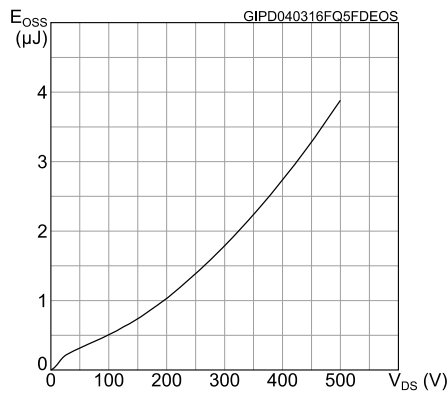
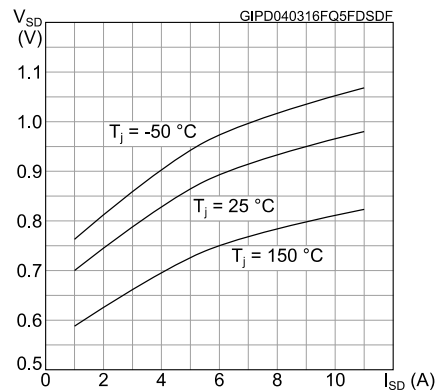
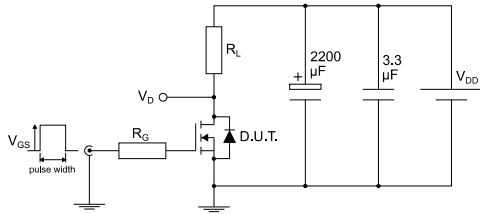


Figure 13: Source-drain diode forward characteristics



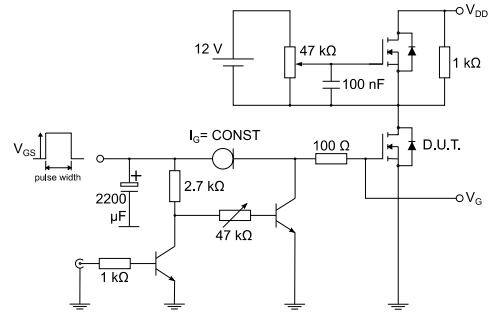
3 Test circuits

Figure 14: Test circuit for resistive load switching times



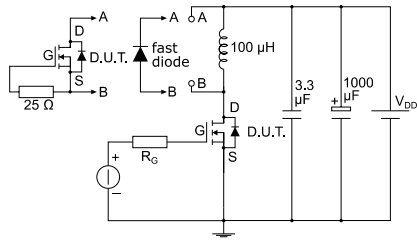
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Figure 15: Test circuit for gate charge behavior



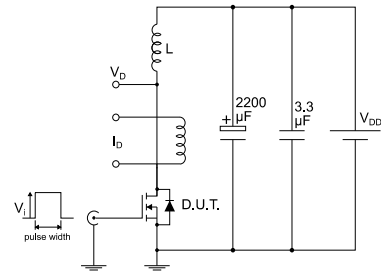
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Figure 16: Test circuit for inductive load switching and diode recovery times



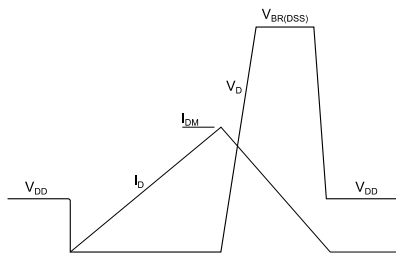
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Figure 17: Unclamped inductive load test circuit



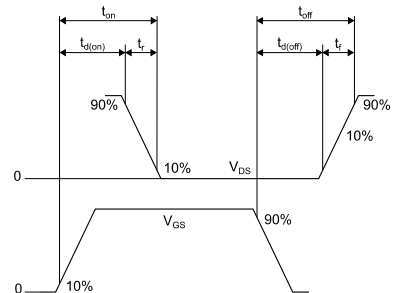
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK package information

Figure 20: DPAK (TO-252) type A2 package outline

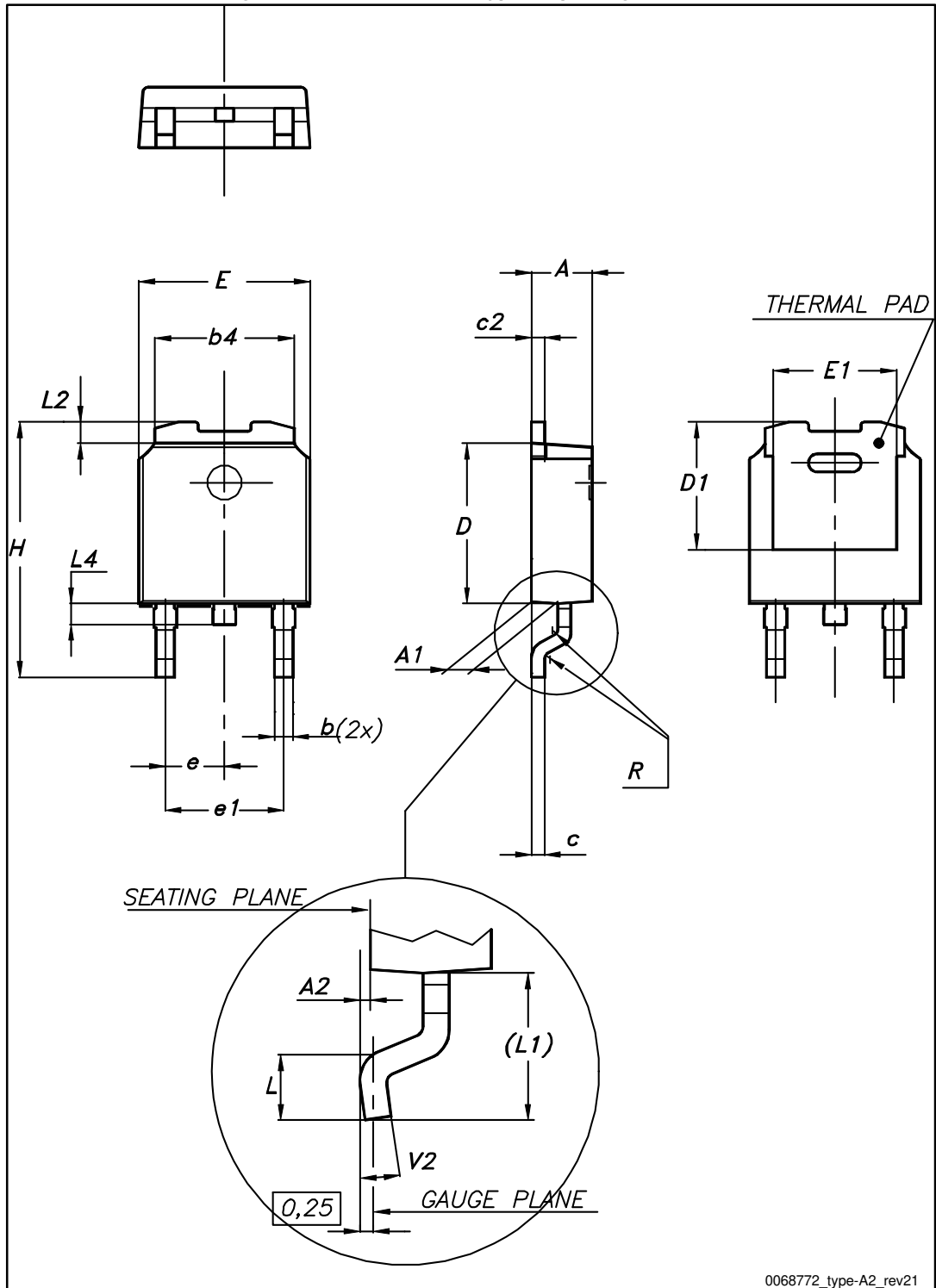
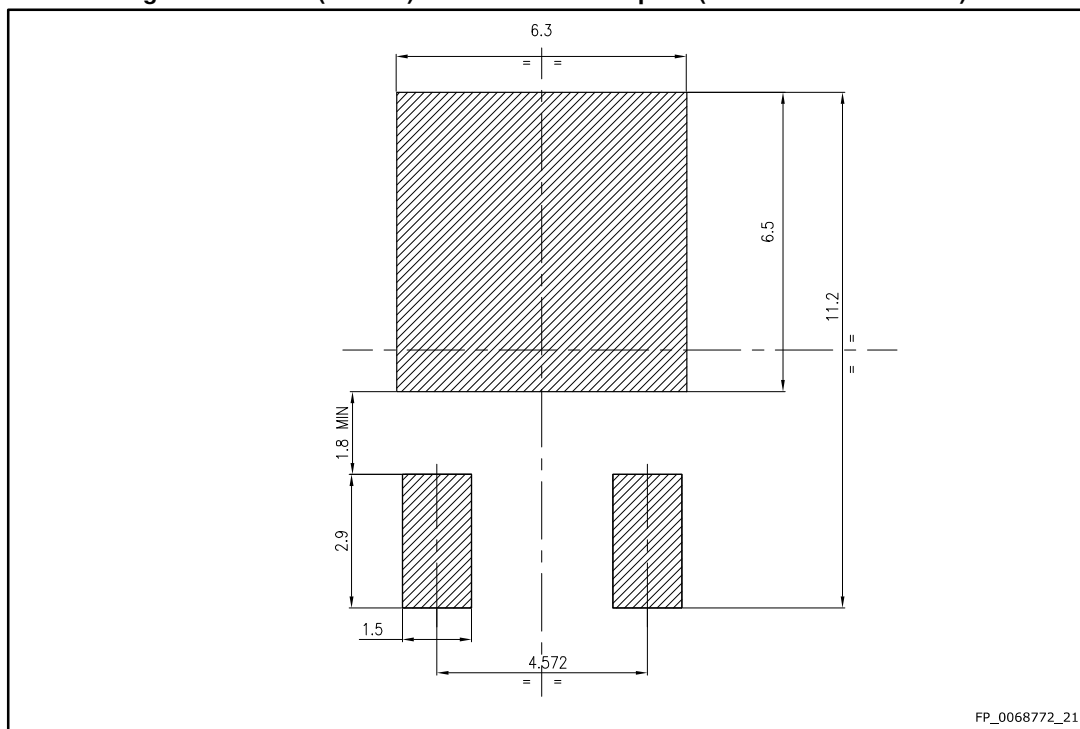


Table 9: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 22: DPAK (TO-252) tape outline

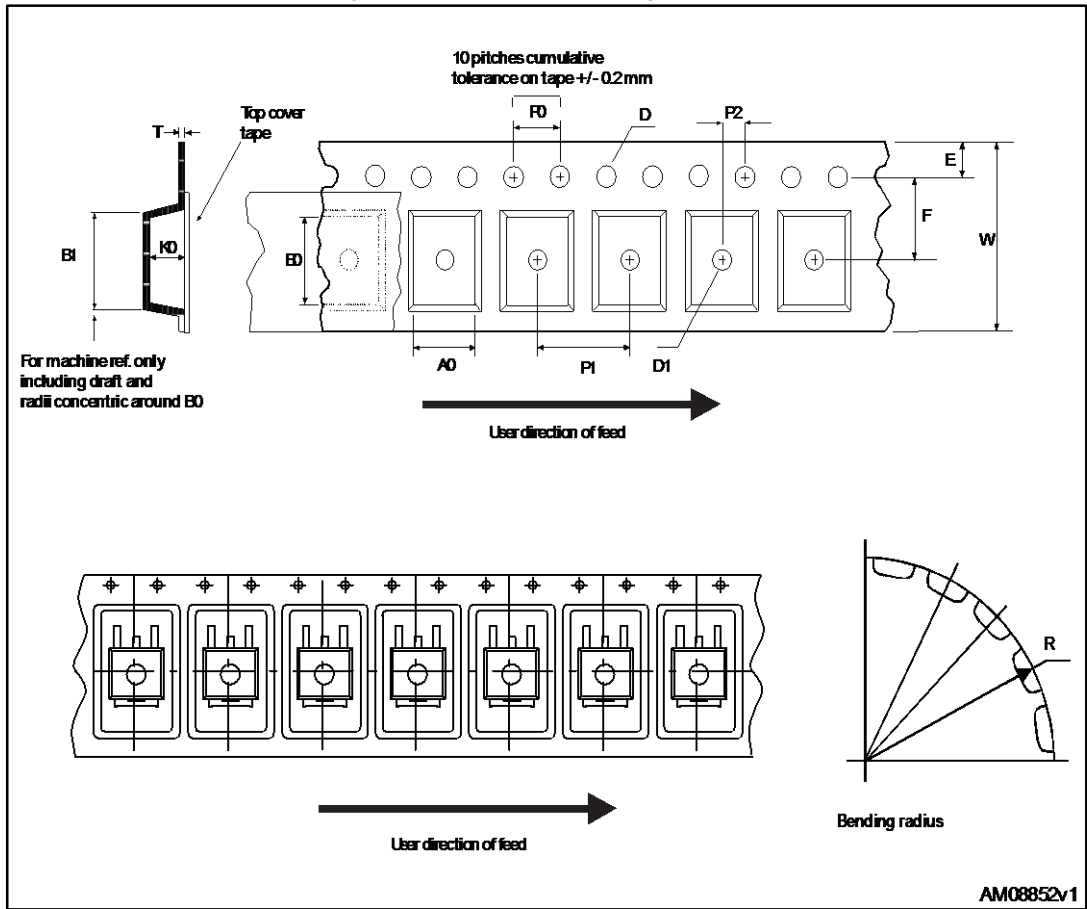
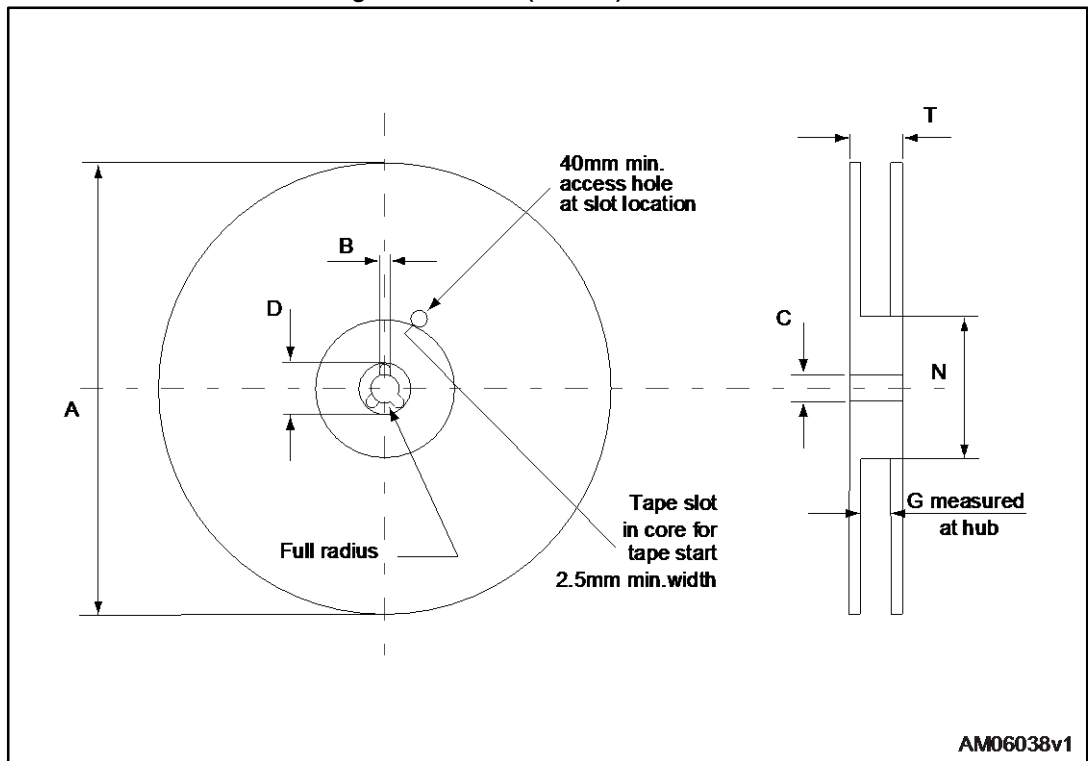


Figure 23: DPAK (TO-252) reel outline



AM06038v1

Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
26-Aug-2014	1	First release.
07-Mar-2016	2	Text and formatting changes throughout document In Section 1: "Electrical ratings" : - updated Table 4: "Avalanche characteristics" In Section 2: "Electrical characteristics" - updated Table 6: "Dynamic" , Table 7: "Switching times" and Table 8: "Source drain diode" Added Section 2.1: "Electrical characteristics (curves)" Updated Section 4: "Package information"

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