Power Amplifier Module for LTE and 5G

The AFSC5G37D37 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells, and low power remote radio heads. The field-proven LDMOS power amplifiers are designed for TDD and FDD LTE systems.

- Typical LTE Performance: P_{out} = 5.7 W Avg., V_{DD} = 29 Vdc, 1 × 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF.(1)

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3600 MHz	29.5	–32.3	39.3
3700 MHz	29.7	–33.6	38.8
3800 MHz	29.9	–34.4	37.6

1. All data measured with device soldered in NXP reference circuit.

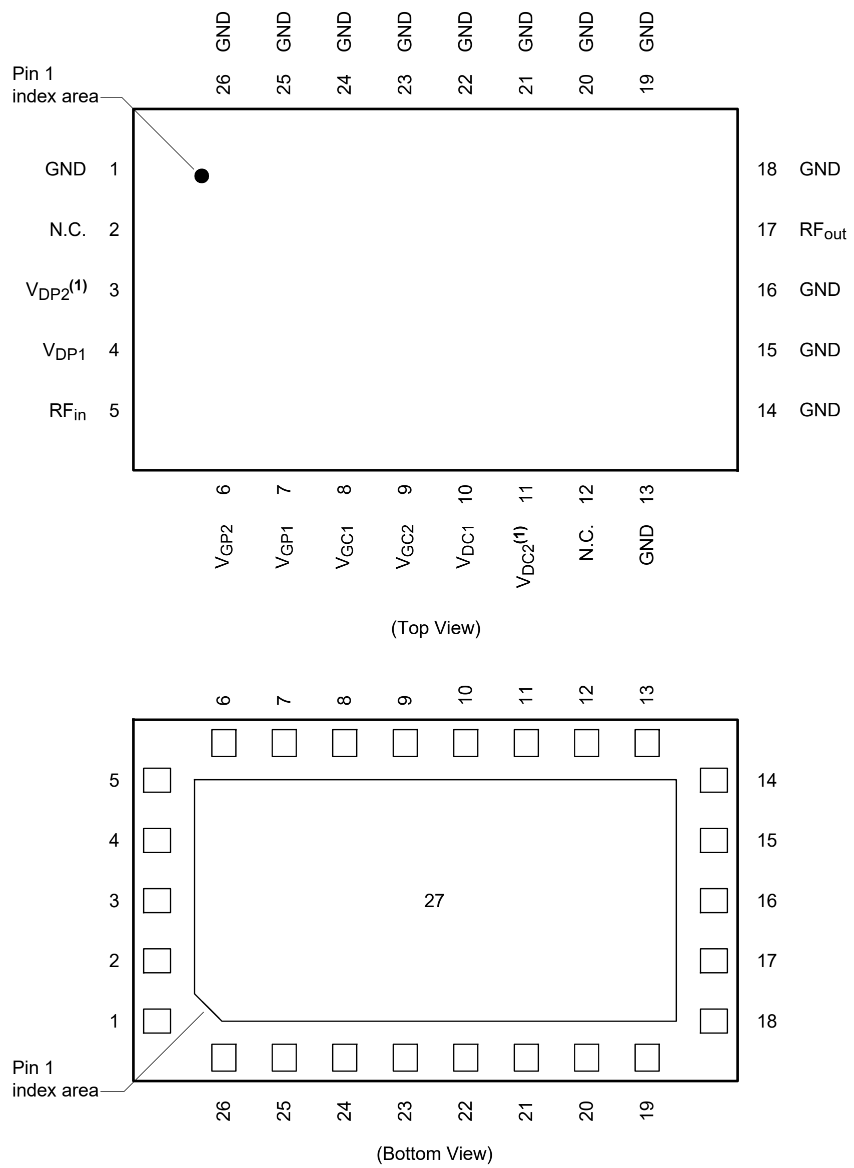
Features

- Frequency: 3600–3800 MHz
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity analog or digital linearization systems

AFSC5G37D37

3600–3800 MHz, 29 dB, 5.7 W Avg. AIRFAST POWER AMPLIFIER MODULE

10 mm × 6 mm Module



Note: Exposed backside of the package is DC and RF ground.

Figure 1. Pin Connections

1. V_{DP2} and V_{DC2} are DC coupled internal to the package and must be powered by a single DC power supply.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Gate-Bias Voltage Range	V_G	–0.5 to +10	Vdc
Operating Voltage Range	V_{DD}	0 to 32	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature	T_C	125	°C
Peak Input Power (3500 MHz, Pulsed CW, 10 μsec(on), 10% Duty Cycle)	P_{in}	30	dBm

Table 2. Lifetime

Characteristic	Symbol	Value	Unit
Mean Time to Failure Case Temperature 125°C, 5.7 W Avg., 32 Vdc	MTTF	> 10	Years

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1B
Charge Device Model (per JS-002-2014)	C3

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
Carrier Stage 1 — On Characteristics				
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 1.6 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 30 Vdc, I_{DQ1A} = 17.5 mAdc)	$V_{GS(Q)}$	1.45	±0.4	Vdc
Fixture Gate Quiescent Voltage [2] (V_{DD} = 30 Vdc, I_{DQ1A} = 17.5 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	5.2	±1.4	Vdc
Carrier Stage 2 — On Characteristics				
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 12.8 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 30 Vdc, I_{DQ2A} = 60.5 mAdc)	$V_{GS(Q)}$	1.6	±0.4	Vdc
Fixture Gate Quiescent Voltage [3] (V_{DD} = 30 Vdc, I_{DQ2A} = 60.5 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	3.1	±1.2	Vdc
Peaking Stage 1 — On Characteristics [1]				
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 2.4 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc
Peaking Stage 2 — On Characteristics [1]				
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 21.6 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc

1. Each side of device measured separately.
2. V_{GG} = 2.79 × $V_{GS(Q)}$. Parameter measured on NXP test fixture due to temperature compensation bias network on the board. Refer to reference circuit layout.
3. V_{GG} = 1.72 × $V_{GS(Q)}$. Parameter measured on NXP test fixture due to temperature compensation bias network on the board. Refer to reference circuit layout.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic		Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Doherty Production ATE (2) Test Fixture, 50 ohm system) V_{DD} = 30 Vdc, I_{DQ1A} = 17.5 mA, I_{DQ2A} = 60.5 mA, V_{GS1B} = (V_t + 0.07) (3) Vdc, V_{GS2B} = (V_t – 0.21) (3) Vdc, P_{out} = 5.7 W Avg., Two-tone CW, f1 = 3645 MHz, f2 = 3705 MHz, 60 MHz Tone Spacing.						
Gain		G	26.5	28.5	30.5	dB
Drain Efficiency		η_D	33.0	36.2	—	%
Intermodulation Distortion		IM3	—	–23.9	–16.3	dBc
P_{out} @ 3 dB Compression Point	f1 = 3550 MHz f2 = 3800 MHz	P3dB	42.9 43.8	44.3 44.3	— —	dBm
Wideband Ruggedness (4) (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) I_{DQ1A} = 17.5 mA, I_{DQ2A} = 60.5 mA, V_{GSP1} = 1.6 Vdc, V_{GSP2} = 1.4 Vdc, f = 3700 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR						
ISBW of 400 MHz at 32 Vdc, 14 W Avg. Modulated Output Power (6 dB Input Overdrive from 5.7 W Avg. Modulated Output Power)		No Device Degradation				
Typical Performance (4) (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) V_{DD} = 29 Vdc, I_{DQ1A} = 17.5 mA, I_{DQ2A} = 60.5 mA, V_{GSP1} = 1.6 Vdc, V_{GSP2} = 1.4 Vdc, P_{out} = 5.7 W Avg., 3700 MHz						
VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)		VBW_{res}	—	200	—	MHz
Quiescent Current Accuracy over Temperature (5) with 2.2 kΩ Gate Feed Resistors (–40 to 85°C) Stage 1 with 2.2 kΩ Gate Feed Resistors (–40 to 85°C) Stage 2		ΔI_{QT}	 — —	 1.0 2.0	 — —	%
1-carrier 20 MHz LTE, 8 dB Input Signal PAR						
Gain		G	—	29.7	—	dB
Power Added Efficiency		PAE	—	38.8	—	%
Adjacent Channel Power Ratio		ACPR	—	–33.6	—	dBc
Adjacent Channel Power Ratio		ALT1	—	–42.9	—	dBc
Adjacent Channel Power Ratio		ALT2	—	–51.2	—	dBc
Output Peak-to-Average Ratio @ 0.01% Probability		PAR	—	7.7	—	dB
Gain Flatness (6)		G_F	—	0.3	—	dB
Fast CW, 27 ms Sweep						
P_{out} @ 3 dB Compression Point		P3dB	—	44.7	—	dBm
AM/PM @ P3dB		Φ	—	–27	—	°

Table 6. Ordering Information

Device	Tape and Reel Information	Package
AFSC5G37D37T2	T2 Suffix = 2,000 Units, 24 mm Tape Width, 13-inch Reel	10 mm × 6 mm Module

1. Part input and output matched to 50 ohms.
2. ATE is a socketed test environment.
3. Refer to AN12071, *Doherty Biasing Methodology for Volume Production*.
4. All data measured in fixture with device soldered in NXP reference circuit.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
6. Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High}))

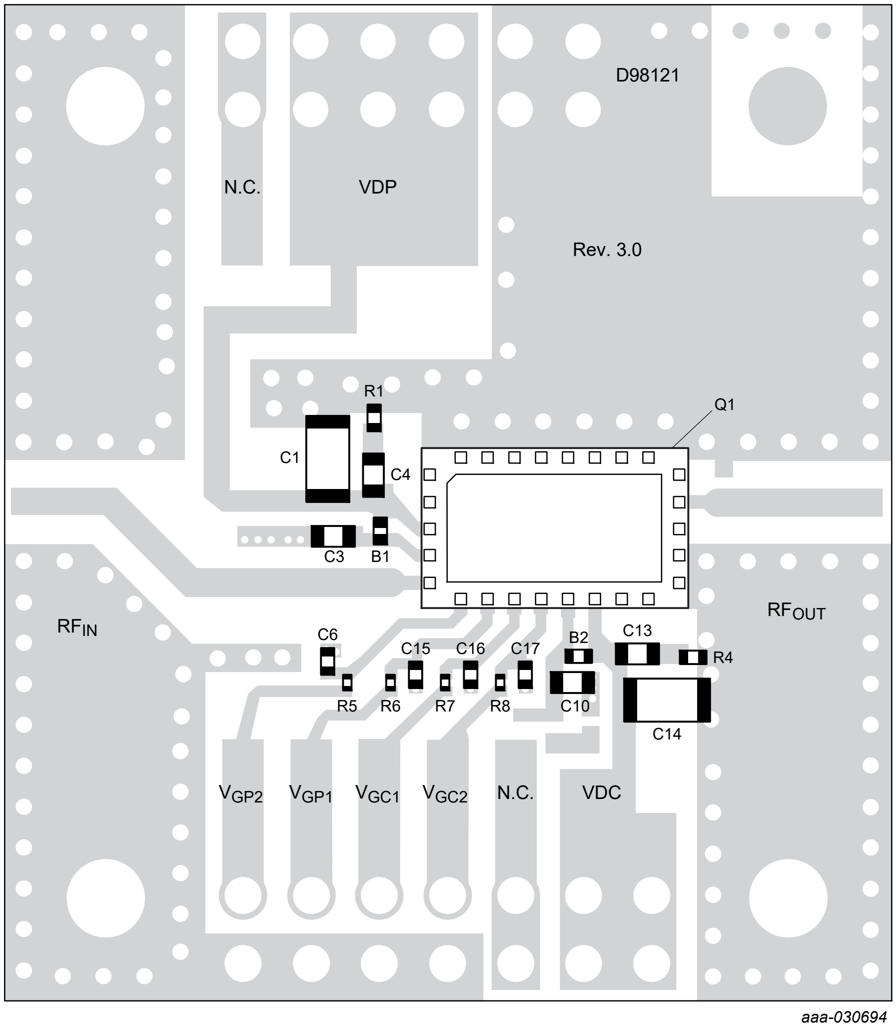


Figure 2. AFSC5G37D37 Reference Circuit Component Layout

Table 7. AFSC5G37D37 Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1, B2	30 Ω Ferrite Bead	BLM15PD300SN1	Murata
C1, C14	10 μF Chip Capacitor	CL31A106KBHNNNE	Samsung
C3, C4, C10, C13	1 μF Chip Capacitor	06035D105KAT2A	AVX
C6, C15, C16, C17	0.1 μF Chip Capacitor	GRM155R61H104KE14	Murata
Q1	Power Amplifier Module	AFSC5G37D37	NXP
R1, R4	5.1 Ω, 1/10 W Chip Resistor	ERJ-2GEJ5R1X	Panasonic
R5, R6, R7, R8	2.2 kΩ, 1/20 W Chip Resistor	ERJ-1GEJ222C	Panasonic
PCB	Rogers RO4350B, 0.020″, ε_r = 3.67	D98121	MTL

Note: Component numbers C2, C5, C7, C8, C9, C11, C12, R2 and R3 are intentionally omitted.

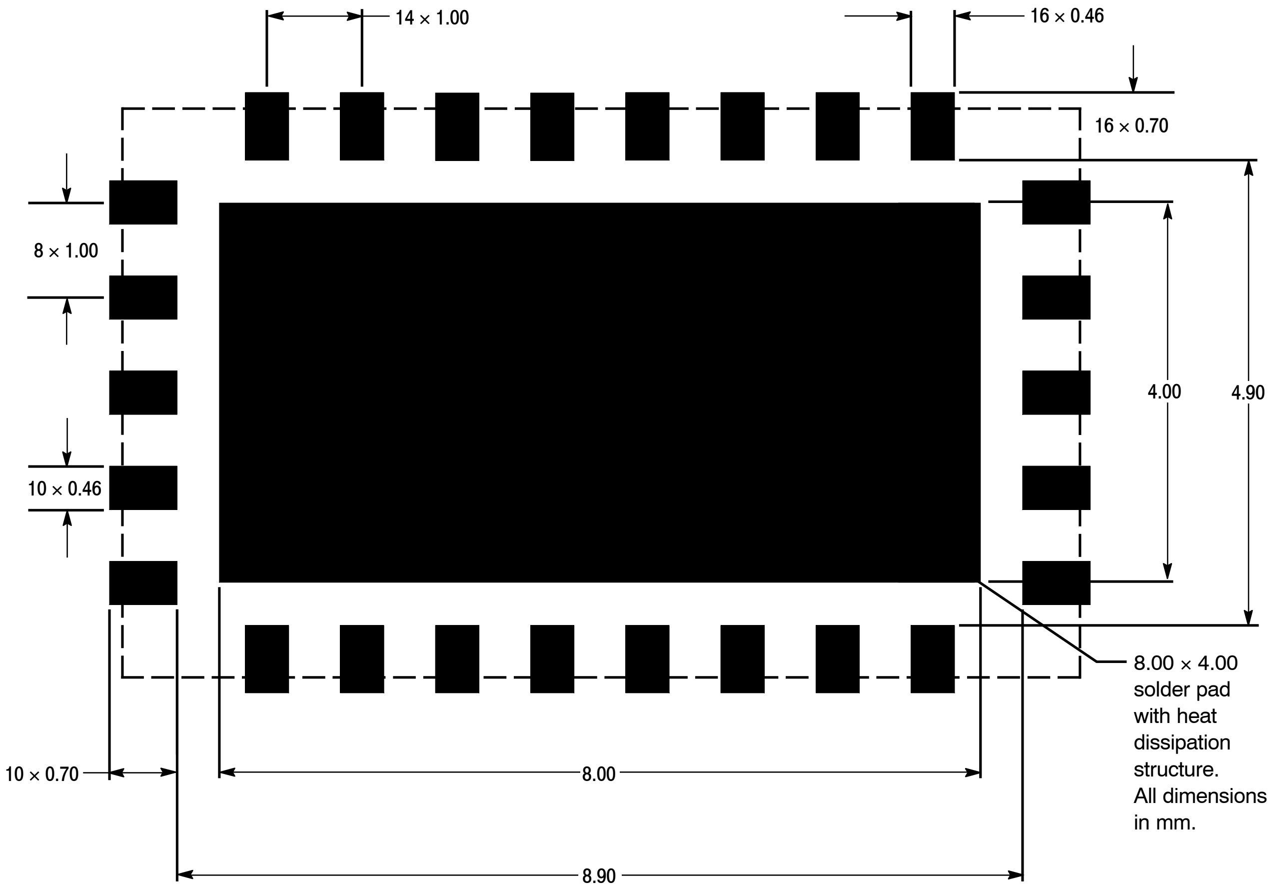


Figure 3. PCB Pad Layout for 10 mm × 6 mm Module

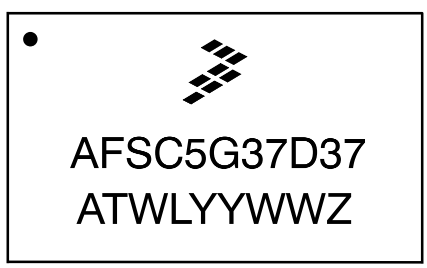
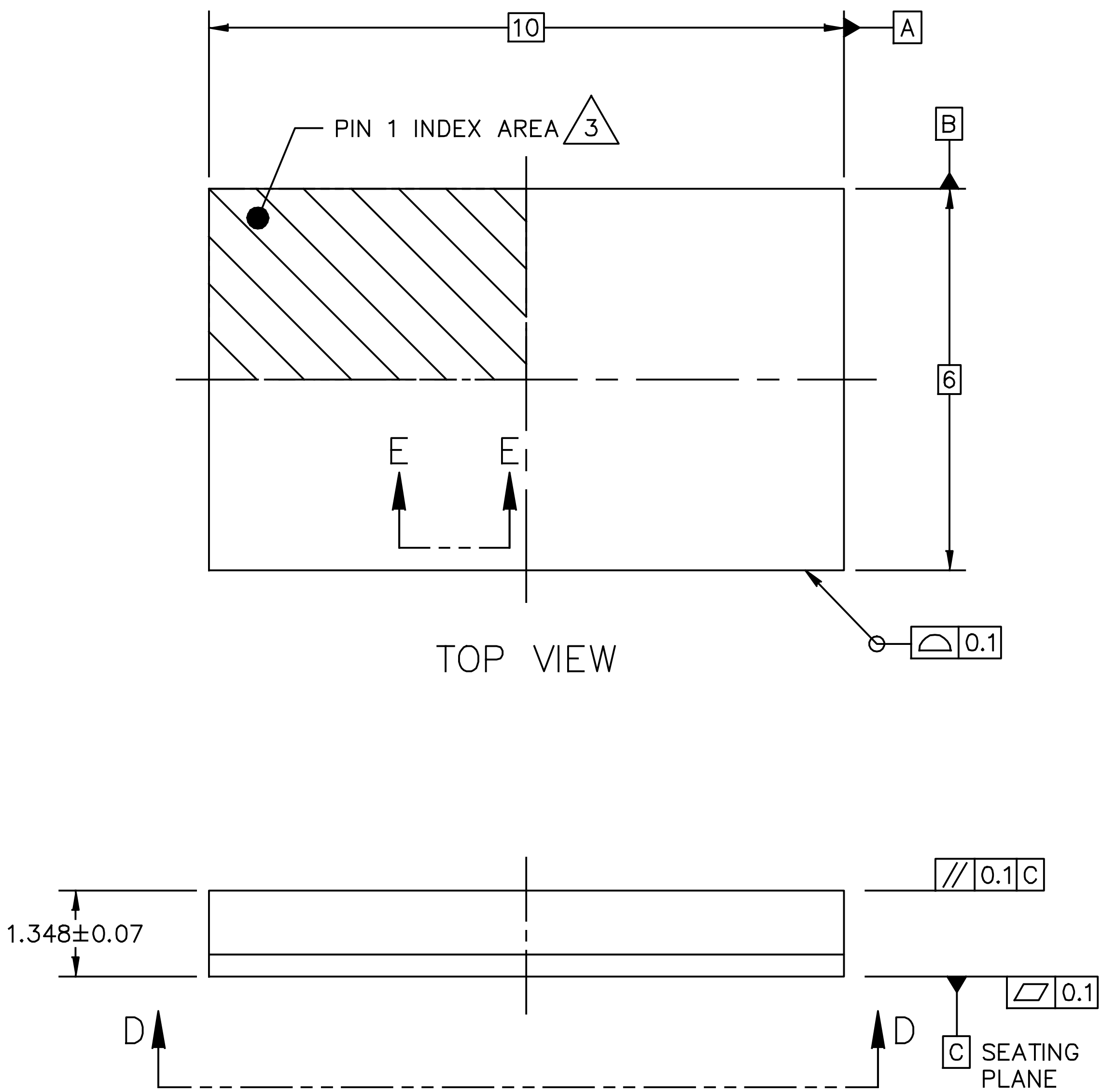


Figure 4. Product Marking



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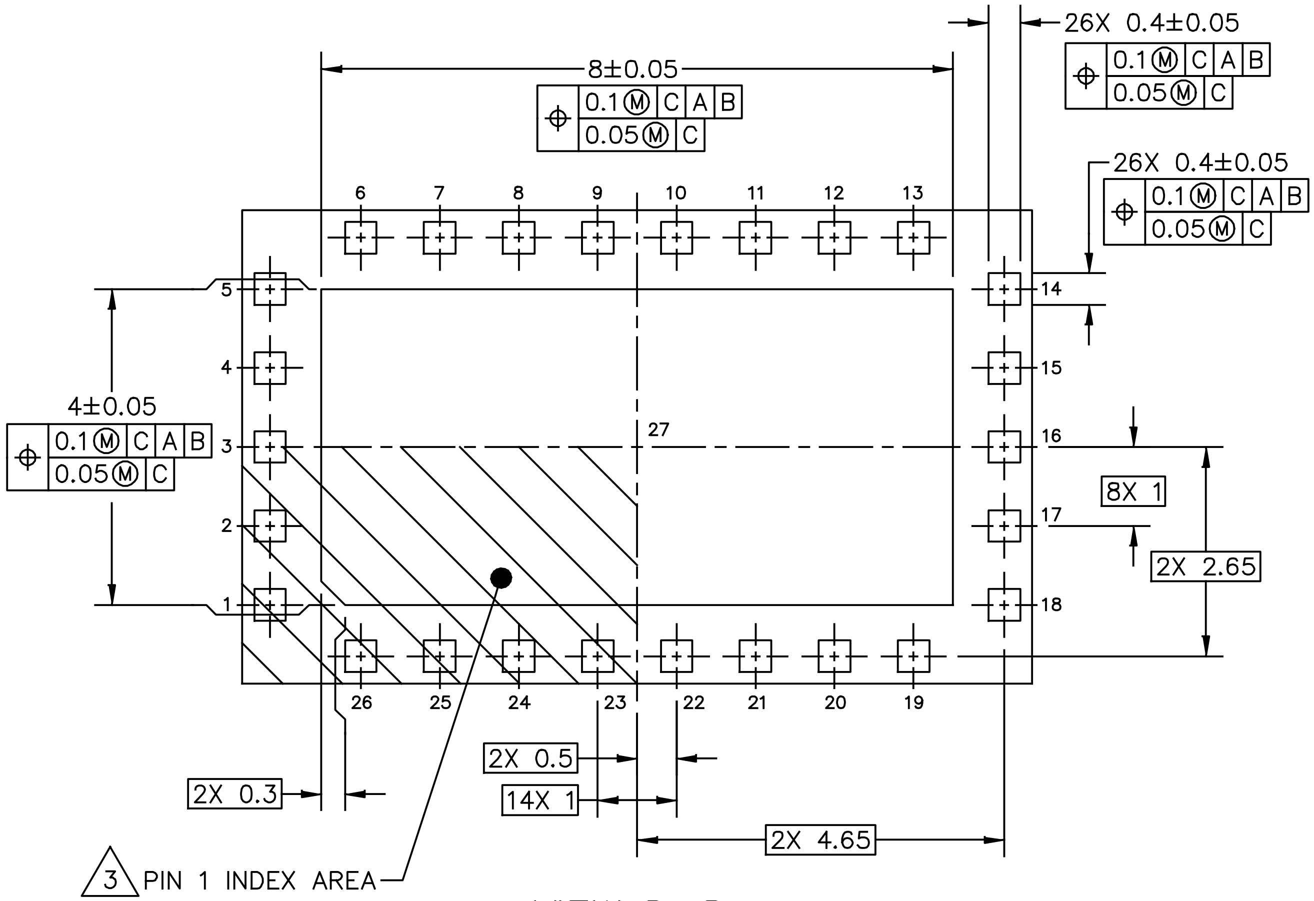
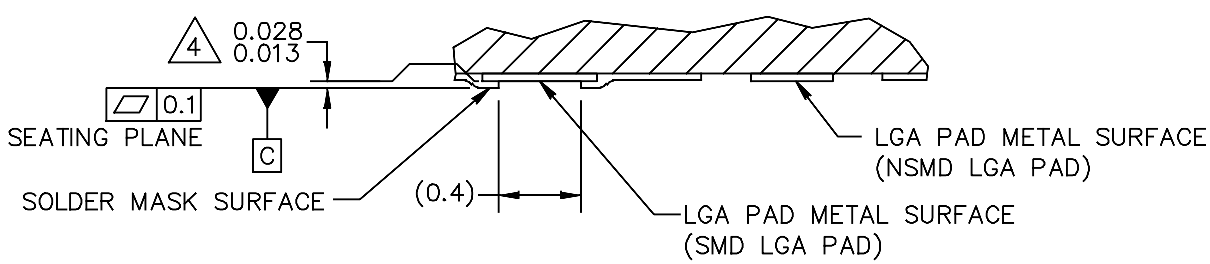
TITLE: WBMOD, 10 X 6 X 1.348 PKG, 1 MM PITCH, 27 I/O	DOCUMENT NO: 98ASA00953D	REV: A
	STANDARD: NON-JEDEC	
	SOT1831-1	20 JUL 2017



VIEW D–D
(BOTTOM VIEW)



SECTION E–E 5

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
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	STANDARD: NON–JEDEC	
	SOT1831–1	20 JUL 2017

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.
3. (△) PIN 1 CONFIGURATION MAY VARY.
4. (△) DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. (△) THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON—SOLDERMASK DEFINED (NSMD).

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: WBMOD, 10 X 6 X 1.348 PKG, 1 MM PITCH, 27 I/O	DOCUMENT NO: 98ASA00953D	REV: A
	STANDARD: NON—JEDEC	
	SOT1831—1	25 JUL 2017

PRODUCT DOCUMENTATION AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN12071: Doherty Biasing Methodology for Volume Production

Development Tools

- Printed Circuit Boards

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2019	• Initial release of data sheet

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