To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HAT2199R

Silicon N Channel Power MOS FET
Power Switching

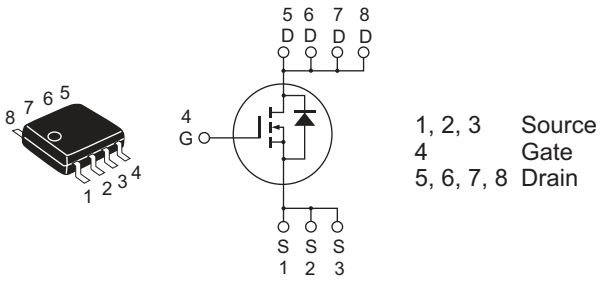
REJ03G0063-0300
Rev.3.00
Sep.23.2004

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 13.0 mΩ typ. (at V_{GS} = 10 V)

Outline

SOP-8



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	11	A
Drain peak current	$I_{D(pulse)}$ Note1	88	A
Body-drain diode reverse drain current	I_{DR}	11	A
Avalanche current	I_{AP} Note 2	11	A
Avalanche energy	E_{AR} Note 2	12.1	mJ
Channel dissipation	Pch Note3	2.0	W
Channel to ambient thermal impedance	θch-a Note3	62.5	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 ∝s, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics

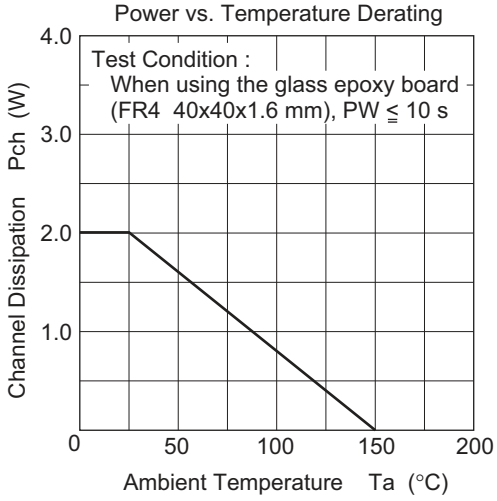
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	∝A	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	∝A	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	13.0	16.5	mΩ	I_D = 5.5 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	17.0	25.0	mΩ	I_D = 5.5 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	12	20	—	S	I_D = 5.5 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	1060	—	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	255	—	pF	
Reverse transfer capacitance	Crss	—	85	—	pF	
Gate Resistance	Rg	—	1.5	—	Ω	
Total gate charge	Qg	—	7.5	—	nC	V_{DD} = 10 V V_{GS} = 4.5 V I_D = 11 A
Gate to source charge	Qgs	—	3.1	—	nC	
Gate to drain charge	Qgd	—	1.8	—	nC	
Turn-on delay time	$t_{d(on)}$	—	8.0	—	ns	V_{GS} = 10 V, I_D = 5.5 A V_{DD} ≅ 10 V R_L = 1.81 Ω Rg = 4.7 Ω
Rise time	t_r	—	16	—	ns	
Turn-off delay time	$t_{d(off)}$	—	37	—	ns	
Fall time	t_f	—	3.6	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.84	1.10	V	IF = 11 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	18	—	ns	IF = 11 A, V_{GS} = 0 diF/ dt = 100 A/ ∝s

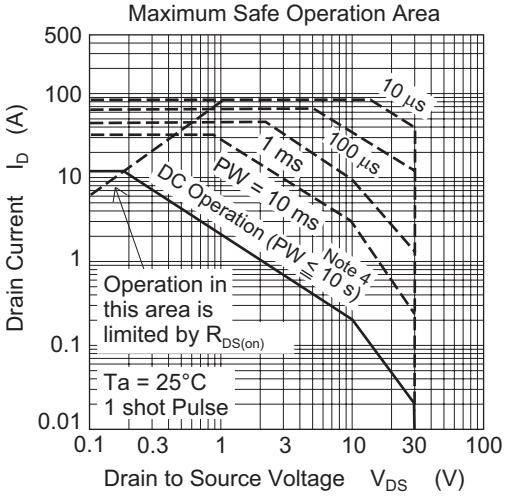
Notes: 4. Pulse test

Main Characteristics

Power vs. Temperature Derating

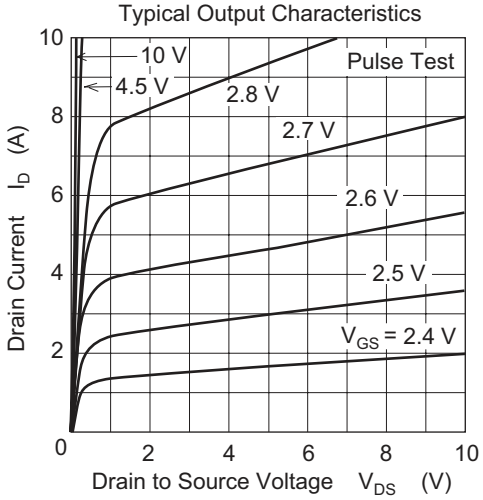


Maximum Safe Operation Area

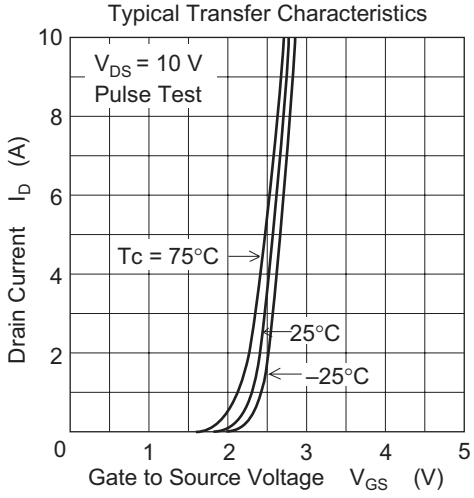


Note 4 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

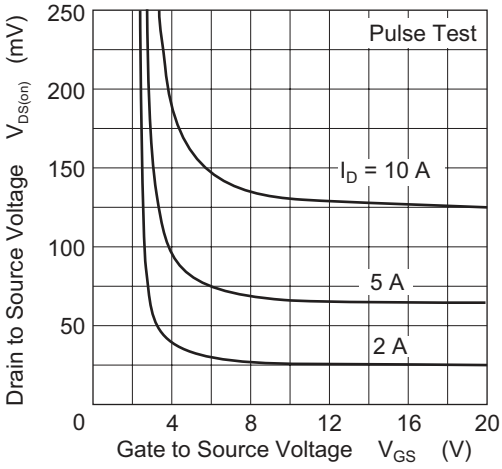
Typical Output Characteristics



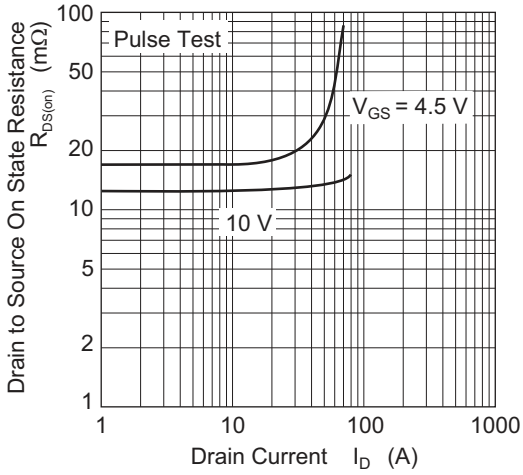
Typical Transfer Characteristics



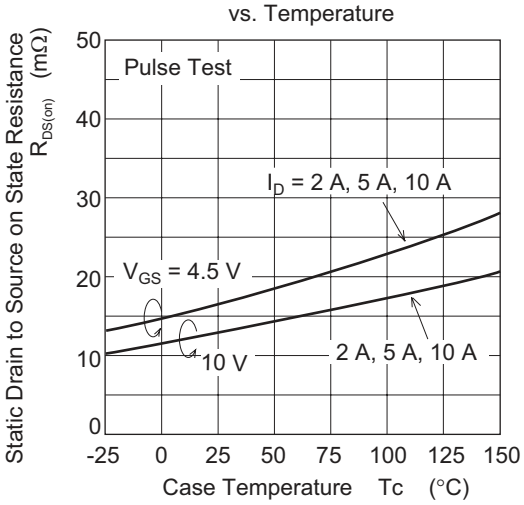
Drain to Source Saturation Voltage vs. Gate to Source Voltage



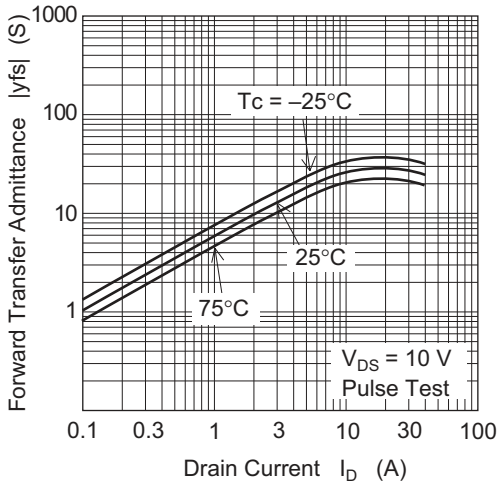
Static Drain to Source on State Resistance vs. Drain Current



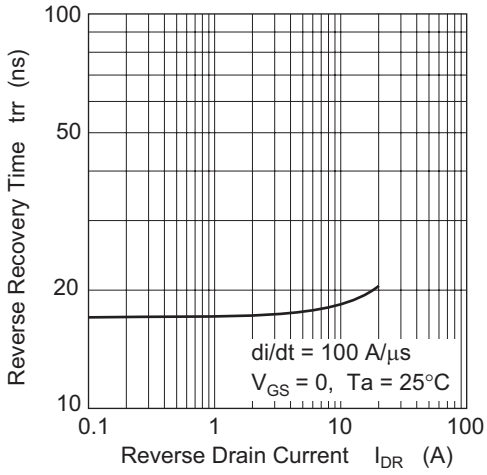
Static Drain to Source on State Resistance vs. Temperature



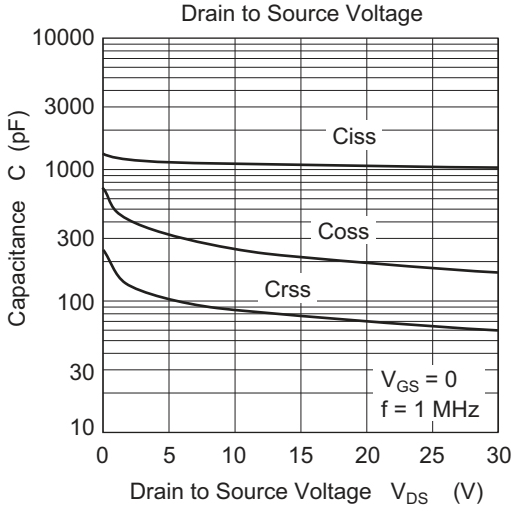
Forward Transfer Admittance vs. Drain Current



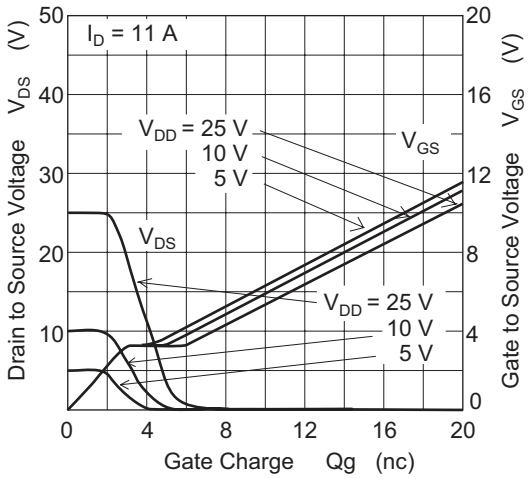
Body–Drain Diode Reverse Recovery Time



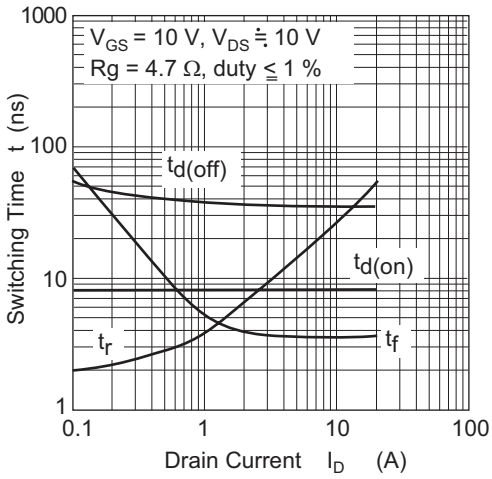
Typical Capacitance vs. Drain to Source Voltage



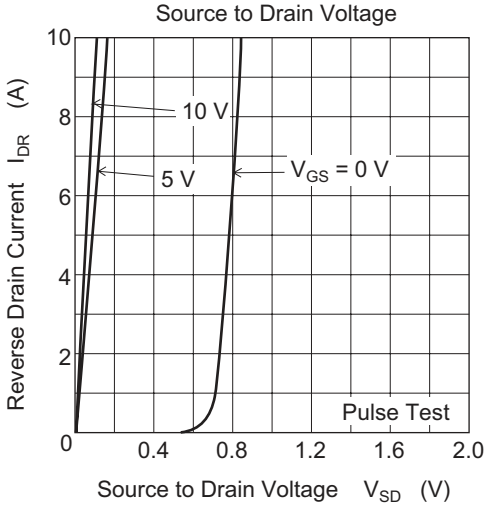
Dynamic Input Characteristics



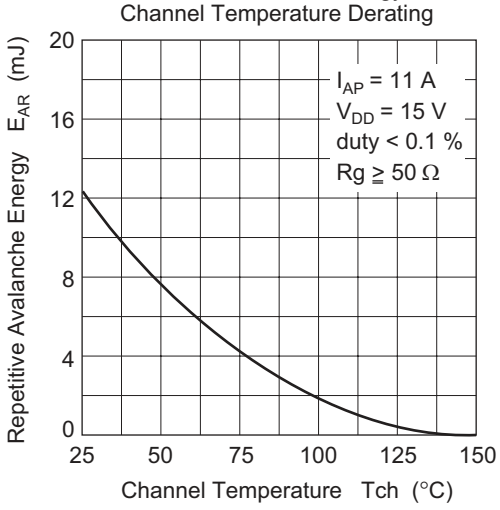
Switching Characteristics



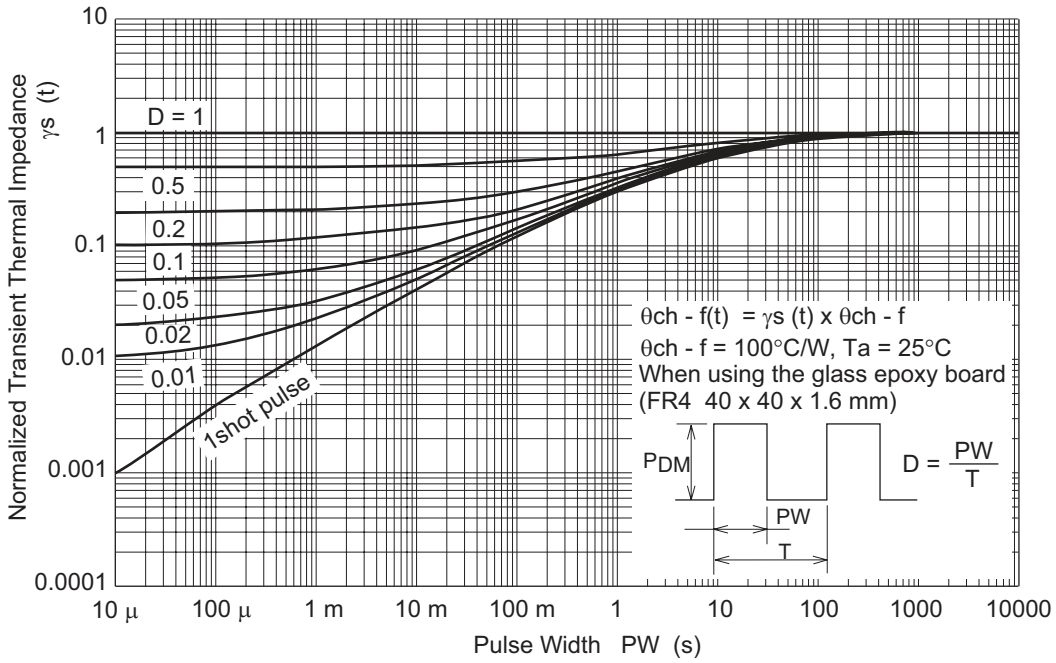
Reverse Drain Current vs.
Source to Drain Voltage



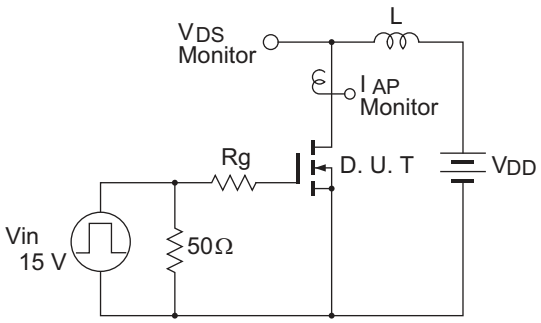
Maximum Avalanche Energy vs.
Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

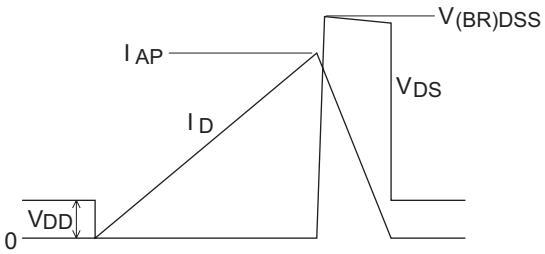


Avalanche Test Circuit

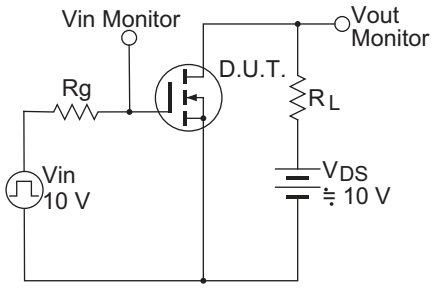


Avalanche Waveform

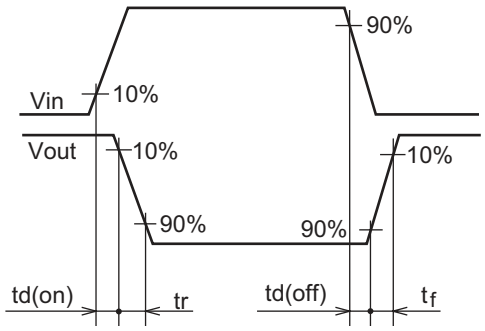
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



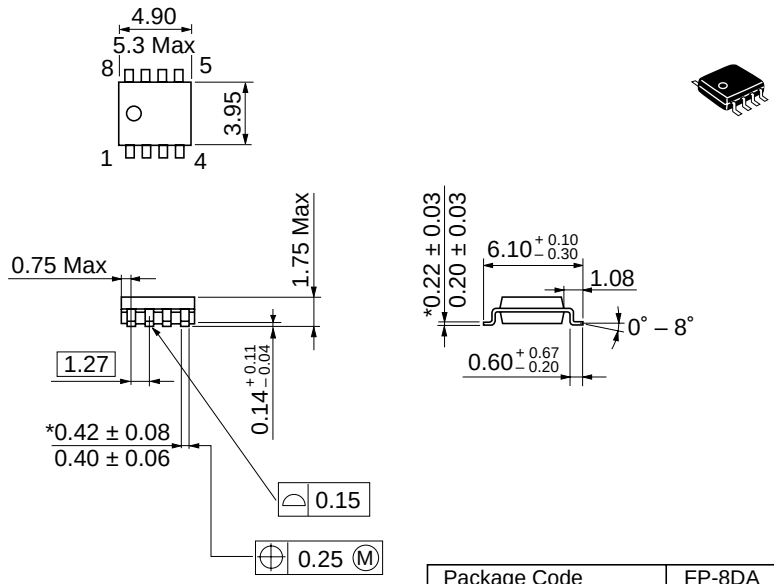
Switching Time Waveform



Package Dimensions

As of January, 2003

Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

Ordering Information

Part Name	Quantity	Shipping Container
HAT2199R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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