

DESCRIPTION

The MP6402 is a dual-channel, high PSRR linear regulator with reset function.

The outputs range from 0.9V and 3.3V with $\pm 1.5\%$ voltage accuracy at both channels by operating from a +2.5V to +5.5V input. OUT2 pin voltage is recommended to be higher than OUT1 pin voltage. Short circuit protection and thermal protection are built in to prevent damage caused by output short circuit and overloading, respectively.

A reset circuit is designed to monitor output voltage of channel 2. The $\overline{\text{RESET}}$ becomes active (low) when OUT2 pin voltage drops below its threshold. To ensure that a complete reset occurs, the $\overline{\text{RESET}}$ remains active for a pre-set delay time. The delay time is programmable by the user through changing the external capacitor. The MP6402 is available in SOIC8E and 3x3mm TQFN8 packages and is specified for operation T_j from -40°C to $+125^\circ\text{C}$.

FEATURES

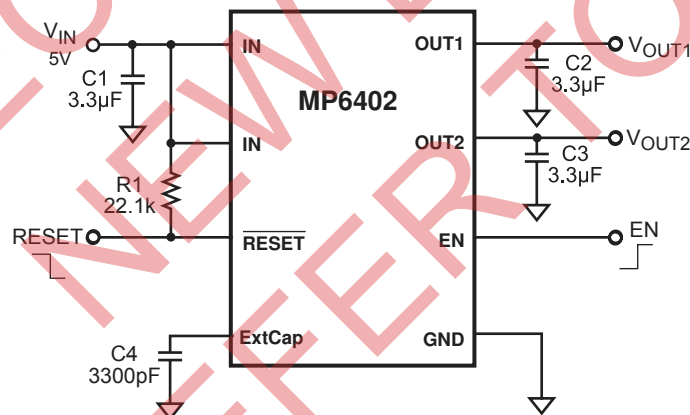
- Up to 500mA Output Current
- High Output Voltage Accuracy ($\pm 1.5\%$)
- High Reset Voltage Accuracy ($\pm 3\%$)
- Programmable Reset Delay Time
- High PSRR: 60dB at 100Hz
- $15\mu\text{V}_{\text{RMS}}$ Low Noise Outputs
- Built-in Short Circuit Protection
- Built-in Thermal Protection
- Output Discharge
- SOIC8E and 3x3mm TQFN8

APPLICATIONS

- Consumer electronics
- Blu-ray
- Portable GPS Devices
- Wireless Devices

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	Junction Air Temperature (T _J)
MP6402DN-EF-LF-Z*	SOIC8E	6402DNEF	-40°C to +125°C
MP6402DQT-EF-LF-Z**	TQFN8 (3x3mm)	9X	-40°C to +125°C

* For Tape & Reel, add suffix -Z (e.g. MP6402DN-Z);
For RoHS compliant packaging, add suffix -LF (e.g. MP6402DN-LF-Z).

** For Tape & Reel, add suffix -Z (e.g. MP6402DQT-Z);
For RoHS compliant packaging, add suffix -LF (e.g. MP6402DQT-LF-Z).

ORDERING GUIDE***

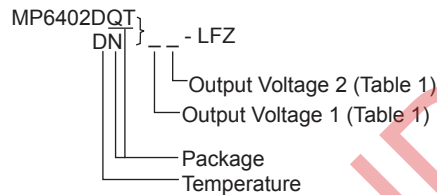


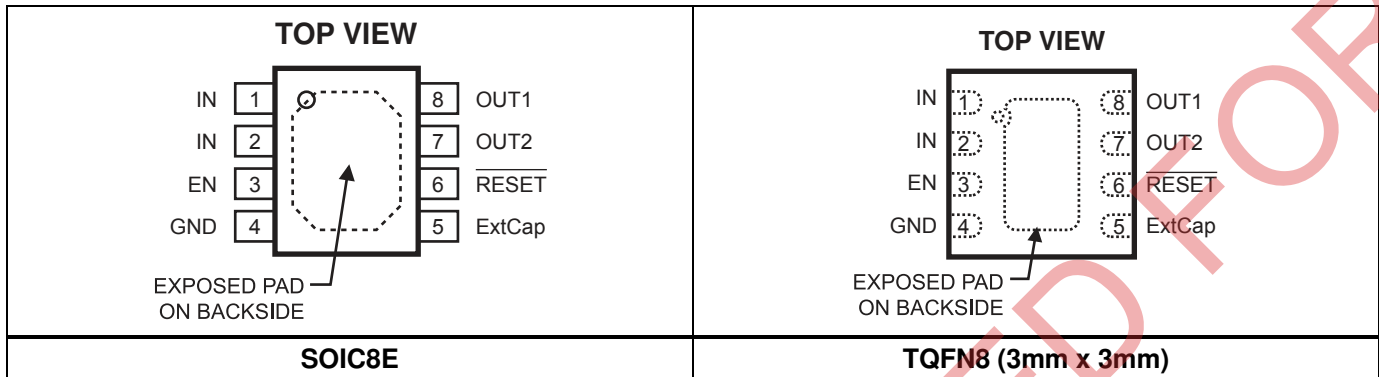
Table 1 — Output Voltage Selector Guide

Code	V _{OUT1}	V _{OUT2}
A	0.9	--
B	1.05	--
C	1.2	--
D	1.3	1.3
E	1.8	1.8
F	2.5	2.5
G	2.8	2.8
H	--	3.3

*** Code in Bold are standard versions. For other output voltage between 0.9V to 3.3V contact factory for availability.

Minimum order quantity on no-standard version in 25,000 units.

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN	-0.3V to 6V
RESET	-0.3V to 6V
All Other Pins	-0.3V to +6V
Continuous Power Dissipation. (T_A = +25°C) ⁽²⁾	
SOIC8E	2.2W
TQFN8 (3mm x 3mm)	2.6W
Storage Temperature Range	-55°C to 150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10sec)	260°C

Recommended Operating Conditions ⁽³⁾

Input Voltage V _{IN}	2.5V to 5.5V
Operating Junct. Temp (T _J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}	
SOIC8E	55	12	°C/W
TQFN8 (3mm x 3mm)	48	11	°C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX) = (T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=150°C(TYP) and disengages at T_J=130°C(TYP)
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = V_{OUT2} + 0.5V$ or $2.5V$ for each LDO. Typical Value at $T_A = +25^\circ C$ unless otherwise noted.

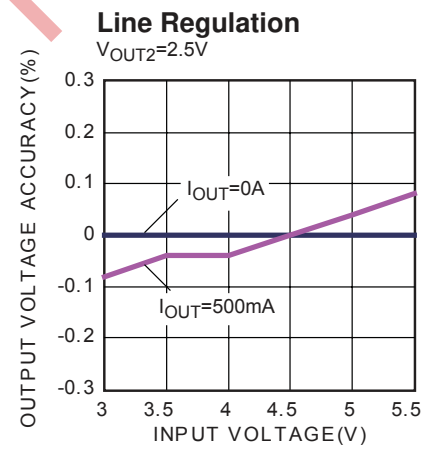
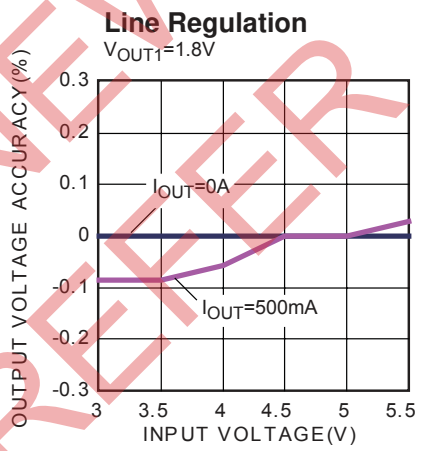
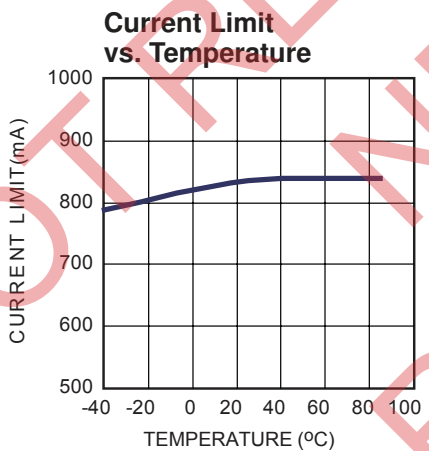
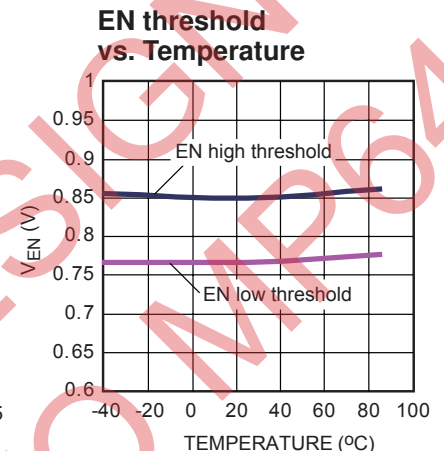
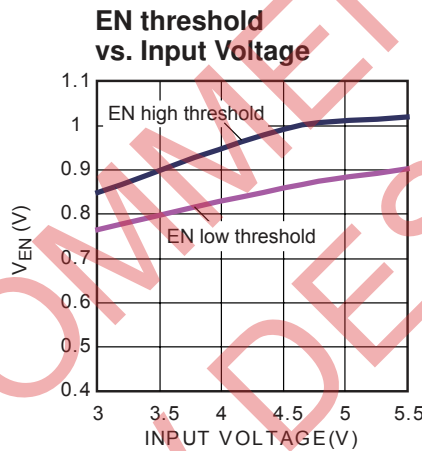
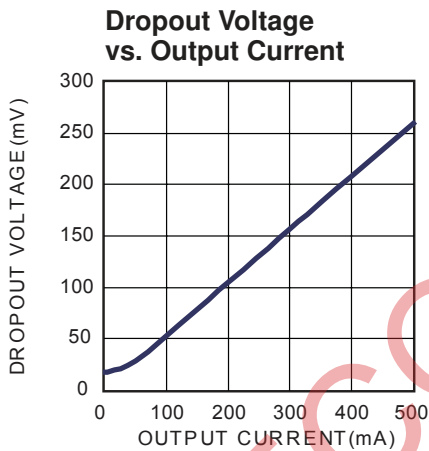
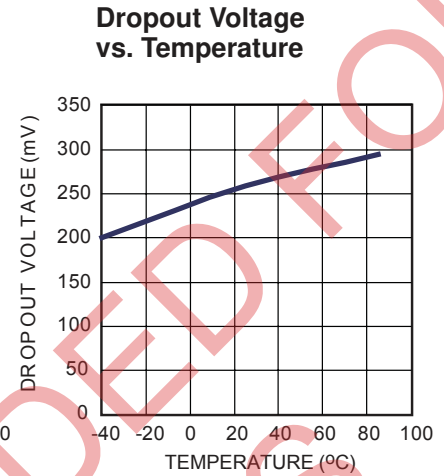
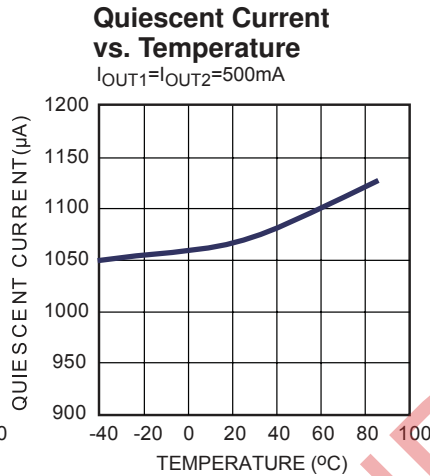
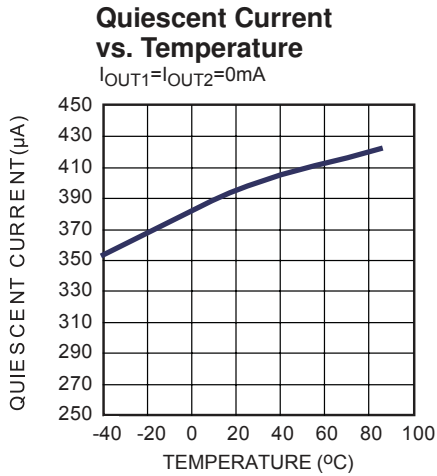
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Quiescent Current (ON)	I_q	EN activate without load		0.4	0.58	mA
Quiescent Current (OFF)	I_{qEBL}	EN deactivate		17	36	μA
Output Voltage Range	V_{OUT}		0.9		3.3	V
Dropout Voltage	V_{DROP}	$I_{OUT} = 500mA$		260		mV
Output Voltage Accuracy		$I_{OUT} = 10mA$	-1.5		1.5	%
		$I_{OUT} = 10mA, T_A = -40^\circ C$ to $85^\circ C$	-2.3		2.3	%
Output Current Limit	I_{LIM}		550			mA
Short Circuit Current	I_{ST}	OUT short to GND		200		mA
Load Regulation	ΔV_{OUT1}	$V_{IN} = (V_{OUT1} + 0.5V$ or $2.5V)$, $I_{OUT1} = 1mA$ to $500mA$			45	mV
	ΔV_{OUT2}	$V_{IN} = (V_{OUT2} + 0.5V$ or $2.5V)$, $I_{OUT2} = 1mA$ to $500mA$			50	mV
Line Regulation	ΔV_{LINE1}	$V_{IN} = (V_{OUT1} + 0.5V$ or $2.5V)$ to $5.5V$, $I_{OUT1} = 10mA$		0.05	0.1	%/V
	ΔV_{LINE2}	$V_{IN} = (V_{OUT2} + 0.5V$ or $2.5V)$ to $5.5V$, $I_{OUT2} = 10mA$		0.05	0.1	%/V
PSRR	$V_{OUT1} = 1.8V$	PSR	$f = 100Hz, I_{OUT1} = 100mA$		60	dB
	$V_{OUT2} = 2.5V$	PSR2	$f = 100Hz, I_{OUT2} = 100mA$		51	dB
Output Voltage Noise		$100Hz$ to $80kHz$, $C_{OUT} = 3.3\mu F, I_{OUT} = 10mA$		15		μV_{RMS}
RESET OUT						
Reset Delay Time	RSTDLY	$V_{IN} = V_{OUT2} + 0.5V$, ExtCap=3300pF	1.4	2.1	2.8	ms
Reset Voltage	RSTVOL	V_{IN} falling		92.5		% V_{OUT2}
Reset Hysteresis	ΔV_{HYS}			2		% V_{OUT2}
Reset Voltage Accuracy			-3		3	%
Reset Low Level Voltage	RSTLOW	$I_{IN} = 2mA$		0.2		V
EN Input High Voltage			1.5			V
EN Input High Voltage					0.6	V

PIN FUNCTIONS

Pin #	Name	Description
1	IN	Power supply input pin.
2	IN	Power supply input pin.
3	EN	Enable (Active High). Connect EN to IN generally. Don't float EN pin.
4	GND	Ground.
5	ExtCap	Reset delay time set external capacitor connect pin.
6	RESET	Reset signal output pin.
7	OUT2	Channel 2 LDO output pin.
8	OUT1	Channel 1 LDO output pin.

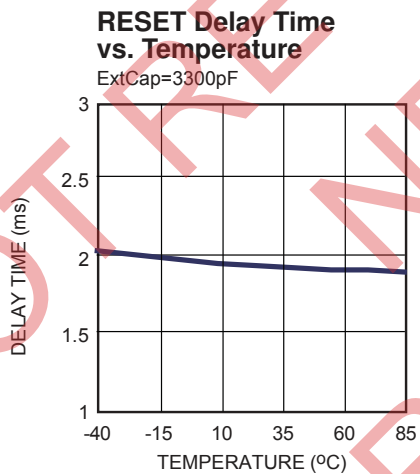
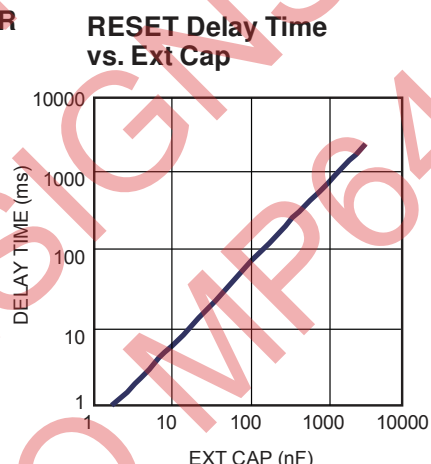
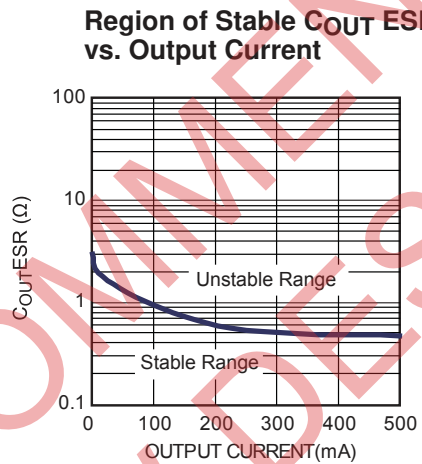
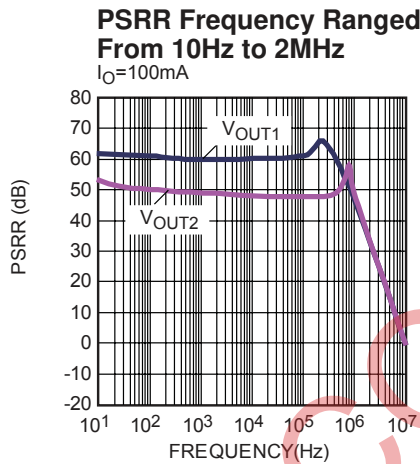
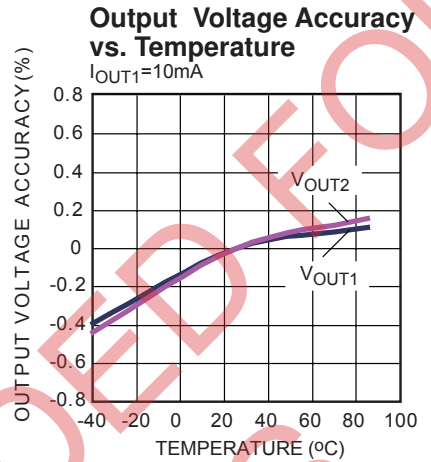
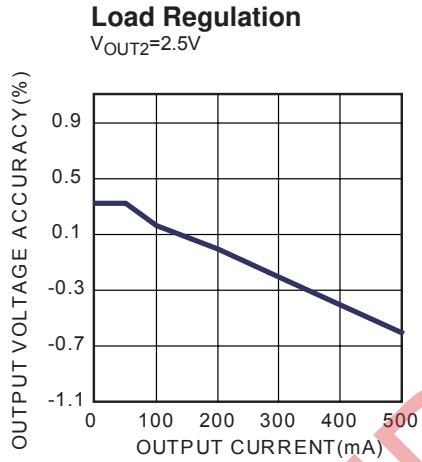
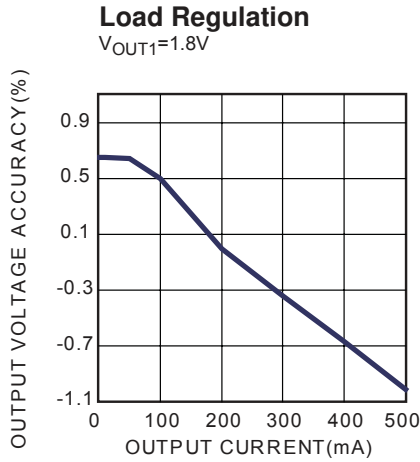
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 3V$, $V_{OUT1}=1.8V$, $V_{OUT2}=2.5V$, $C_{IN} = C_{OUT1} = C_{OUT2}=3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3V$, $V_{OUT1}=1.8V$, $V_{OUT2}=2.5V$, $C_{IN} = C_{OUT1} = C_{OUT2}=3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

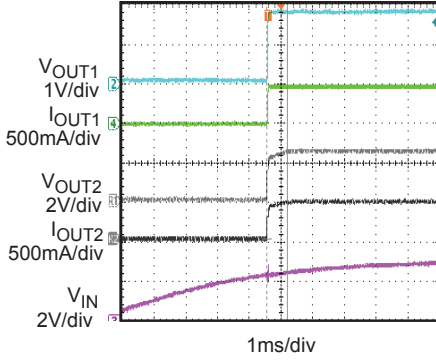


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 2.5V$, $C_{IN} = C_{OUT1} = C_{OUT2} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

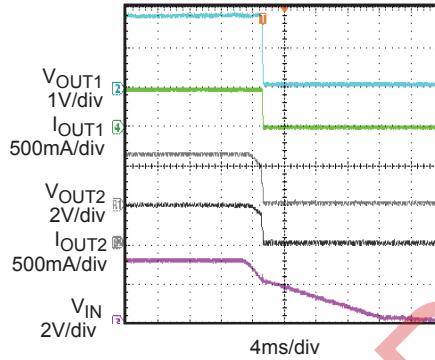
Input Power Start Up

$I_{OUT1} = I_{OUT2} = 500mA$
with Resistor Load



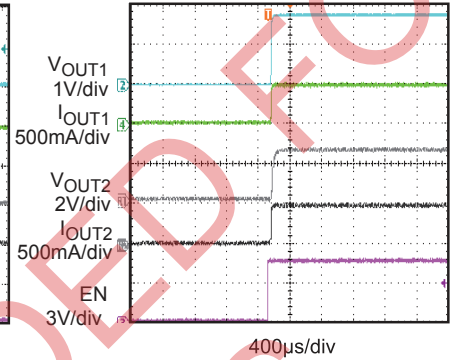
Input Power Shutdown

$I_{OUT1} = I_{OUT2} = 500mA$
with Resistor Load



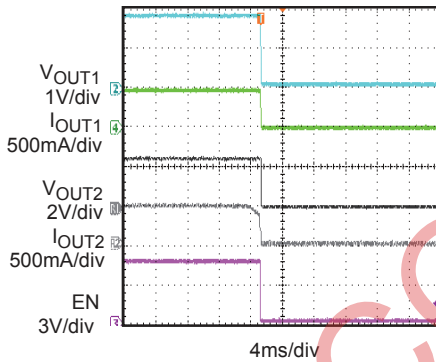
EN Start Up

$I_{OUT1} = I_{OUT2} = 500mA$
with Resistor Load



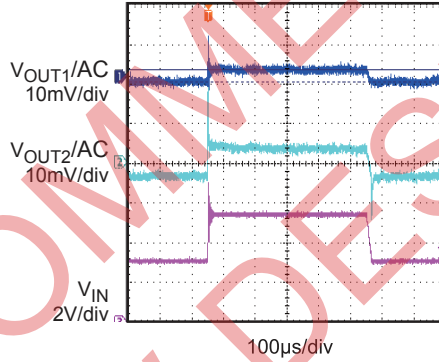
EN Shutdown

$I_{OUT1} = I_{OUT2} = 500mA$
with Resistor Load



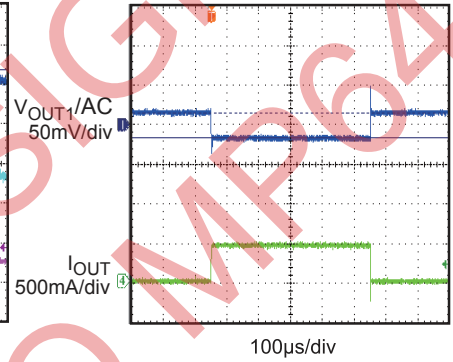
Line Transient

$V_{IN} = 3V$ to $5.5V$, $I_{OUT} = 500mA$
with Resistor Load



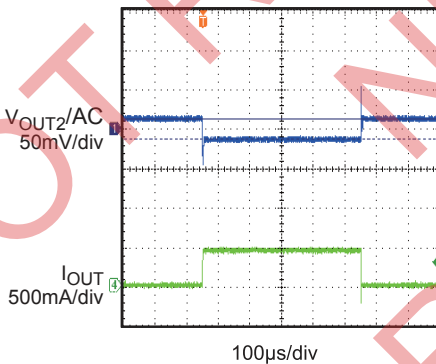
Load Transient

$V_{OUT1} = 1.8V$, $I_{OUT} = 10mA$ to $500mA$
with Resistor Load

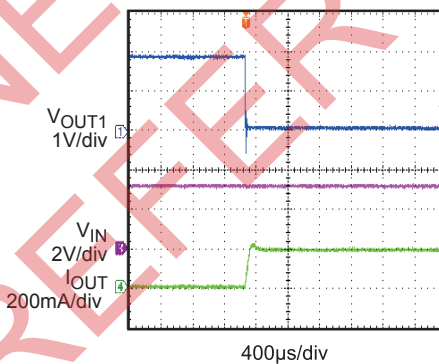


Load Transient

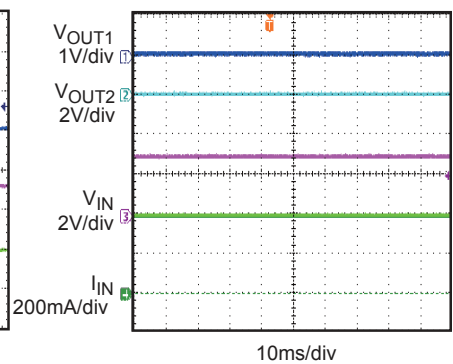
$V_{OUT2} = 2.5V$, $I_{OUT} = 10mA$ to $500mA$
with Resistor Load



Over Current Protection Entry

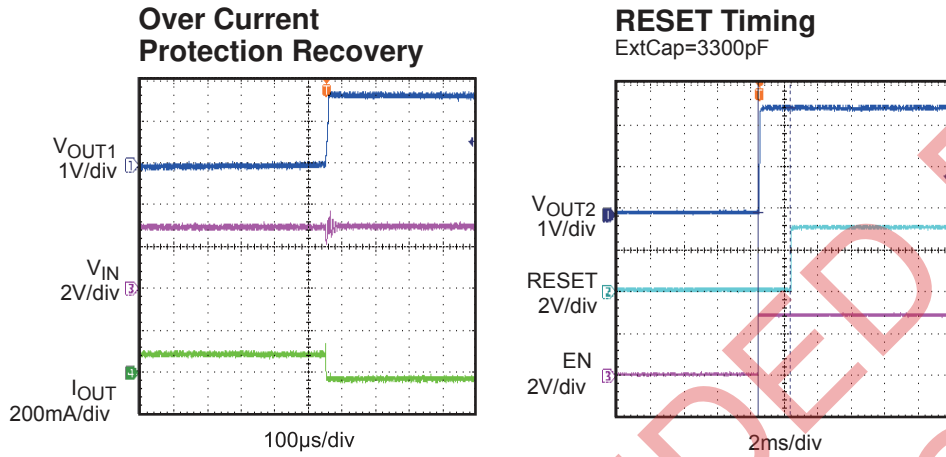


Over Current Protection Steady State



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 3V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 2.5V$, $C_{IN} = C_{OUT1} = C_{OUT2} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.



BLOCK DIAGRAM

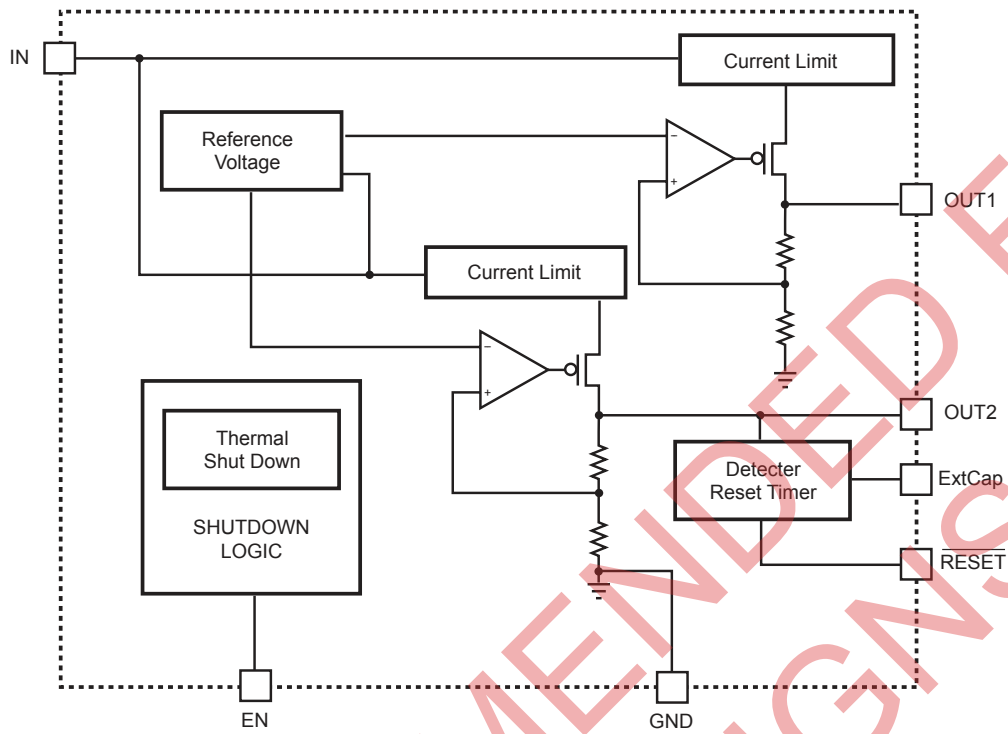


Figure 1—MP6402 Block Diagram

TIMING DIAGRAM

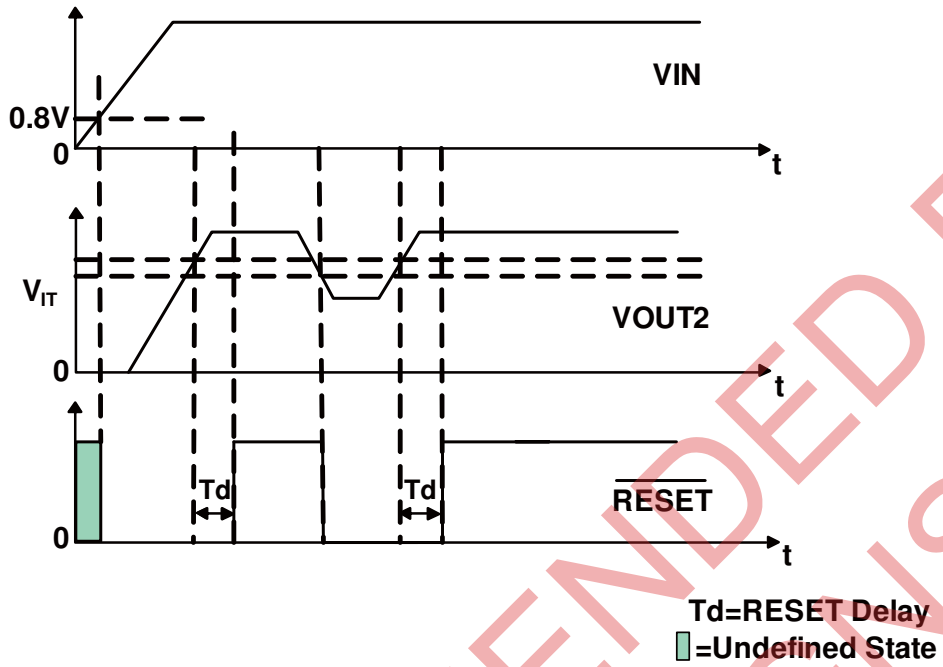


Figure 2—RESET Timing Diagram

OPERATION

The MP6402 integrates two low-noise, low-dropout, low-quiescent current linear regulators with a reset circuit. It operates from a 2.5V to 5.5V input voltage. The dual-channel LDOs can supply up to 500mA of load current. The internal reset circuit is used to monitor the output voltage of channel 2. The RESET becomes active (low) when output voltage drops below its threshold. The MP6402 uses the internal P-channel MOSFET as the pass element and features internal thermal shutdown and internal current limit circuits.

Linear Regulator

The MP6402 integrates dual-channel LDOs. The output voltages are fixed. Their values range from 0.9V and 3.3V with $\pm 1.5\%$ accuracy. Each channel of MP6402 can supply up to 500mA of load current.

Reset Function

The reset circuit monitors the OUT2 pin voltage. RESET is an open-drain, active-low signal pin. It should be connected to power supply through a pull up resistor (R1 should be larger than 10k Ω). RESET becomes active (low) when output voltage of channel 2 drops below its threshold. The thermal shutdown will make the RESET active. When the activated triggering condition is removed, RESET will become inactive after a pre-set delay time. The delay time is programmable through external capacitor between ExtCap and GND.

EN Shutdown

The MP6402 can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator is off and the supply current is reduced. If this feature is not to be used, the EN input should be tied to IN pin to keep the regulator on at all time. Do not float the EN pin.

Current Limit

The MP6402 includes two independent current limit structures which monitor and control the gate voltage of the pass element to limit the guaranteed maximum output current to 500mA.

Output Discharge

The part involves a discharge function that provides a 100 Ω resistive discharge path for the external output capacitor. The function will be active when the part is disabled and it will be done in a very limited time.

Thermal Shutdown

Thermal protection turns off the pass element when the junction temperature exceeds +150 $^{\circ}$ C, allowing cooling the IC. When the IC's junction temperature drops by 20 $^{\circ}$ C, the pass element will be turned on again. Thermal protection limits total power dissipation in the MP6402. For reliable operation, junction temperature should be limited to 125 $^{\circ}$ C maximum.

APPLICATION INFORMATION

Operating Region and Power Dissipation

The maximum power dissipation of MP6402 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipation across the device is

$$P = I_{OUT} \times (V_{IN} - V_{OUT})$$

The maximum power dissipation is:

$$P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$$

Where $(T_J(\text{MAX}) - T_A)$ is the temperature difference between the MP6402 die junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the surrounding environment. The FIN of the MP6402 performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the FIN to ground using a large pad or ground plane.

Input Capacitor Selection

Using a capacitor whose value is higher than 1 μ F on the MP6402 input and the amount of capacitance can be increased without limit. Larger values will help improve line transient response with the drawback of increased size. Ceramic capacitors are preferred.

Output Capacitor Selection

The MP6402 is designed specifically to work with very low ESR ceramic output capacitor in space-saving and performance consideration. A ceramic capacitor in the range of 3.3 μ F and 10 μ F, and with ESR lower than 0.5 Ω is suitable for the MP6402 application circuit. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size.

Programmable Reset Delay Time

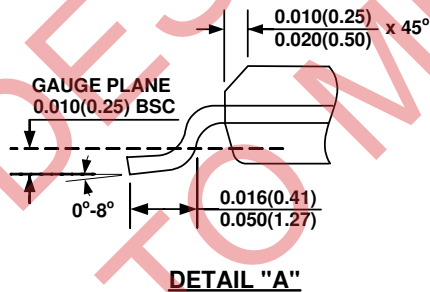
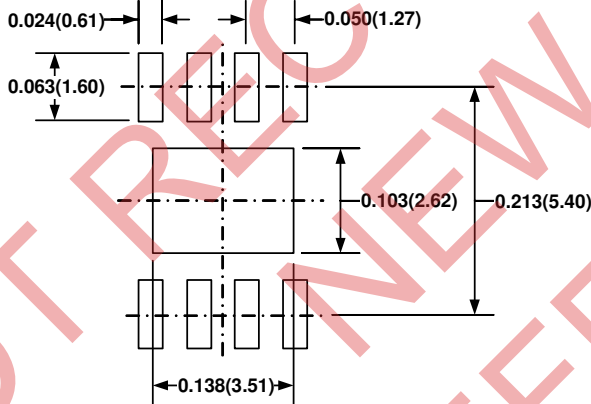
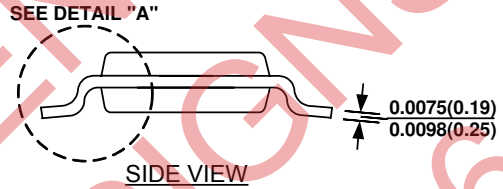
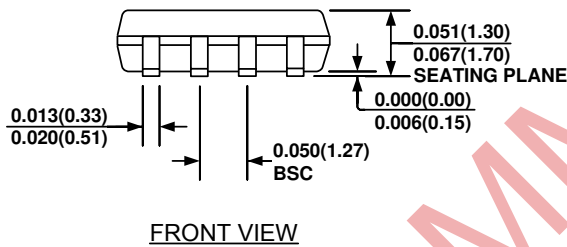
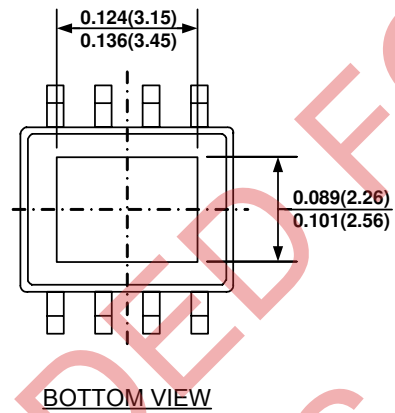
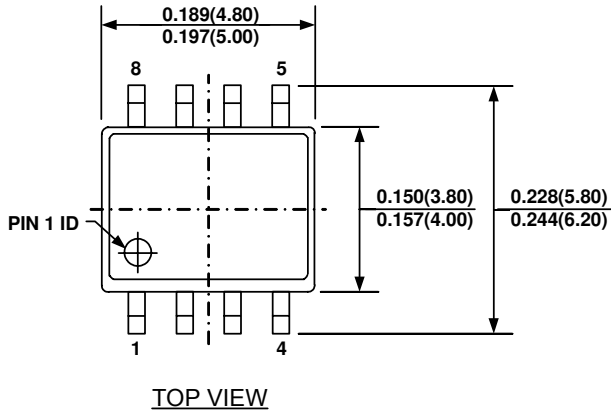
The reset delay time is determined by the value of external capacitor (C_4) connected to ExtCap pin. Typically the reset delay time is 2.1mSec when the external capacitor is 3300pF. For a given delay time, the capacitor value can be calculated using the following equation:

$$T_D(\text{ms}) = [C_4(\text{nF}) \times 0.6] + 0.1$$

The reset delay time is determined by the charge time of external capacitor. Stray capacitance may cause errors of the delay time. A ceramic capacitor with low leakage is strongly recommended.

PACKAGE INFORMATION

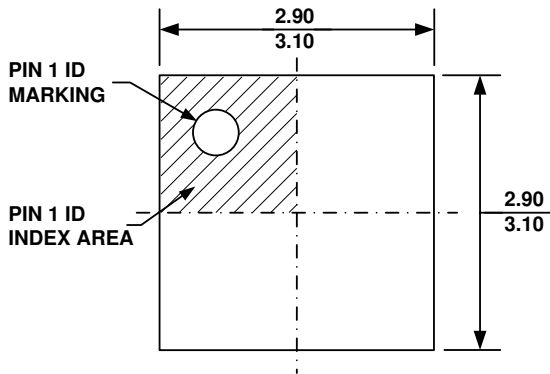
SOIC8E (EXPOSED PAD)



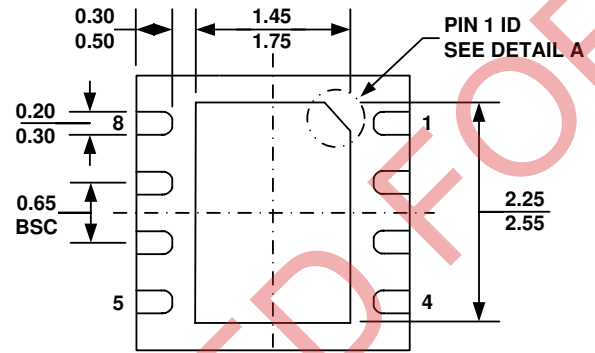
NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

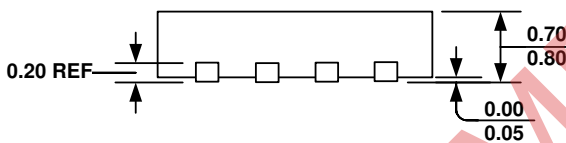
TQFN8 (3mm x 3mm)



TOP VIEW



BOTTOM VIEW



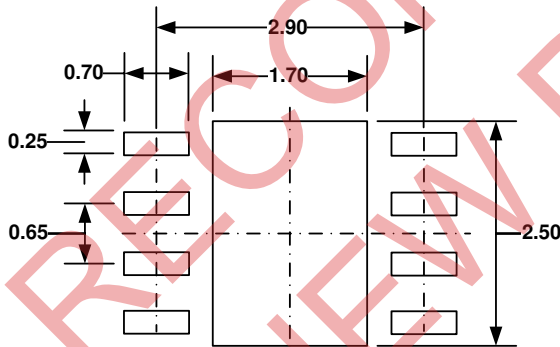
SIDE VIEW

PIN 1 ID OPTION A
0.30x45° TYP.

PIN 1 ID OPTION B
R0.20 TYP.



DETAIL A



RECOMMENDED LAND PATTERN

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