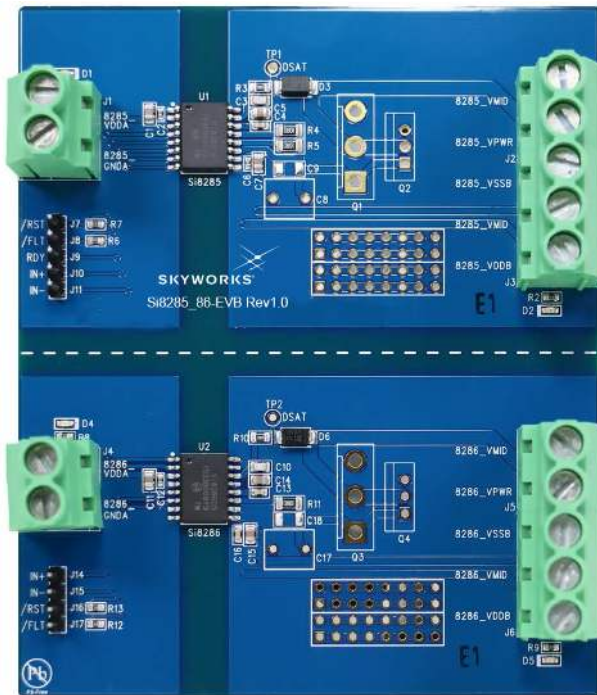# UG169: Si8285/86-EVB User's Guide

This document describes the operation of the Si8285_86-EVB.

The Si8285_86 Evaluation Kit contains the following items:
- Si8285_86-EVB
- Si8285CD-IS and Si8286CD-IS installed on the evaluation board.

KEY POINTS

- Discusses hardware overview and setup, including:
  - Si8285/86 low voltage side connections.
  - Si8285/86 isolated gate drive connections.
- Offers alternative configurations.
- Demonstrates driver functionality.
- Shows Si8285/86-EVB schematics and silkscreen/copper layout.
- Includes a bill of materials and ordering guide.

1. Overview and Setup

1.1 Hardware

Si8285/86-EVB can be used to demonstrate the isolated gate drive capabilities of the installed Si8285CD-IS and Si8286CD-IS, as well as their features specific to driving MOSFETs and IGBTs. The EVB is split into two halves that operate independently—one for Si8285 and the other for Si8286.

Si8285 Low Voltage Side Connections

Supply power to the input side of Si8285 by applying 3 to 5.5 V_{DC} to VDDA at terminal block J1. LED D1 above terminal block J1 illuminates to show power applied.

J7–J11 single pin headers provide access to the IN+, IN–, RSTb inputs, and FLTb and RDY outputs of the Si8285. These signals can be brought out to an external microcontroller using a ribbon cable (not supplied). FLTb output signal has a pull-up resistor to VDDA and is open drain output. This allows multiple gate drivers' FLTb outputs to share the same microcontroller input.

Driver functionality can be exercised without a microcontroller by applying a GNDA referenced PWM signal from a function generator to the IN+ and IN– inputs. Maximum input voltage is VDDA.

Si8285 Isolated Gate Drive Connections

Supply power to the output side of the Si8285 by applying VDDB, VMID, and VSSB at terminal block J3. In typical MOSFET driver applications, VMID = VSSB. When driving IGBTs, typical values for VDDB and VSSB IGBTs are +15 V and –9 V, with respect to VMID. LED D2 above terminal block J3 illuminates to show power applied.

There are four different load options for the Si8285 gate driver:

1. Through holes for a MOSFET or an IGBT in a TO-247 package (not supplied) at Q1.
2. Through holes for a MOSFET or an IGBT in a TO-220 package (not supplied) at Q2.
3. Through holes for a capacitor (not supplied) at C8.
4. Pads for a 1206-size surface mount capacitor (not supplied) at C9.

From top to bottom, the through holes for the transistor leads are Source, Drain, and Gate. Load transistors are biased by applying voltage across VPWR and VMID terminals of J2. This voltage should not exceed the rated VDS of the transistor or the 300 V blocking voltage rating of installed D3. Supply voltage constraints are summarized in .

Note: Si8285 can drive the gate of either high-side or low-side MOSFET or IGBT in a bridge configuration. When used as a high-side gate driver, VMID is connected to the load. When used as a low-side gate driver, VMID is the return for the load.

For capacitive loads, capacitor value should be chosen to match the gate capacitance of the desired transistor.

Si8286 Low Voltage Side Connections

Supply power to the input side of Si8286 by applying 3 to 5.5 V_{DC} to VDDA at terminal block J4. LED D4 above terminal block J4 illuminates to show power applied.

J14-J17 single pin headers provide access to the IN+, IN–, RSTb input, and the FLTb output of the Si8286. These signals can be brought out to an external microcontroller using a ribbon cable (not supplied). FLTb output signal has a pull-up resistor to VDDA and is an open drain output. This allows multiple gate drivers' FLTb outputs to share the same microcontroller input.

Si8286 Isolated Gate Drive Connections

Supply power to the output side of the Si8286 by applying VDDB, VMID, and VSSB at terminal block J6. In typical MOSFET driver applications, VMID = VSSB. When driving IGBTs, typical values for VDDB and VSSB IGBTs are +15 V and –9 V, with respect to VMID. LED D5 above terminal block J6 illuminates to show power applied.

There are four different load options for Si8286 gate driver:
1. Through holes for a MOSFET or an IGBT in a TO-247 package (not supplied) at Q3.
2. Through holes for a MOSFET or an IGBT in a TO-220 package (not supplied) at Q4.
3. Through holes for a capacitor (not supplied) at C17.
4. Pads for a 1206-size surface mount capacitor (not supplied) at C18.

From top to bottom, the through holes for the transistor leads are Source, Drain, and Gate. Load transistors are biased by applying voltage across VPWR and VMID terminals of J5. This voltage should not exceed the rated V_{DS} of the transistor or the 300 V blocking voltage rating of installed D6.

Note: Si8286 can drive the gate of either high-side or low-side MOSFET or IGBT in a bridge configuration. When used as a high-side gate driver, VMID is connected to the load. When used as a low-side gate driver, VMID is the return for the load.

For capacitive loads, capacitor value should be chosen to match the gate capacitance of the desired transistor. Supply voltage constraints are summarized in the table below.

Table 1.1. Supply Voltage Constraints

3.0 V ≤ VDDA – GNDA ≤ 5.5 V
VSSB ≤ VMID < VDDB
UVLO+ < VDDB – VSSB < 30 V
VPWR < V_{DS} (Q)
VPWR < 300 V
|GNDA-VSSB| < 5 kV
Note: 1. UVLO+ for the Si8285CD-IS and Si8286CD-IS is 12.3 V typically.

1.2 Alternative Configurations

Positive Voltage Gate Drive Only

The standard configuration for the gate driver is to apply positive voltage, VDDB–VMID, to the gate during the high drive portion of the PWM cycle and negative voltage, VSSB–VMID, during the low drive portion of the PWM cycle. Alternatively, if only positive drive voltage is desired, short VSSB and VMID at terminals 2 and 3 of J3/J6.

Prototyping Area

If additional components are needed to evaluate the gate drive function for a particular load, there is a prototyping area just below Q1 and Q3 locations.

1.3 Demonstrating Driver Functionality

Even with no load connected, the basic functionality of the Si8285 can be demonstrated:

1. Apply 5 V to VDDA. D1 will illuminate.
2. Apply 15 V between VDDB and VMID. Apply –9 V between VMID and VSSB (VMID 9 V higher than VSSB). D2 will illuminate.
3. Short VPWR to VMID using a wire between the terminals of J2. This disables desaturation detection and allows for normal operation of the Si8285.
4. Since both sides have been powered on, RDY will output 5 V, which can be observed at J9.
5. Apply 5 V to both J10, IN+ and J11, IN–. The Si8285 will drive low and –9 V can be observed across C8.
6. Apply 5 V to J10, IN+ and 0 V to J11, IN–. The Si8285 will drive high and +15 V can be observed across C8.
7. Remove the short between VPWR and VMID at J2.
8. With no path for the DSAT current, the voltage at the DSAT pin rises and the Si8285 will drive the output low and will drive FLTb to 0 V, which can be observed at J8.
9. Once again, place the short back between VPWR and VMID at J2. Drive RSTb input to 0 V. This clears the fault and 5 V will be observed on J8, FLTb.

Using the same method, Si8286 basic functionality can also be demonstrated:

1. Apply 5 V to VDDA. D4 will illuminate.
2. Apply 15 V between VDDB and VMID. Apply –9 V between VMID and VSSB. D5 will illuminate.
3. Short VPWR to VMID using a wire between the terminals of J5. This disables desaturation detection and allows for normal operation of the Si8286.
4. Apply 5 V to both J14, IN+ and J15, IN–. The Si8286 will drive low and –9 V can be observed across C17.
5. Apply 5 V to J14, IN+ and 0 V to J15, IN–. The Si8286 will drive high and +15 V can be observed across C17.
6. Remove the short between VPWR and VMID at J5.
7. With no path for the DSAT current, the voltage at the DSAT pin rises and the Si8286 will drive the output low and will drive FLTb to 0 V, which can be observed at J17.
8. Once again, place the short between VPWR and VMID at J5. Drive RSTb input to 0 V. This clears the fault and 5 V will be observed on J17, FLTb.

1.4 Quick Reference Table

Table 1.2. Test Point Descriptions

Test Point	Description	Referenced to
TP1	DSAT (Si8285)	VMID
TP2	DSAT (Si8286)	VMID

2. Schematics
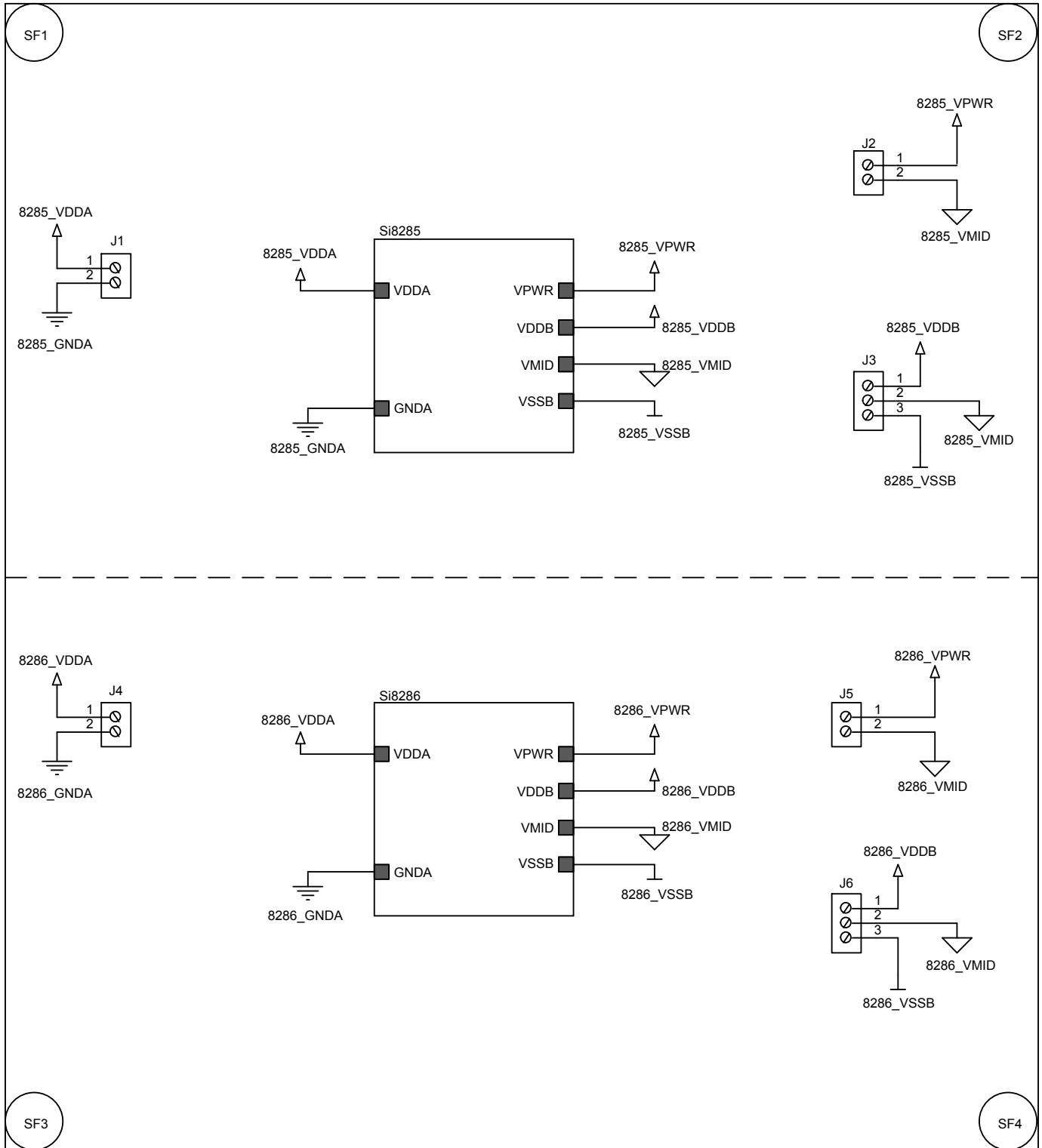
Figure 2.1. Si8285/86-EVB Top Level Schematic
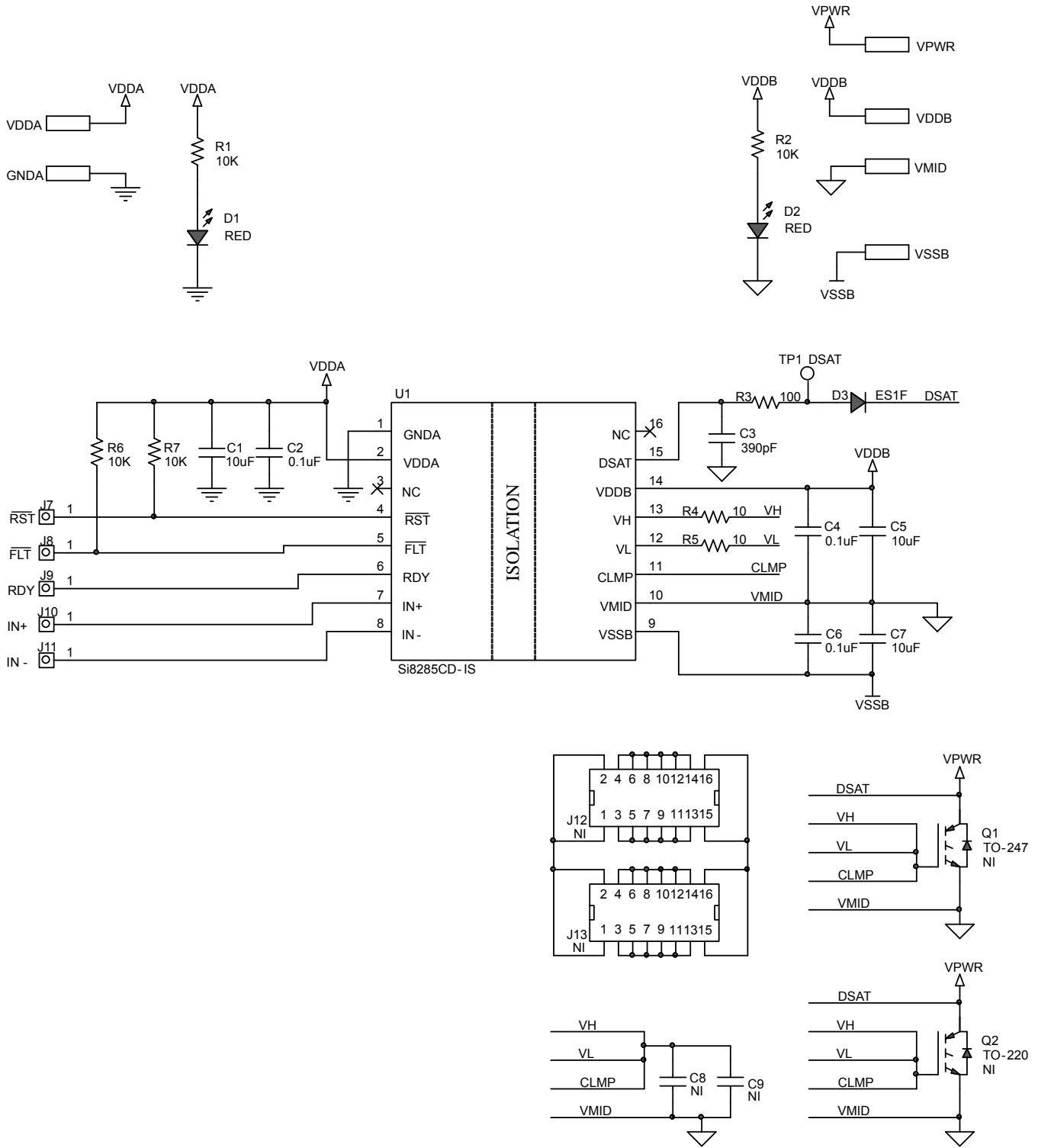
Figure 2.2. Si8285 Circuit Schematic
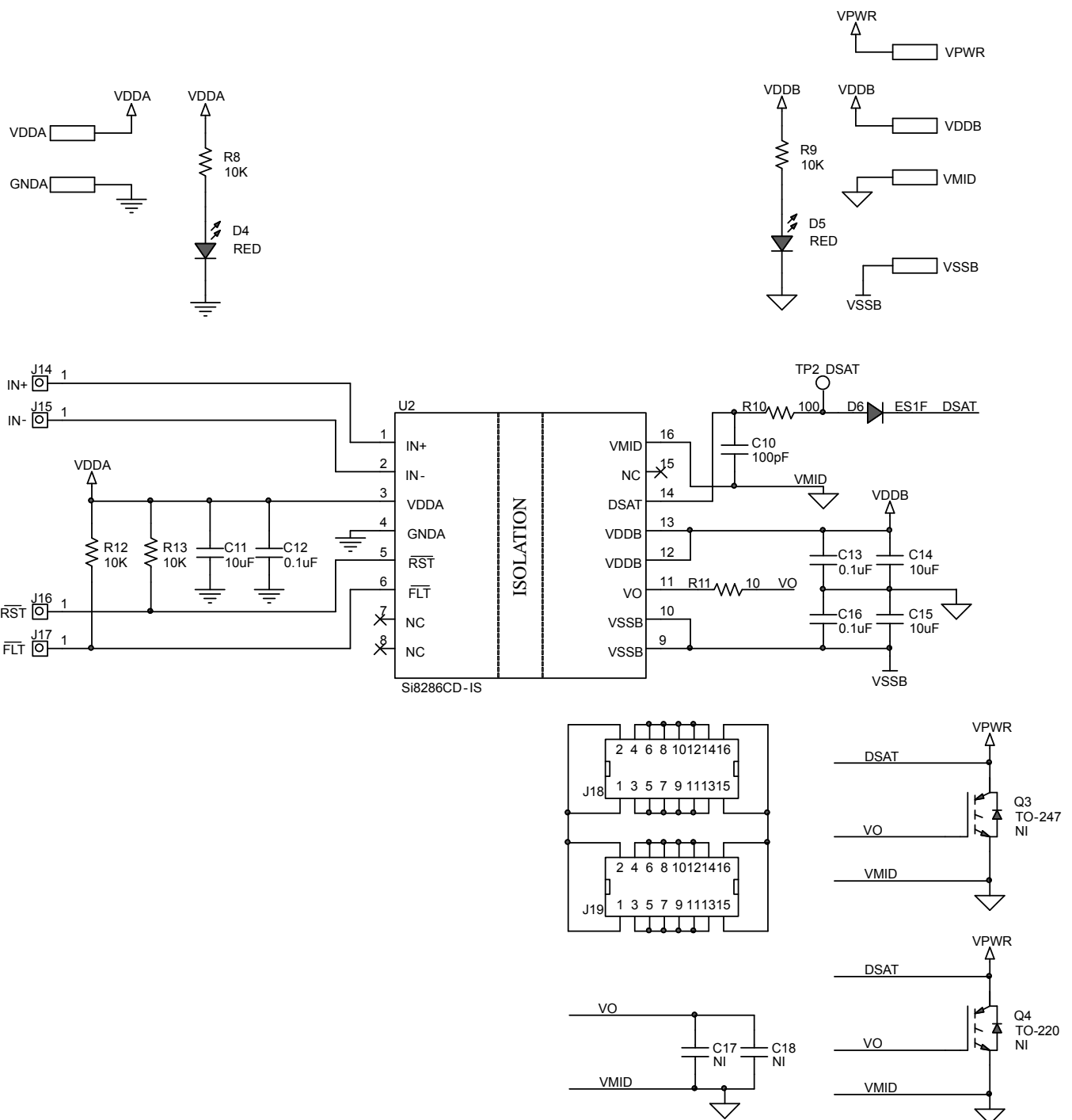
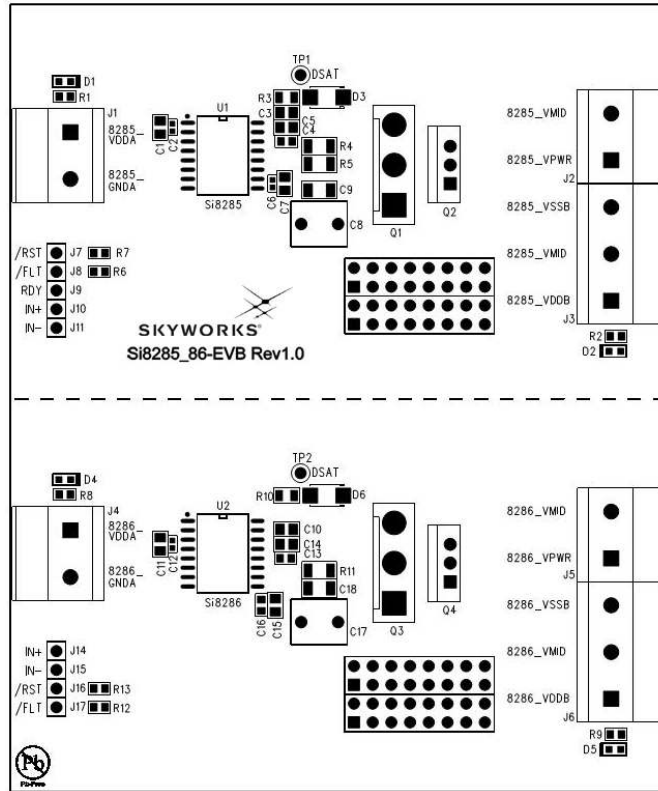**Figure 2.3. Si8286 Circuit Schematic**

3. Layout

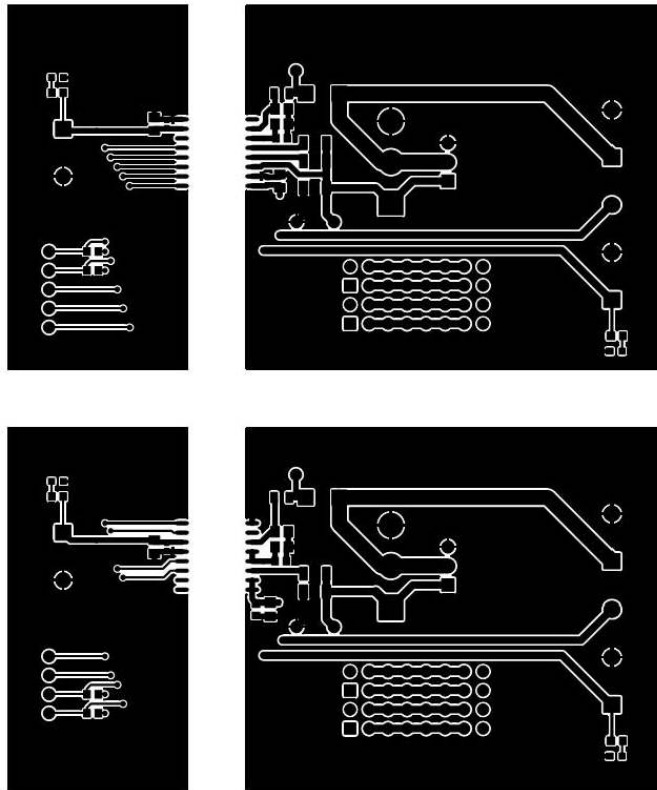**Figure 3.1. Si8285/86-EVB Top Silkscreen**

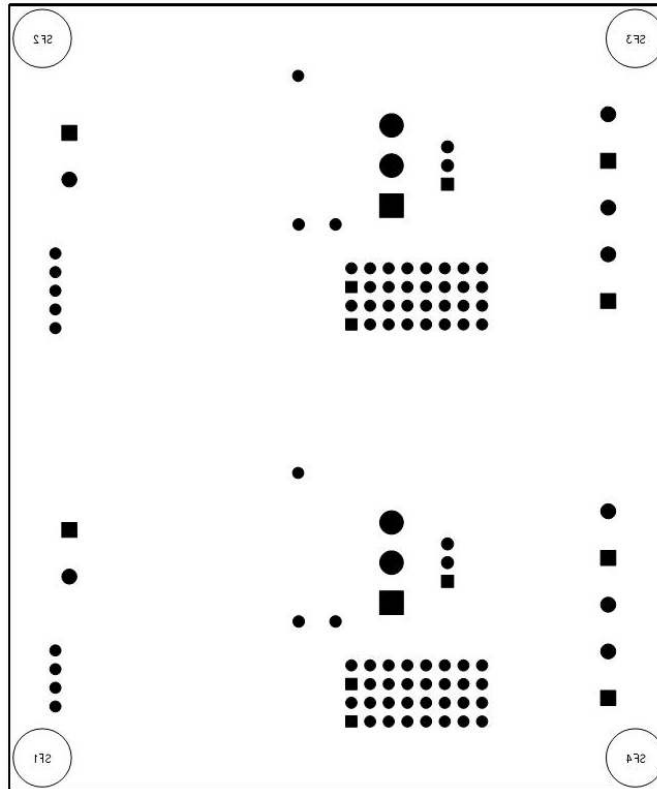**Figure 3.2. Si8285/86-EVB Top Copper**
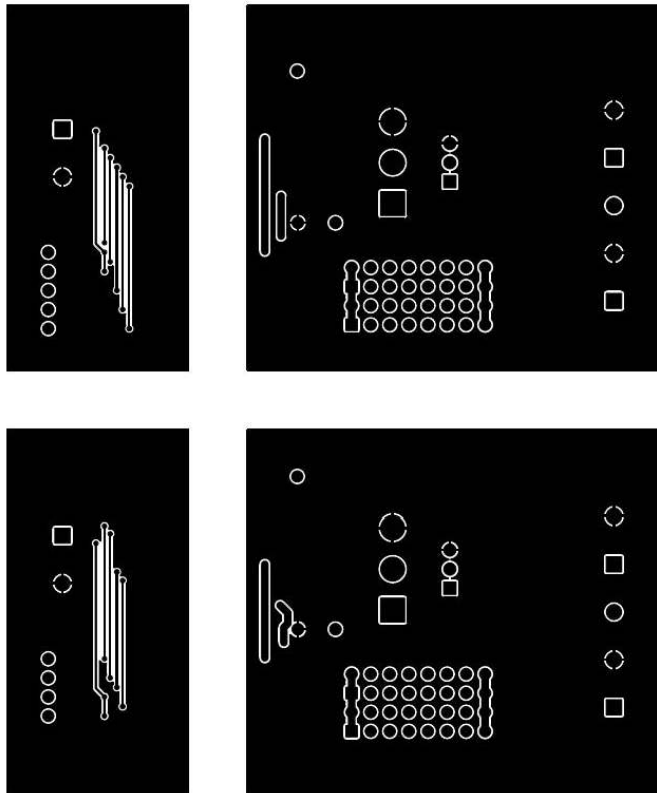
Figure 3.3. Si8285/86-EVB Bottom Silkscreen

Figure 3.4. Si8285/86-EVB Bottom Copper

4. Bill of Materials

Table 4.1. Si8285/86-EVB Bill of Materials

Part Reference	Description	Manufacturer	Manufacturer Part Number
C1, C11	CAP, 10 µF, 16 V, ±10%, X5R, 0805	Venkel	C0805X5R160-106K
C2, C6, C12	CAP, 0.1 µF, 16 V, ±10%, X7R, 0402	Venkel	C0402X7R160-104K
C3	CAP, 390 pF, 100 V, ±20%, X7R, 0805	Venkel	C0805X7R101-391M
C4, C13, C16	CAP, 0.1 µF, 50 V, ±10%, X7R, 0603	Venkel	C0603X7R500-104K
C5, C7, C14, C15	CAP, 10 µF, 25 V, ±20%, X6S, 0805	Venkel	C0805X6S250-106M
C10	CAP, 100 pF, 200 V, ±5%, NP0 HIGH Q, 0805	Venkel	C0805HQN201-101J
D1, D2, D4, D5	LED, RED, 631 nM, 20 mA, 2 V, 54mcd, 0603	LITE-ON TECHNOLOGY CORP	LTST-C190KRKT
D3, D6	DIO, FAST, 300 V, 1.0A, SMA	Fairchild	ES1F
J1, J2, J4, J5	Terminal Block, 2 pos, 6.35 mm, 10-30AWG, 300 V, 32 A	Phoenix Contact	1714955
J3, J6	Terminal Block, 3 pos, 6.35 mm, 10-30AWG, 300V, 32 A	Phoenix Contact	1714968
J7, J8, J9, J10, J11, J14, J15, J16, J17	Header, Single Pin, Tin Plated	Samtec	TSW-101-07-T-S
R1, R2, R6, R7, R8, R9, R12	RES, 10 K, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-1002F
R13			
R3, R10	RES, 100 Ω, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-1000F
R4, R5, R11	RES, 10 Ω, 1/4 W, ±1%, ThickFilm, 1206	Venkel	CR1206-4W-10R0F
SF1, SF2, SF3, SF4	HDW, BUMPON CYLINDRICAL, 0.312 x 0.215, BLK	3M	SJ61A6
TP1, TP2	TESTPOINT, WHITE, PTH	Kobiconn	151-201-RC
U1	IC, 4 AMP ISODRIVER, 12 V UVLO, 5KV, SOW16	Skyworks	Si8285CD-IS
U2	IC, 4 AMP ISODRIVER, 12 V UVLO, 5KV, SOW16	Skyworks	Si8286CD-IS

5. Ordering Guide

Table 5.1. Si8285/86-EVB Ordering Guide

Ordering Part Number (OPN)	Description
Si8285_86-KIT	Si8285/Si8286 Isolated gate driver evaluation board kit.

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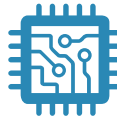
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