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December 2013

FQN1N50C

N-Channel QFET® MOSFET

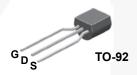
500 V, 0.38 A, 6 Ω

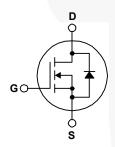
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 0.38 A, 500 V, $R_{DS(on)} = 6 \Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 0.19 \text{ A}$
- Low Gate Charge (Typ. 4.9 nC)
- Low Crss (Typ. 4.1 pF)
- 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		/	FQN1N50CTA	Unit
V _{DSS}	Drain-Source Voltage		500	V	
I _D	Drain Current	- Continuous (T _C = 25°C)		0.38	A
		- Continuous (T _C = 100°C)		0.24	A
I _{DM}	Drain Current - Pulsed (Note 1)		(Note 1)	3.04	A
V_{GSS}	Gate-Source Voltage			± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		(Note 2)	44.4	mJ
I _{AR}	Avalanche Current (Note 1		(Note 1)	0.38	A
E _{AR}	Repetitive Avalanche Energy (No		(Note 1)	0.21	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		(Note 3)	4.5	V/ns
P_{D}	Power Dissipation (T _A = 25°C)			0.89	W
	Power Dissipation (T _L = 25°C)			2.08	W
	- Derate above 25°C			0.017	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.			300	°C

Thermal Characteristics

Symbol	Parameter	FQN1N50CTA	Unit	
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead, Max.	(Note 5a)	60	- °C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	(Note 5b)	140	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQN1N50CTA	1N50C	TO-92	AMMO	N/A	N/A	2000 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

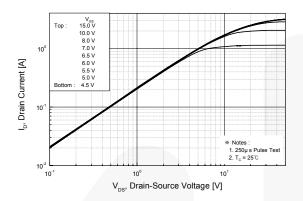
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Characte	ristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{D} = 250 μA	500			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.5		V/°C
I _{DSS}	Zero Gate Voltage Drain Current V _{DS} = 500 V, V _{GS} = 0 V				50	μΑ
		V _{DS} = 400 V, T _C = 125°C			250	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$	/-		-100	nA
On Characte	ristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.19 A	-	4.6	6.0	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 0.19A	\	0.6		S
Dynamic Cha	aracteristics				T	
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		150	195	pF
C _{oss}	Output Capacitance	1 = 1.0 MHZ		28	40	pF
C _{rss}	Reverse Transfer Capacitance			4.1		pF
Switching Cl	naracteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 1.0 A,		10	30	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		10	30	ns
t _{d(off)}	Turn-Off Delay Time			20	50	ns
t _f	Turn-Off Fall Time	(Note 4)	/	15	40	ns
Qg	Total Gate Charge	$V_{DS} = 400 \text{ V}, I_D = 1.0 \text{ A},$		4.9	6.4	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		0.66		nC
Q _{gd}	Gate-Drain Charge	(Note 4)		2.9		nC
Drain-Source	e Diode Characteristics and Maximum R	atings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				0.38	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				3.04	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.38 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 1.0 A,		188		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs		0.55		μС

- 1. Repetitive rating : pulse-width limited by maximum junction temperature.
- 2. L = 80 mH, I_{AS} = 1.0 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C.
- $3.~\text{I}_{SD} \leq 0.38~\text{A, di/dt} \leq 200~\text{A/}\mu\text{s, V}_{DD} \leq \text{BV}_{DSS,}~\text{starting}~~\text{T}_{J} = 25^{\circ}\text{C}.$
- 4. Essentially independent of operating temperature.

- 5. a) Reference point of the R_{0,IL} is the drain lead.
 b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment (R_{0,IA} is the sum of the junction-to-case and case-to-ambient thermal resistance. R_{0CA} is determined by the user's board design)

Typical Performance Characteristics

Figure 1. On-Region Characteristics



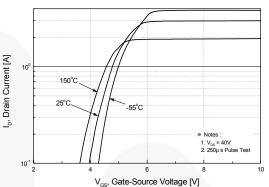


Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs. **Drain Current and Gate Voltage**

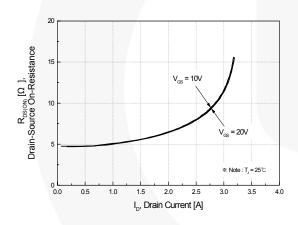


Figure 4. Body Diode Forward Voltage **Variation vs. Source Current** and Temperatue

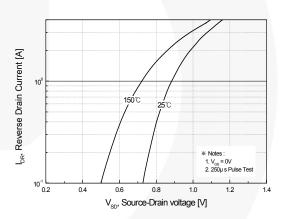


Figure 5. Capacitance Characteristics

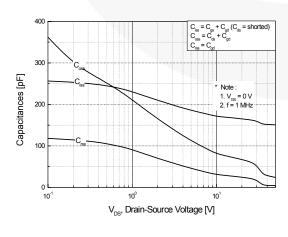
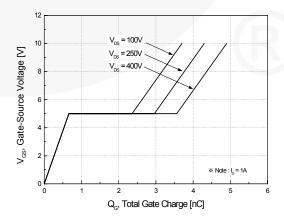


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

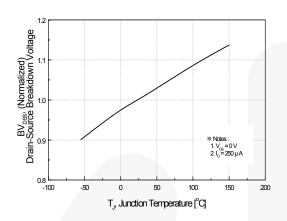


Figure 8. On-Resistance Variation vs. Temperature

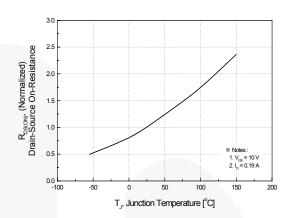


Figure 9. Maximum Safe Operating Area

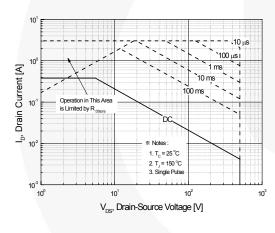


Figure 10. Maximum Drain Current vs. Case Temperature

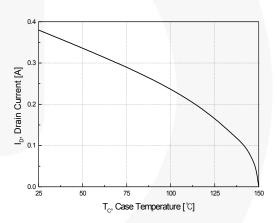
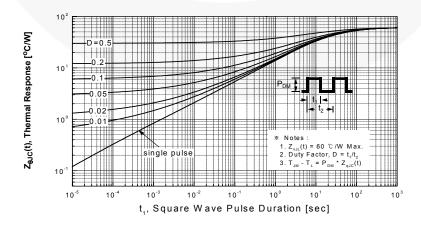


Figure 11. Transient Thermal Response Curve



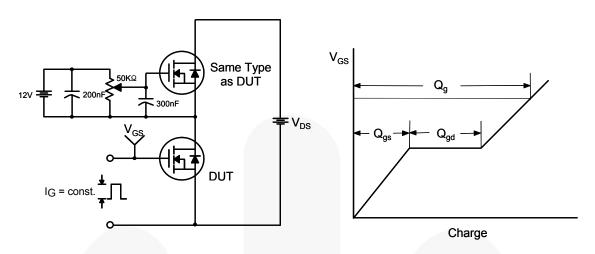


Figure 12. Gate Charge Test Circuit & Waveform

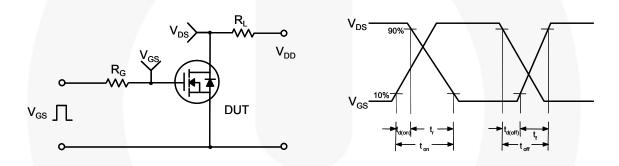


Figure 13. Resistive Switching Test Circuit & Waveforms

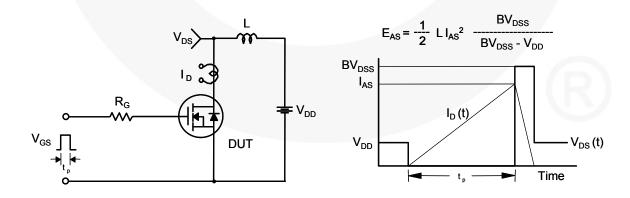


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

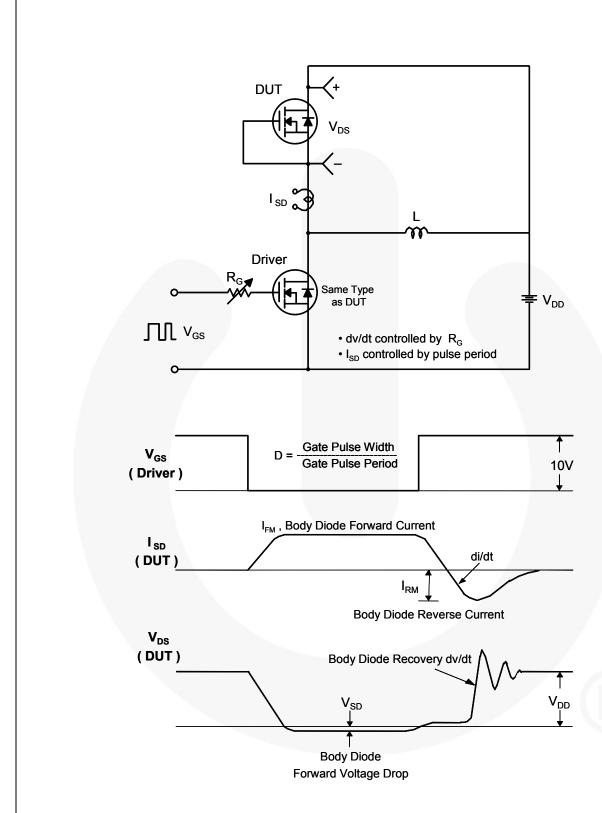


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

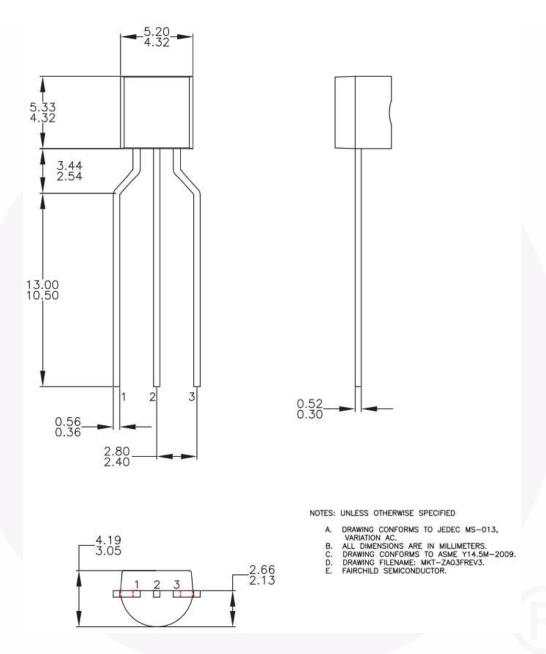


Figure 16. TO92, Molded, 3-Lead, 0.200 In Line Spacing LD Form (J61Z Option)

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