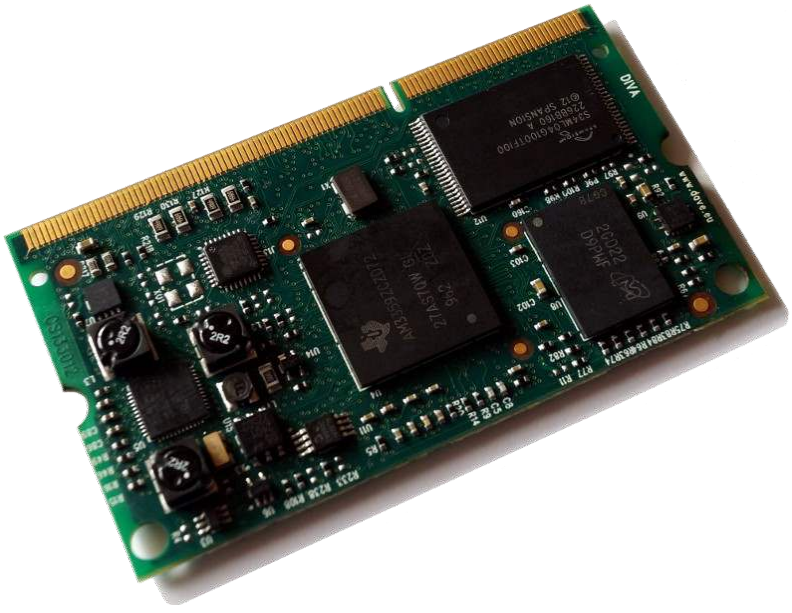
ARM Cortex-A8 CPU Module Family

LITE Line

HARDWARE MANUAL



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1 Preface

1.1 About this manual

This Hardware Manual describes the DIVA CPU module series, their design and functions.

Precise specifications for the Texas Instruments AM335x processors can be found in the CPU datasheets and/or reference manuals.

1.2 Copyrights/Trademarks

Ethernet® is a registered trademark of XEROX Corporation.

All other products and trademarks mentioned in this manual are property of their respective owners.

1.3 Standards

DAVE Embedded Systems is certified to ISO 9001 standards.

1.4 Disclaimers

DAVE Embedded Systems does not assume any responsibility for availability, supply and support related to all products mentioned in this manual that are not strictly part of the DIVA CPU module.

DIVA CPU Modules are not designed for use in life support appliances, devices, or systems where malfunctioning of these products can reasonably be expected to result in personal injury. **DAVE Embedded Systems** customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

1.5 Warranty

DIVA is guaranteed against defects in material and workmanship for the warranty period from the shipment date. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair or replace defective products. Within the warranty period, the repair of products is free of charge provided that warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the customer, unauthorized modification or misuse, operation outside of the product's specifications or improper installation or maintenance.

DAVE Embedded Systems will not be responsible for any defects or damages to other products not supplied by **DAVE Embedded Systems** that are caused by a faulty DIVA module.

1.6 Technical Support

We are committed to making our products easy to use and will help customers use our CPU modules in their systems.

Technical support is delivered through email for registered kits owners. Support requests can be sent to support-diva@dave.eu. Software upgrades are available for download in the restricted download area of **DAVE Embedded Systems** web site: http://www.dave.eu/reserved-area. An account is required to access this area.

Please refer to our Web site at http://www.dave.eu/dave-cpu-module-am335x-diva.html for the latest product documents, utilities, drivers, Product Change Notices, Board Support Packages, Application Notes, mechanical drawings and additional tools and software.

1.7 Related documents

Document	Location
DAVE Embedded Systems Developers Wiki	http://wiki.dave.eu/index.php/Main_Page
AM335x Technical Reference Manual	http://www.ti.com/lit/ug/spruh73h/spruh73h.pdf
AM335x Portal (on TI Embedded Processors Wiki)	http://processors.wiki.ti.com/index.php/Sitara_AM335x_Portal
Integration guide (on **DAVE Embedded Systems** Developers Wiki)	http://wiki.dave.eu/index.php/Integration_guide_%28Diva%29

Tab. 1: Related documents

1.8 Conventions, Abbreviations, Acronyms

Abbreviation	Definition
BTN	Button
DIVELK	DIVA Embedded Linux Kit
EMAC	Ethernet Media Access Controller
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
PCB	Printed circuit board
PMIC	Power Management Integrated Circuit
PRU	Programmable Real-Time Unit
PSU	Power supply unit

Abbreviation	Definition
RTC	Real time clock
SOC	System-on-chip
SO-DIMM	Small Outline Dual In-line Memory Module
SOM	System-on-module
WDT	Watchdog

Tab. 2: Abbreviations and acronyms used in this manual

Revision History

Version	*Date*	*Notes*
0.9.0	October 2012	First Draft
1.0.0	June 2013	First official release
1.0.1	September 2013	Minor fixes
1.0.2	October 2013	Fixed RTC_PWRONRSTn direction VAUX33 added to pinout table Fixed PMIC_VBACKUP information Fixed section 8.1 and 8.2 tables Added I2C pull-up/pull-down information Minor fixes
1.0.3	April 2014	Minor fixes
1.0.4	August 2014	Updated block diagram Fixed PGOOD (VAUX33) description Minor fixes
1.0.5	October 2013	Pinout table fixes Minor fixes
1.0.6	June 2015	Minor Fixes Updated mechanical drawings

2 Introduction

DIVA is a family of system-on-modules (SOM) that belongs to **DAVE Embedded Systems LITE Line** product class. DIVA is based on Texas Instruments "Sitara" AM335x Cortex-A8 application processor and is built with SO-DIMM 204 pin form factor.

Fig. 1: DIVA CPU module

DIVA offers lots of graphics, processing, peripherals and industrial interface options, allowing customers to implement cost-effective design. The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) adds further flexibility and enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink.

Typical applications for DIVA are:

- Industrial sensors and I/O units
- Industrial drives with integrated communications and multi-axis motor control
- Programmable logic/automation controllers (PLC/PAC) with integrated industrial communications such as PROFIBUS, CAN and Ethernet
- Home and Building Automation

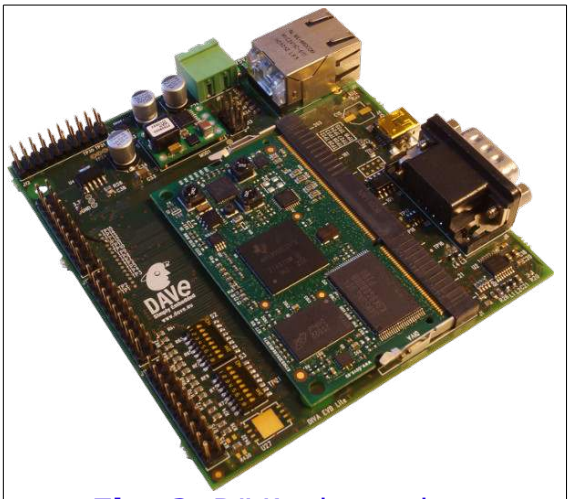


Fig. 2: DIVA plugged on DIVAEVB-Lite

2.1 Product Highlights

- ARM Cortex-A8 architecture @ 275/500/600/720 MHz
  - LITE Line
  - "No-frills" CPU module
  - SO-DIMM connector
  - Great cost-efficiency
- Extended power supply range [3.6 - 5.5]V, power regulation on board
- Coprocessing modules
  - NEON
  - PowerVR SGX
  - Crypto accelerator
- Industrial specification compliance
  - Extended temperature range (-40°C/+85°C)
  - Industrial-oriented interfaces set
- Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
  - Supports protocols such as EtherCAT, PROFIBUS, PROFINET, EtherNet/IP™, and more
  - Peripherals Inside the PRU-ICSS: UART port with flow control pins, MII Ethernet ports, MDIO port, ...

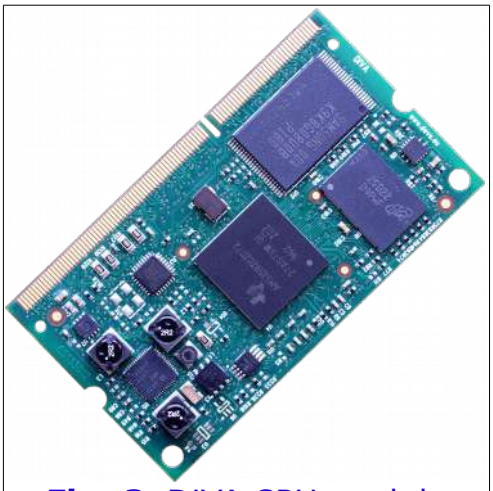
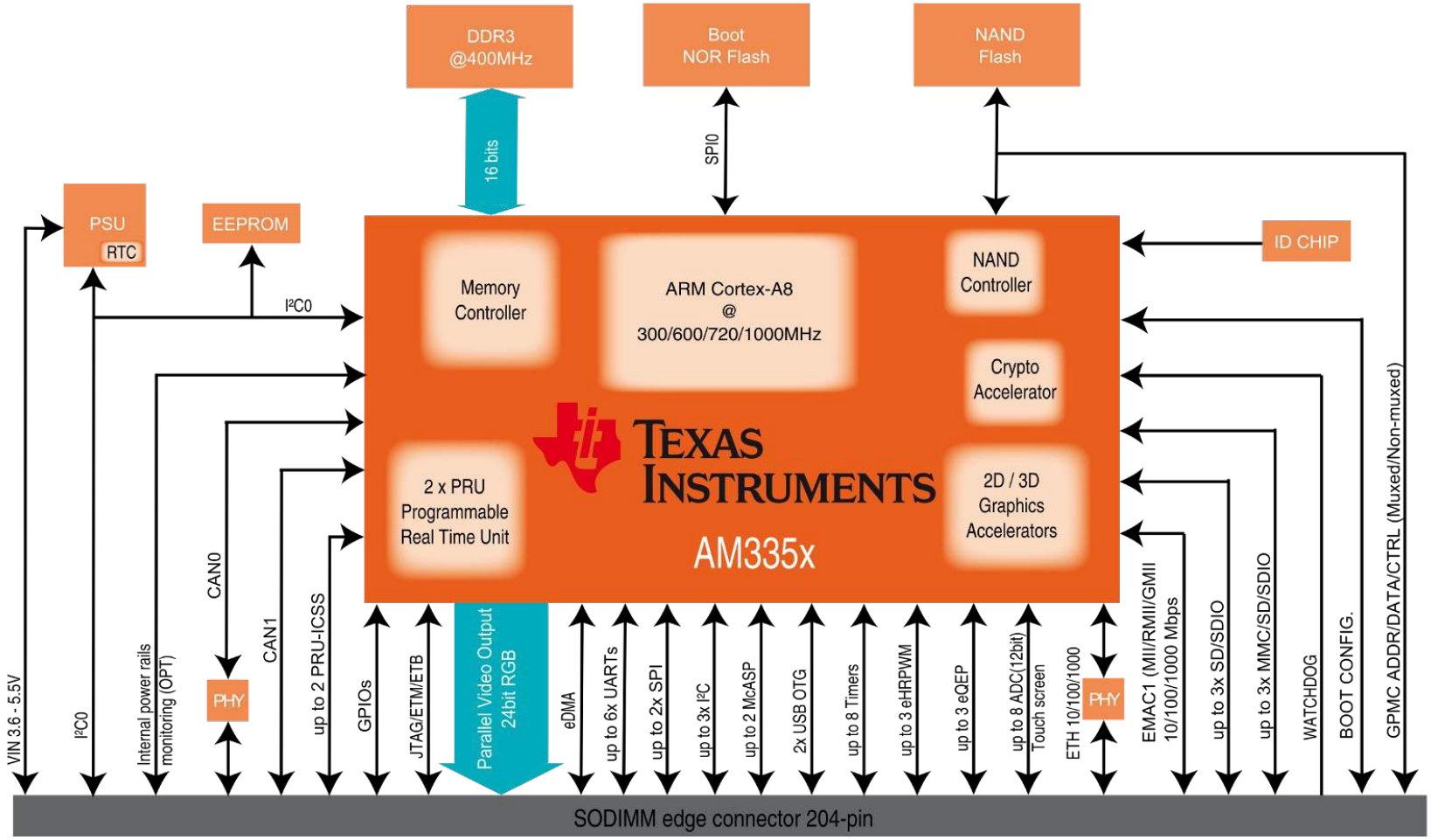


Fig. 3: DIVA CPU module

2.2 Block Diagram



2.3 Feature Summary

Feature	Specifications	Options
CPU	"Sitara" AM335x ARMv7 architecture Cortex A8 @ 300/600/800/1000	
RAM	16-bit DDR3 @ 333 MHz Up to 512 MB	
Storage	Flash NOR SPI Flash NAND on Local bus I²C 32 kbit EEPROM	

Tab. 3: CPU, Memories, Busses

Feature	Specifications	Options
Graphics Controller	Up to 24-Bits Data Output Resolution Up to 2048x2048 (With Maximum 126-MHz Pixel Clock) TFT/RGB support	
2D/3D Engines	NEON Multimedia SIMD coprocessor PowerVR SGX 530 3D Accelerator	
Coprocessors	Crypto Hardware Accelerator (AES, SHA, PKA, RNG) Up to 2x Programmable Realtime Units (PRUs)	
USB	Up to 2x 2.0 OTG ports	
UARTs	Up to 6x UART ports	
GPIO	Up to 118 lines, shared with other functions (interrupts available)	
Input interfaces	Integrated 4/5/8-wire resistive touch screen controller	
Networking	Fast Ethernet with PHY Additional MII/RMII/RGMII interface	
CAN	Dual CAN controller (version 2 part A, B)	
SD/MMC	Up to 3x MMC/SD/SDIO Serial interfaces (up to 48 MHz)	
Serial busses	Up to 3x I²C channels Up to 2x SPI channels	
Audio	Up to 2x McASP interface	
Timers/PWM	Up to 4 programmable general purpose	

Feature	Specifications	Options
	timers (PWM function available) PWMSS (Pulse width modulation subsystem) with 3x eHRPWM, 3x eCap, 3x eQEP	
RTC	On board, external battery powered	
Debug	JTAG IEEE 1149.1 Test Access Port ETM Port ETB Port	
Miscellaneous	Up to 8x 12-bit ADC channels	

Tab. 4: Peripherals

Feature	Specifications	Options
Supply Voltage	[3.6 - 5.5] V, voltage regulation on board	
Active power consumption	Please refer to Power consumption section	
Dimensions	67.5 mm x 38.3 mm	
Weight	<tbd>	
MTBF	<tbd>	
Operation temperature	0..70 °C -40..+85 °C	
Shock	<tbd>	
Vibration	<tbd>	
Connectors	204-pin SO-DIMM	
Connectors insertion/removal	<tbd>	

Tab. 5: Electrical, Mechanical and Environmental Specifications

3 Design overview

The heart of DIVA module is composed by the following components:

- Texas Instruments AM335x processor
- Power supply unit
- DDR2 memory bank
- NOR and NAND flash banks
- 204 pin SO-DIMM connector with interfaces signals

This chapter shortly describes the main DIVA components.

3.1 “Sitara” AM335x CPU

Sitara™ ARM Cortex-A8 microprocessors (MPUs) are designed to optimize performance and peripheral support for customers in a variety of markets. AM335x Sitara™ are highly-integrated, scalable and programmable CPU families from Texas Instruments and are enhanced with image, graphics processing, peripherals and industrial interface options such as EtherCAT and PROFIBUS. The following subsystems are part of the processor:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 architecture:
  - ARM Cortex-A8 RISC processor, with Neon™ Floating-Point Unit, 32KB L1 Instruction Cache, 32KB L1 Data Cache and 256KB L2 Cache
  - VFP coprocessor
- Debug subsystem (JTAG, CoreSight Embedded Trace Macrocell (ETM))
- General-Purpose Memory Controller (GPMC)
- PowerVR SGX 530 subsystem for vector/3D graphics acceleration to support display and gaming effects
- LCD and Touchscreen Controller

- Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
- Integrated peripherals (USBs, EMACs, UARTs, ...)

The following table shows a **comparison** between the devices, highlighting the differences:

Processor	PowerVR SGX 3D	PRU-ICSS	Ethercat	Crypto	Clock speed (MHz)
AM3359	YES	YES	YES	YES	800
AM3358	YES	YES	N.A.	YES	600 800 1000
AM3357	N.A.	YES	YES	YES	300 600 800
AM3356	N.A.	YES	N.A.	YES	300 600 800
AM3354	YES	N.A.	N.A.	YES	600 800 1000
AM3352	N.A.	N.A.	N.A.	YES	300 600 800 1000

Tab. 6: AM335x part number comparison

3.2 DDR3 memory bank

DDR3 SDRAM memory bank is composed of a 16-bit width chip. The following table reports the SDRAM specifications:

CPU connection	SDRAM bus
Size min	64 MB
Size max	512 MB
Width	16 bit
Speed	333 MHz

Tab. 7: DDR3 specifications

3.3 NOR flash bank

NOR flash is a Serial Peripheral Interface (SPI) device. This feature is optional and, when populated, the device is connected to AM335X_SPI0 and can act as boot memory. The chip select is AM335X_SPI0_CS0.

The following table reports the NOR flash specifications:

CPU connection	AM335X_SPI0 (CS0n)
Size min	4 MByte
Size max	128 MByte
Bootable	Yes

Tab. 8: NOR flash specifications

3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash. This feature is optional and, when populated, the device is connected to the GPMC bus. The chip select is AM335X_GPMC_CS0n.

The following table reports the NAND flash specifications:

CPU connection	GPMC bus (CS0n)
Page size	512 byte, 2 kbyte or 4 kbyte
Size min	32 MByte
Size max	2 GByte
Width	8 bit
Bootable	Yes

Tab. 9: NAND flash specifications

3.5 Memory Map

This section will be completed in a future version of this manual.

3.6 Power supply unit

DIVA, as the other LITE Line CPU modules, embeds all the

elements required for powering the unit, therefore power sequencing is self-contained and simplified. Nevertheless, power must be provided from carrier board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters. For detailed information, please refer to Section 5.1.

3.7 CPU module connectors

All interface signals provided by DIVA are routed through a 204 pin SO-DIMM connector. The host board must mount the mating connector and connect the desired peripheral interfaces according to DIVA pinout specifications.

For mechanical information, please refer to Section 4 (Mechanical specifications). For pinout and peripherals information, please refer to Sections 6 (Pinout table) and 7 (Peripheral interfaces).

4 Mechanical specifications

This chapter describes the mechanical characteristics of the DIVA module.

Mechanical drawings are available in DXF format from the DIVA page on DAVE Embedded Systems website http://http//www.dave.eu/dave-cpu-module-am335x-diva.html

4.1 Board Layout

The following figure shows the physical dimensions of the DIVA module:

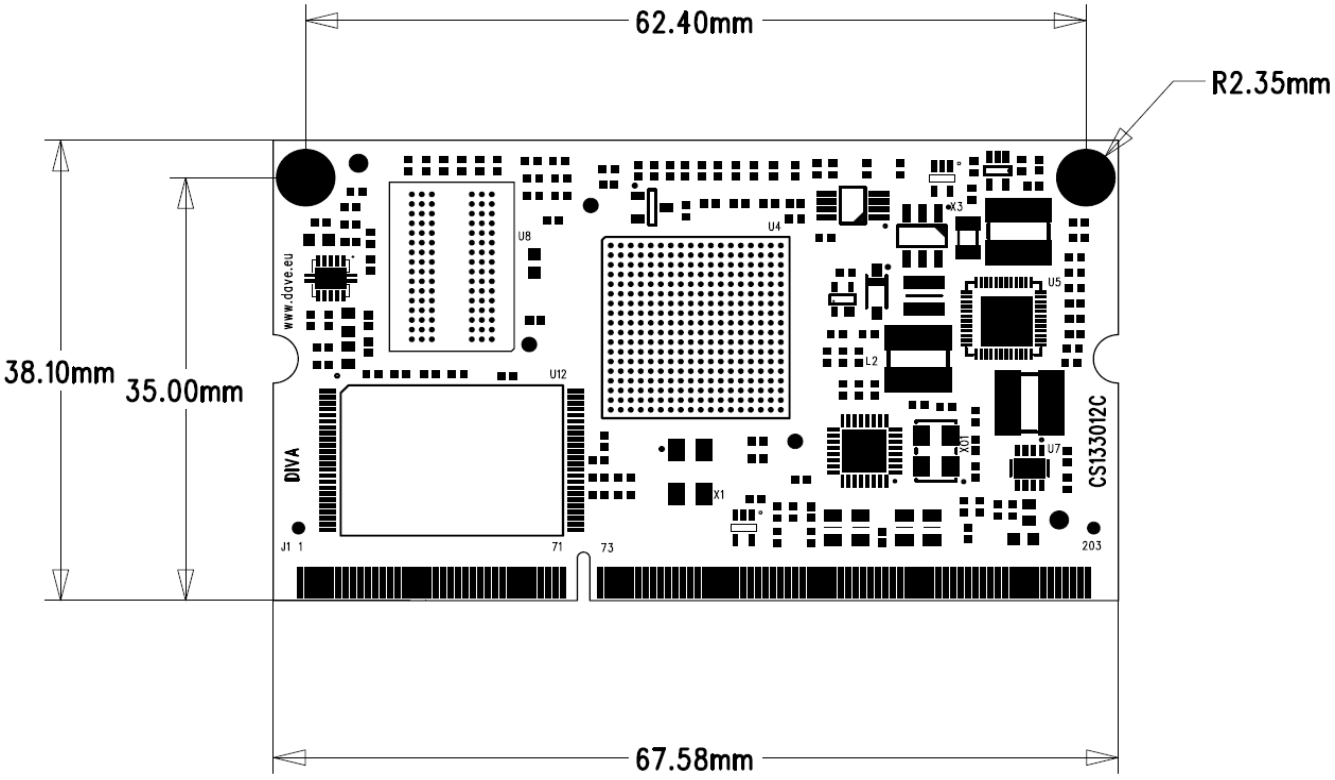


Fig. 4: Board layout - top view

- Board height: 38.3 mm

- Board width: 67.6 mm
- Height of all components is < 2.8 mm.
- PCB thickness is 1 mm.

The following figure highlights the maximum components' heights on DIVA module:

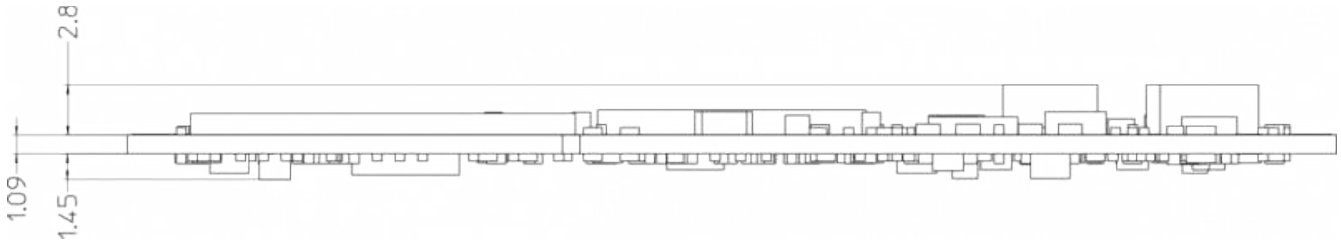


Fig. 5: DIVA module - Side view

4.2 Connectors

The following figure shows the DIVA SODIMM connector layout:

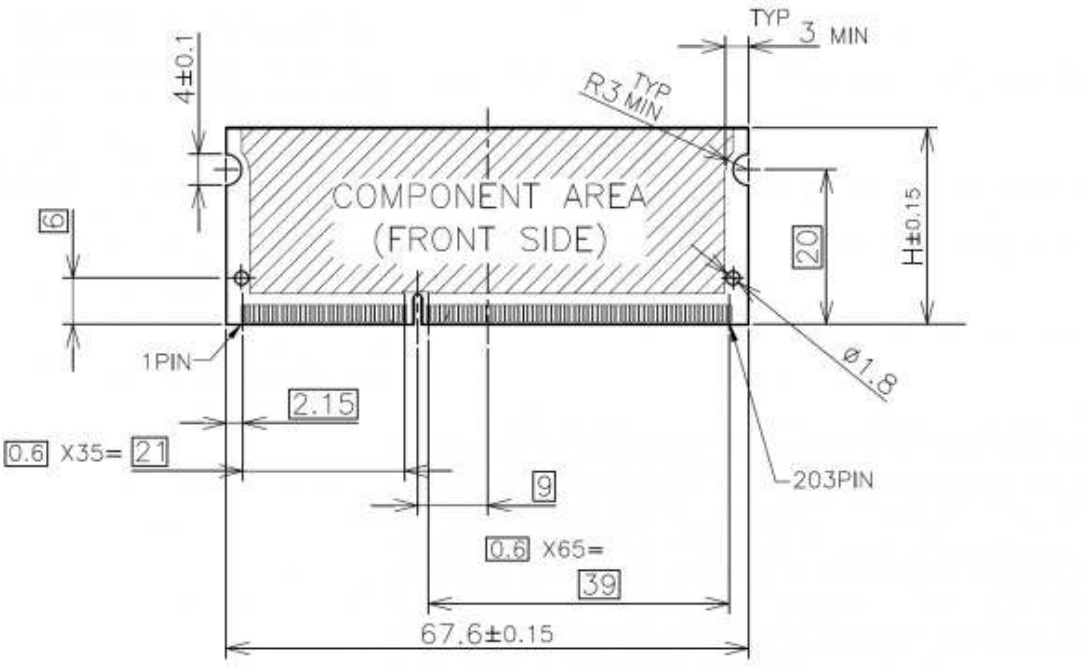


Fig. 6: Connectors layout

The following table reports the connectors specifications:

Part number	Standard SO-DIMM 204-pin (DDR3)
Mating connectors	DDR3 SO-DIMM SOCKET Part number : TE Connectivity 2013289-1 (used on DIVAEVB-Lite)

5 Power, reset and control

5.1 Power Supply Unit (PSU) and recommended power-up sequence

Implementing correct power-up sequence for AM335x processors family is not a trivial task because several power rails are involved. DIVA SOM simplifies this task and embeds all the needed circuitry. The following picture shows a

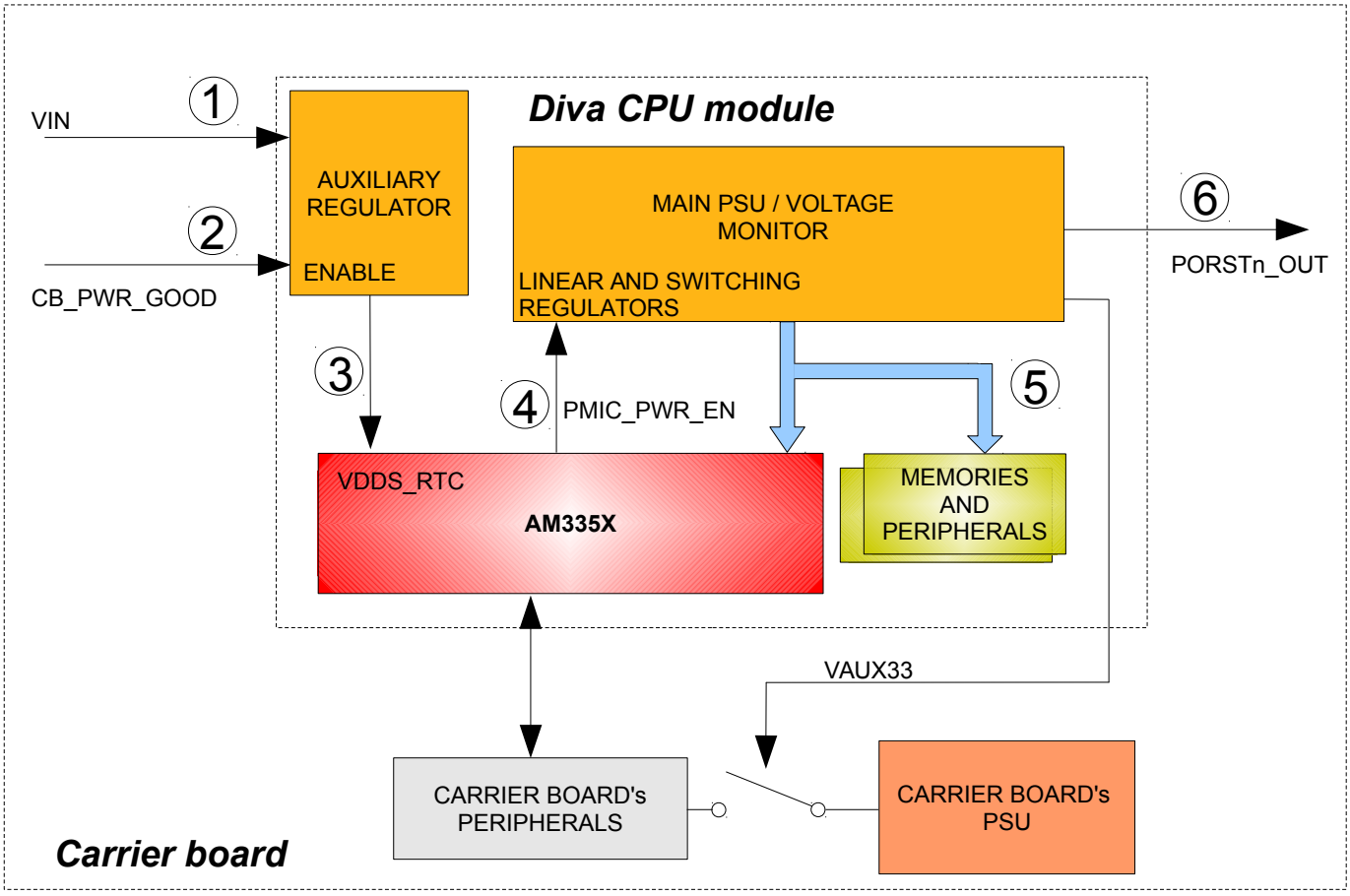


Fig. 7: DIVA power-up sequence

simplified block diagram of PSU/voltage monitoring circuitry:

The recommended power-up sequence is:

1. main power supply rail (VIN) ramps up
2. carrier board circuitry raises CB_PWR_GOOD; this indicates VIN rail is stable ([1])
3. auxiliary regulator is enabled, thus processor's VDDS_RTC domain is powered
4. processor raises PMIC_PWR_EN signal to start main PSU
5. this step is composed of two events:
   - main PSU enables several voltage rails to complete CPU, memories and peripheral power up sequence
   - VAUX33 signal is raised; this active-high signal indicates that SoM's I/O is powered. This signal can be used to manage carrier board power up sequence in order to prevent back powering (from SoM to carrier board or vice versa)
6. PORSTn_OUT signal is raised to indicate that all power rails of SOM are stable

5.2 PMIC

Main PSU subsystem of DIVA SOM is based on Power Management Integrated Circuit (PMIC) Texas Instruments TPS65910A3A1. PMIC controls processor's power up sequence and sources the majority of power rails needed by AM335x.

Once processors is booted, it can control PMIC via the I2C0 bus to:

- set all the voltage needed by CPU in all operating conditions
- set RTC and control it
- manage power modes.

Besides I2C bus, PMIC has several control signals including:

- PWRHOLD (input): This signal is connected to

1 This step is not mandatory and VIN and CB_PWR_GOOD can be connected together. CB_PWR_GOOD is provided to prevent, if necessary, DIVA's PSU to turn on during ramp of carrier board VIN rail.

processor's PMIC_PWR_EN and is used to initiate power up sequence.

- PMIC_PWRON (input): A rising edge of this pin (automatically done at startup) the PMIC performs an OFF-to-ACTIVE state transition. On a falling edge of this pin, the PMIC performs an ACTIVE-to-OFF state transition. This signal is pulled-up to VIN through 10kOhm resistor.

5.3 Reset scheme and voltage monitoring

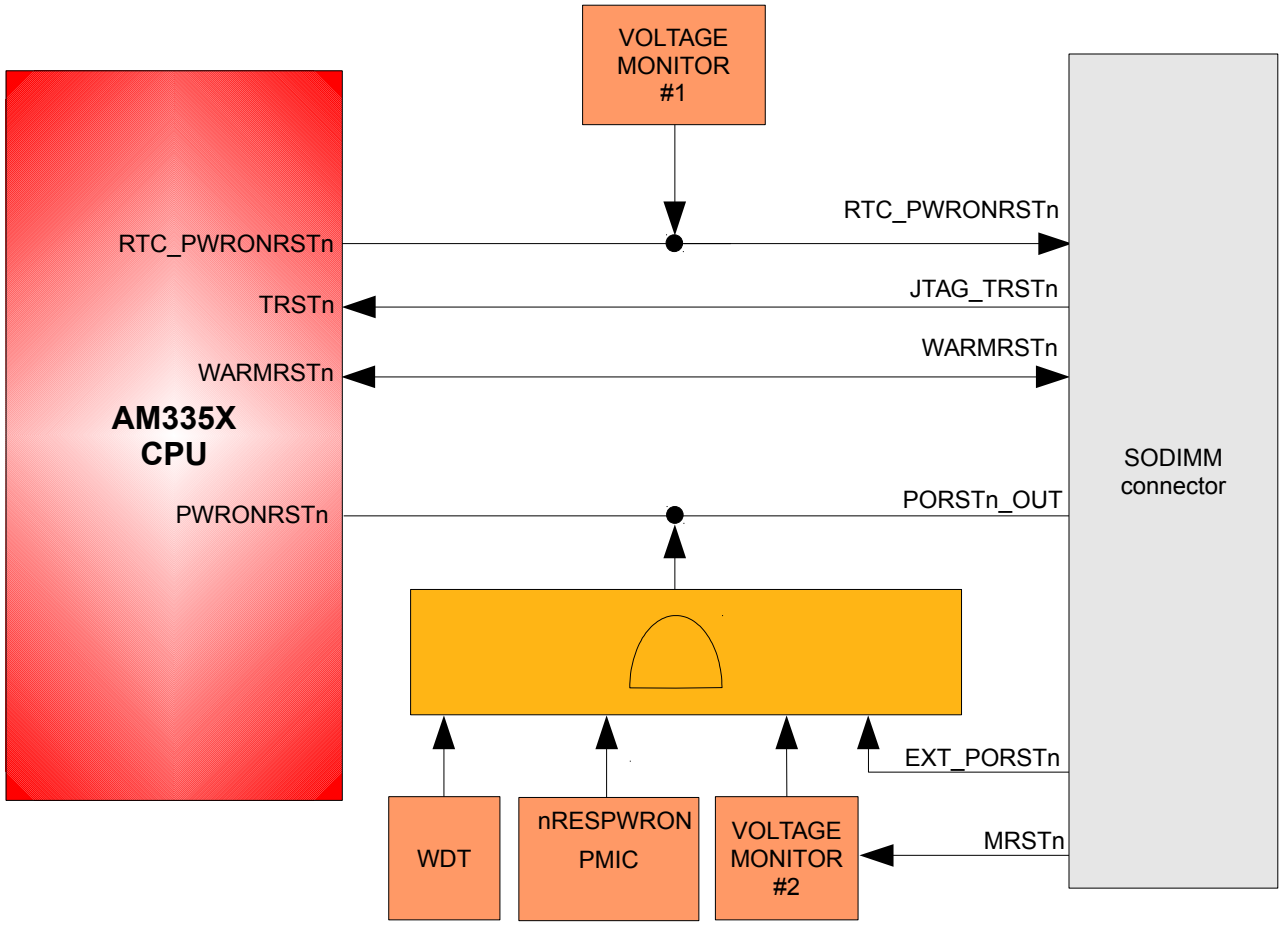


Fig. 8: DIVA Reset scheme

DIVA implements a flexible reset scheme that offers several different solutions for system integrators at carrier board level. The following picture shows a diagram of the reset scheme:

Apart from processor, there are four reset sources on DIVA SOM:

1. voltage monitor #1
   - this device monitors VDDS_RTC power rail and acts on processor's RTC_PWRONRSTn signal
2. voltage monitor #2
   - this device monitors processor's I/O power rail (3.3V) and acts on processor's PWRONRSTn signal
3. watchdog timer (please note that this watchdog timer has nothing to do with AM335x watchdog)
   - this optional device (Maxim MAX6373KA+) acts on processor's PWRONRSTn signal
4. PMIC
   - PMIC's nRESPWRON ouput acts on processor's PWRONRSTn signal.

In case a reset is issued by sources 2, 3 or 4 - eg. as consequence of a voltage glitch on power rail - or by an external source via EXT_PORSTn signal, non-volatile memories are protected against spurious write operations that might occur.

Some of these reset signals are accessible by carrier board circuitry as described below.

5.3.1 EXT_PORSTn (J1.199)

The EXT_PORSTn signal is an open-drain system reset input. When issued, a complete reset is done of all DIVA SOM circuitry. Note that the power sequence is not retriggered when a system reset is performed. Only CPU and peripherals on module are reset when this pin is in low state and they remain in reset state while the EXT_PORSTn remains low. When the board is powered up, EXT_PORSTn is automatically asserted by DIVA reset circuitry.

EXT_PORSTn is pulled-up to processor's I/O voltage (3.3V) with 10kOhm resistor.

5.3.2 PORSTn_OUT (J1.170)

PORSTn_OUT is an active-low push-pull ouput signal. PORSTn_OUT is asserted whenever any of the following conditions are met:

- EXT_PORSTn is asserted
- watchdog timer reset is asserted
- voltage monitor #2 reset is asserted
- PMIC_nRESPWRON is asserted

PORSTn_OUT is connected to processor's PWRONRSTn (also known as PORZ) signal.

PORSTn_OUT is pulled-down with 10kOhm resistor.

5.3.3 WARMRSTn (J1.197)

WARMRSTn is an active-low open-drain bidirectional signal. It is connected to processor's WARMRSTn (aka nRESETIN_OUT) signal and it is asserted by processor itself as described by AM335x Technical Reference Manual.

WARMRSTn is pulled-up to processor's I/O voltage (3.3V) with 10kOhm resistor.

5.3.4 RTC_PWRONRSTn (J1.195)

RTC_PORZ signal is connected to processor's RTC_PWRONRSTn signal. It is an output-only signal, pulled-down with 100kOhm resistor. It only affects processor's RTC operations and registers.

5.3.5 JTAG_TRSTn (J1.135)

JTAG_TRSTn is the test and emulation logic reset input. It is pulled-down with 10kOhm resistor.

5.3.6 PMIC_nRESPWRON (J1.191)

PMIC_nRESPWRON is push-pull output signal. It is connected to PMIC's nRESPWRON. It is asserted by PMIC and acts on PORSTn_OUT signal. PMIC_nRESPWRON is pulled-down with

10kOhm resistor. For more details please refer to PMIC Data Manual.

5.3.7 MRSTn (J1.193)

MRSTn is connected to the RESET IN input of the voltage monitor #2 (Maxim MAX6389XS31D3+T). This signal is compared to the voltage monitor internal +1.27V reference. If the voltage at RESET IN is less than 1.27V, reset asserts.

MRSTn is pulled-up to processor's I/O voltage (3.3V) with 10kOhm resistor.

5.4 Boot options

AM335x processor provides several boot sequences selectable via BTMODE[15:0] bootstrap pins. In order to fully understand how boot works on DIVA platform, please refer to chapter 26 ("Initialization") of the AM335x Technical Reference Manual.

Function	Boot signals	Default config	Selection
Crystal frequency	SYSBOOT[15:14]	01	24 MHz
Reserved	SYSBOOT[13:12]	00	Normal operation
XIP/NAND boot	SYSBOOT[11:10]	00	Non-muxed device
NAND ECC / WAIT	SYSBOOT[9]	0	ECC by ROM
Bus width	SYSBOOT[8]	0	8 bit device
EMAC Phy mode	SYSBOOT[7:6]	01	RMII
CLKOUT1	SYSBOOT[5]	0	CLKOUT1 disabled
Boot sequence	SYSBOOT[4:0]	10111	MMC0/SPI0/UART0

SYSBOOT[15:0] terminals are respectively LCD_DATA[15:0] inputs, latched on the rising edge of PWRONRSTn. The booting device list is created based on the SYSBOOT pins. A booting device can be a memory booting device (soldered flash memory or temporarily booting device like memory card) or a peripheral interface connected to a host. The main loop of the booting procedure goes through the booting device list and tries to search for an image from the currently selected booting device. This loop is exited if a valid booting image is found and

successfully executed or upon watchdog expiration. The memory booting procedure is executed when the booting device type is one of NOR, NAND, MMC or SPI-EEPROM. The peripheral booting is executed when the booting device type is Ethernet, USB or UART.

5.4.1 Default boot configuration

The default DIVA boot sequence is configured through a pull-up/pull-down resistors network. The following table describes the default boot signals (SYSBOOT[15:0]) configuration:

With these settings, the default boot sequence is:

1. MMC0
2. SPI0
3. UART0

The internal bootrom tries each boot mode in sequence and stops when it finds a valid boot code.

Assuming that:

- default configuration is not changed,
- no boot MMC card is connected to processor's MMC0 interface,
- there's a valid boot code programmed in SPI memory

the actual boot sequence performed by ARM core will be:

1. bootrom: this is executed from internal ROM code memory
2. U-Boot 1. bootloader (1st stage) is
   - copied from on-board NOR flash memory connected to SPI0 port to on-chip SRAM by bootrom
   - executed from on-chip SRAM
3. U-Boot bootloader (2nd stage) is
   - copied by U-Boot 1st stage from NOR flash memory connected to SPI0 port to SDRAM
   - executed from SDRAM.

If no boot code is available in SPI NOR flash (for the bootrom this means that the first sector read returns 0xFFFFFFFF) the bootrom tries UART0 peripheral booting.

5.4.2 Boot sequence customization

DIVA default boot sequence can be changed by optional external circuitry implemented on the carrier board.

5.5 Clock scheme

This section will be completed in a future version of this manual.

5.6 Recovery

For different reason, starting from image corruption due power loss during upgrade or unrecoverable bug while developing a new U-Boot feature, the user will need, sooner or later, to recover (bare-metal restore) the DIVA SOM without using the bootloader itself. The following paragraphs introduce the available options. For further information, please refer to **DAVE Embedded Systems** Developers Wiki or contact the Technical Support Team.

5.6.1 JTAG Recovery

JTAG recovery, though very useful (especially in development or production environment), requires dedicated hardware and software tools. DIVA provides the JTAG interface, which, besides the debug purpose, can be used for programming and recovery operations. For further information on how to use the JTAG interface, please contact the Technical Support Team.

5.6.2 UART Recovery

UART recovery does not requires any specialized hardware, apart a PC and a DB9 serial cross cable. The boot sequence must include the UART option and a way to enable it. Then a simple procedure allow to load the 1st and 2nd stage bootloader from the serial line. When the 2nd stage bootloader

is running, reprogramming the flash memory is straightforward.

*The UART boot uses **UART0** interface.*

5.6.3 SD/MMC Recovery

MMC recovery is a valuable option that requires no special hardware at all, apart a properly formatted MMC. The boot sequence must include the SD/MMC option and a way to enable it. When SD/MMC boot option is selected, bootrom looks for a valid boot sector on SD/MMC0. Once the board is running after booting from SD, reprogramming the flash memory is straightforward.

5.7 Multiplexing

AM335x pins can have up to eight alternate function modes. The I/O pins can be internally routed to/from one of several peripheral modules within the device: this routing is referred to as Pin Multiplexing. Pin Multiplexing allows software to choose the subset of internal signals which will be mapped to balls of the device for a given application. Pin multiplexing selects which one of several peripheral pin functions controls the pin's I/O buffer output data values.

Please note that pin mux configuration is a very critical step. Wrong configuration may lead to system instability, side effects or even damage the hardware permanently

Pin multiplexing configuration is quite complex in DIVA but a tool from TI, the Pin Mux Utility, can help to perform this operation. Software installation and generic usage documentation is available on this page of the TI Embedded Processors Wiki:
http://processors.wiki.ti.com/index.php/Pin_Mux_Utility_for_ARM_MPU_Processors

5.8 RTC

The TPS65910A3 PMIC provides a real-time clock (RTC) resource with:

- Oscillator for 32.768-kHz crystal
- Date, time and calendar
- Alarm capability
- Backup power from external battery

Backup power is provided through the PMIC_VBACKUP (J1.203) signal. If not used, PMIC_VBACKUP must be externally connected to PMIC.VCC5 (VIN).

For a detailed description of RTC characteristics, please refer to the TPS65910A3 PMIC datasheet.

5.9 Watchdog

An external watchdog (MAX6373 device) is connected to the AM335X_GMII1_TXD2 (J1.159) signal. During normal operation, the microprocessor should repeatedly toggle the watchdog input WDI (AM335X_GMII1_TXD2) before the selected watchdog timeout period elapses to demonstrate that the system is processing code properly. If the µP does not provide a valid watchdog input transition before the timeout period expires, the supervisor asserts a watchdog (WDO) output to signal that the system is not executing the desired instructions within the expected time frame. The watchdog output pulse is used to reset the µP.

The MAX6373 watchdog timer is pin-selectable and the timer can be configured through the WD_SET0 (J1.7), WD_SET1 (J1.9) and WD_SET2 (J1.11) signals. As a default, the watchdog is configured through a pull-up/pull-down resistors network (WD_SET[2..0] = 110) that keeps the watchdog timer inactive at startup. Startup delay ends when WDI sees its first level transition. The default watchdog timeout period is 10 s.

The configuration can be changed by optional external circuitry implemented on the carrier board.

6 Pinout table

This chapter contains the pinout description of the SO-DIMM-204 edge connector of the DIVA module. The following table reports the pin mapping of the module signals routed to the J1 204 connector's pins.

Each row in the pinout tables contains the following information:

Pin	Reference to the connector pin
Pin Name	Pin (signal) name on the DIVA connector
Internal Connections	Connections to the DIVA components: CPU.<x> : pin connected to CPU pad named <x> PMIC.<x> : pin connected to the Power Manager IC ETHPHY.<x> : pin connected to the LAN PHY WDT.<x>: pin connected to the MAX6373 watchdog EEPROM.<x> : pin connected to the EEPROM
Ball/pin #	Component ball/pin number connected to signal
Supply Group	Power Supply Group
Type	Pin type: I = Input, O = Output, Z = High impedance, S = Supply voltage, G = Ground, A = Analog signal
Voltage	I/O voltage

The **Internal connection** column reports the name of the microprocessor signal, which in turn contains references to all the peripheral functions that can be associated to that pin. For example, the following pin name

CPU.
[I2C0_SCL/TIMER7/UART2_RTSN/ECAP1_IN_PWM1_OUT////GPIO3_6]

means that the pin can be used as:

- I2C0_SCL: I2C channel 0, clock signal
- TIMER7: timer signal 7
- UART2_RTSN: UART port 2, Request to Send signal
- ECAP1_IN_PWM1_OUT: Enhanced Capture 1 input or Auxiliary PWM1 output

- GP3_6: General Purpose I/O port 3, channel 6

The following table reports all the function names that can be found on the **Internal connection** and the associated description.

Function name	Description
EMACx	Ethernet MAC. “x” represents the port number (0 or 1)
UARTx	UART port. “x” represents the port number (0 to 5)
GPIOx_y	General Purpose I/O port. “x” represents the port number (0 to 3)
SPIx	SPI channel. “x” represents the channel number (0 to 3)
DCANx	Controller Area Network module. “x” represents the module number (0 to 1)
MMCx	MMC/SD/SDIO interfaces. “x” represents the interface number (0 to 2)
MCAx	Multi-Channel Audio Serial Port (McASP). “x” represents the port number (0 to 5)
I2Cx	I2C channel. “x” represents the channel number (0 to 3)

6.1 Carrier board mating connector J1

Pin	Pin Name	Internal Connections	Ball/ pin #	Supply Group	Type	Voltage	Note
1	DGND	DGND	-				
2	AM335X_GPMC_WPn	CPU. [GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MII1_TXEN/UART4_TXD/GPIO0_31]	U17				
3	AM335X_I2C0_SCL	CPU. [I2C0_SCL/TIMER7/UART2_RTSN/ECAP1_IN_PWM1_OUT////GPIO3_6]	C16				Internally connected to a 10K pull-up resistor
4	AM335X_GPMC_CS0n	CPU.[GPMC_CSN0///////GPIO1_29]	V6				Internally connected to the NAND flash (if present)
5	AM335X_I2C0_SDA	CPU. [I2C0_SDA/TIMER4/UART2_CTSN/ECAP2_IN_PWM2_OUT////GPIO3_5]	C17				Internally connected to a 10K pull-up resistor
6	AM335X_GPMC_CS1n	CPU. [GPMC_CSN1/GPMC_CLK/MMC1_CLK/PR1_EDIO_DATA_IN6/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30]	U9				
7	WD_SET0	WDT.SET0	4				
8	AM335X_GPMC_CS2n	CPU. [GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31]	V9				
9	WD_SET1	WDT.SET1	5				
10	AM335X_GPMC_CS3n	CPU. [GPMC_CSN3///MMC2_CMD/PR1_MII0_CRS/PR1_MDIO_DATA/EMU4/GPIO2_0]	T13				
11	WD_SET2	WDT.SET2	6				
12	DGND	DGND	-				
13	EEPROM_WP	EEPROM.WP	7				

14	AM335X_GPMC_CLK	CPU.[GPMC_CLK/LCD_MEMORY_CLK/GPMC_WAIT1/MMC2_CLK/PR1_MII1_CRS/PR1_MDIO_MDCLK/MCASP0_FSR/GPIO2_1]	V12				
15	EEPROM_A1	EEPROM.A1	2				
16	AM335X_GPMC_WEn	CPU.[GPMC_WEN//TIMER6/////GPIO2_4]	U6				Internally connected to the NAND flash (if present)
17	EEPROM_A0	EEPROM.A0	1				
18	AM335X_GPMC_OEn_REn	CPU.[GPMC_OEN_REN//TIMER6/////GPIO2_4]	T7				Internally connected to the NAND flash (if present)
19	AM335X_EXT_WAKEUP	CPU.EXT_WAKEUP	C5				
20	AM335X_GPMC_ADVn_ALE	CPU.[GPMC_ADVN_ALE//TIMER4/////GPIO2_2]	R7				Internally connected to the NAND flash (if present)
21	DGND	DGND	-				
22	AM335X_GPMC_BE0n_CLE	CPU.[GPMC_BE0N_CLE//TIMER5/////GPIO2_5]	T6				Internally connected to the NAND flash (if present)
23	AM335X_RMII1_REFCLK		H18				HW option (not connected by default)
24	AM335X_GPMC_BE1n	CPU.[GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28]	U18				
25	AM335X_UART0_TXD	CPU.[UART0_TXD/SPI1_CS1/DCAN0_RX/I2C2_SCL/ECAP1_IN_PWM1_OUT/PR1_PRU1_PRU_R30_15/PR1_PRU1_PRU_R31_15/GPIO1_11]	E16				
26	AM335X_GPMC_WAIT	CPU.[GPMC_WAIT0/GMII2_CRS/GPMC_CSN4/RMII2_CRS_DV/MMC1_SDCD/PR1_MII1_COL/UART4_RXD/GPIO0_30]	T17				Internally connected to the NAND flash (if present)
27	AM335X_UART0_RXD	CPU.[UART0_RXD/SPI1_CS0/DCAN0_TX/I2C2_SDA/ECAP2_IN_PWM2_OUT/PR1_PRU1_PRU_R30_14/PR1_PRU1_PRU_R31_14/GPIO1_10]	E15				
28	AM335X_GPMC_A0	CPU.[GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16]	R13				
29	AM335X_UART0_RTSn	CPU.[UART0_RTSN/UART4_TXD/DCAN1_RX/I2C1_	E17				

		SCL/SPI1_D1/SPI1_CS0/PR1_EDC_SYNC1_OUT/GPIO1_9]					
30	AM335X_GPMC_A1	CPU.[GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/PR1_MII1_TXD3/EHRPWM0_SYNCO/GPIO1_17]	V14				
31	AM335X_UART0_CTSn	CPU.[UART0_CTSN/UART4_RXD/DCAN1_TX/I2C1_SDA/SPI1_D0/TIMER7/PR1_EDC_SYNC0_OUT/GPIO1_8]	E18				
32	DGND	DGND	-				
33	AM335X_UART1_TXD	CPU.[UART1_TXD/MMC2_SDWP/DCAN1_RX/I2C1_SCL//PR1_UART0_TXD/PR1_PRU0_PRU_R31_16/GPIO0_15]	D15				
34	AM335X_GPMC_A2	CPU.[GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/PR1_MII1_TXD2/EHRPWM1A/GPIO1_18]	U14				
35	AM335X_UART1_RXD	CPU.[UART1_RXD/MMC1_SDWP/DCAN1_TX/I2C1_SDA//PR1_UART0_RXD/PR1_PRU1_PRU_R31_16/GPIO0_14]	D16				
36	AM335X_GPMC_A3	CPU.[GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/PR1_MII1_TXD1/EHRPWM1B/GPIO1_19]	T14				
37	AM335X_UART1_RTSn	CPU.[UART1_RTSN/TIMER5/DCAN0_RX/I2C2_SCL/SPI1_CS1/PR1_UART0_RTS_N/PR1_EDC_LATCH1_IN/GPIO0_13]	D17				
38	AM335X_GPMC_A4	CPU.[GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20]	R14				
39	AM335X_UART1_CTSn	CPU.[UART1_CTSN/TIMER6/DCAN0_TX/I2C2_SDA/SPI1_CS0/PR1_UART0_CTS_N/PR1_EDC_LATCH0_IN/GPIO0_12]	D18				

40	AM335X_GPMC_A5	CPU. [GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21]	V15				
41	DGND	DGND	-				
42	AM335X_GPMC_A6	CPU. [GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22]	U15				
43	AM335X_SPI0_SCLK	CPU. [SPI0_SCLK/UART2_RXD/I2C2_SDA/EHRPWM0A/PR1_UART0_CTS_N/PR1_EDIO_SOF/EMU2/GPIO0_2]	A17				Internally connected to the NOR SPI flash (if present)
44	AM335X_GPMC_A7	CPU. [GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23]	T15				
45	AM335X_SPI0_D0	CPU. [SPI0_D0/UART2_TXD/I2C2_SCL/EHRPWM0B/PR1_UART0_RTS_N/PR1_EDIO_LATCH_IN/EMU3/GPIO0_3]	B17				Internally connected to the NOR SPI flash (if present)
46	AM335X_GPMC_A8	CPU. [GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24]	V16				
47	AM335X_SPI0_D1	CPU. [SPI0_D1/MMC1_SDWP/I2C1_SDA/EHRPWM0_TRIPZONE_INPUT/PR1_UART0_RXD/PR1_EDIO_DATA_IN0/PR1_EDIO_DATA_OUT0/GPIO0_4]	B16				Internally connected to the NOR SPI flash (if present)
48	AM335X_GPMC_A9	CPU. [GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25]	U16				
49	AM335X_SPI0_CS0	CPU. [SPI0_CS0/MMC2_SDWP/I2C1_SCL/EHRPWM0_SYNCI/PR1_UART0_TXD/PR1_EDIO_DATA_IN1/PR1_EDIO_DATA_OUT1/GPIO0_5]	A16				Internally connected to the NOR SPI flash (if present)
50	AM335X_GPMC_A10	CPU.	T16				

		[GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/PR1_MII1_RXDV/MCASP0_AXR0/GPIO1_26]					
51	AM335X_SPI0_CS1	CPU.[SPI0_CS1/UART3_RXD/ECAP1_IN_PWM1_OUT/MMC0_POW/XDMA_EVENT_INTR2/MMC0_SDCD/EMU4/GPIO0_6]	C15				
52	DGND	DGND	-				
53	USB0_CE	CPU.USB0_CE	M15				
54	AM335X_GPMC_A11	CPU.[GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27]	V17				
55	USB0_ID	CPU.USB0_ID	P16				
56	AM335X_GPMC_AD0	CPU.[GPMC_AD0/MMC1_DAT0//////GPIO1_0]	U7				Internally connected to the NAND flash (if present)
57	USB0_DP	CPU.USB0_DP	N17				
58	AM335X_GPMC_AD1	CPU.[GPMC_AD1/MMC1_DAT1//////GPIO1_1]	V7				Internally connected to the NAND flash (if present)
59	USB0_DM	CPU.USB0_DM	N18				
60	AM335X_GPMC_AD2	CPU.[GPMC_AD2/MMC1_DAT2//////GPIO1_2]	R8				Internally connected to the NAND flash (if present)
61	DGND	DGND	-				
62	AM335X_GPMC_AD3	CPU.[GPMC_AD3/MMC1_DAT3//////GPIO1_3]	T8				Internally connected to the NAND flash (if present)
63	USB0_DRVVBUS	CPU.USB0_DRVVBUS	F16				
64	AM335X_GPMC_AD4	CPU.[GPMC_AD4/MMC1_DAT4//////GPIO1_4]	U8				Internally connected to the NAND flash (if present)
65	VUSB_VBUS0	CPU.USB0_VBUS	P15				
66	AM335X_GPMC_AD5	CPU.[GPMC_AD5/MMC1_DAT5//////GPIO1_5]	V8				Internally connected to the NAND flash (if present)
67	AM335x_EXTINTn	CPU.NMIn	B18				
68	AM335X_GPMC_AD6	CPU.[GPMC_AD6/MMC1_DAT6//////GPIO1_6]	R9				Internally connected to the NAND flash (if present)
69	AM335X_XDMA_EVENT_INTR0	CPU.[XDMA_EVENT_INTR0//TIMER4/CLKOUT1/SPI1_CS1/PR1_PRU1_PRU_R31_16/EMU2/GPIO0_19]	A15				

70	AM335X_GPMC_AD7	CPU.[GPMC_AD7/MMC1_DAT7//////GPIO1_7]	T9				Internally connected to the NAND flash (if present)
71	AM335X_XDMA_EVENT_INTR1	CPU.[XDMA_EVENT_INTR1//TCLKIN/CLKOUT2/TIMER7/PR1_PRU0_PRU_R31_16/EMU3/GPIO0_20]	D14				
72	DGND	DGND	-				
73	USB1_CE	CPU.USB1_CE	P18				
74	AM335X_GPMC_AD8	CPU.[GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2A/PR1_MII_MT0_CLK//GPIO0_22]	U10				
75	USB1_ID	CPU.USB1_ID	P17				
76	AM335X_GPMC_AD9	CPU.[GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/PR1_MII0_COL//GPIO0_23]	T10				
77	USB1_DP	CPU.USB1_DP	R17				
78	AM335X_GPMC_AD10	CPU.[GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN//GPIO0_26]	T11				
79	USB1_DM	CPU.USB1_DM	R18				
80	AM335X_GPMC_AD11	CPU.[GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/EHRPWM2_SYNCO/PR1_MII0_TXD3//GPIO0_27]	U12				
81	DGND	DGND	-				
82	AM335X_GPMC_AD12	CPU.[GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12]	T12				
83	USB1_DRVVBUS	CPU.USB1_DRVVBUS	F15				
84	AM335X_GPMC_AD13	CPU.[GPMC_AD13/LCD_DATA18/MMC1_DAT5/MMC2_DAT1/EQEP2B_IN/PR1_MII0_TXD1/PR1_PRU0_PRU_R30_15/GPIO1_13]	R12				
85	VUSB_VBUS1	CPU.USB1_VBUS	T18				
86	AM335X_GPMC_AD14	CPU.	V13				

		[GPMC_AD14/LCD_DATA17/MMC1_DAT6/MMC2_DAT2/EQEP2_INDEX/PR1_MII0_TXD0/PR1_PRU0_PRU_R31_14/GPIO1_14]					
87	AM335X_AIN0	CPU.AIN0	B6				
88	AM335X_GPMC_AD15	CPU.[GPMC_AD15/LCD_DATA16/MMC1_DAT7/MMC2_DAT3/EQEP2_STROBE/PR1_ECAP0_ECAP_CAPIN_APWM_O/PR1_PRU0_PRU_R31_15/GPIO1_15]	U13				
89	AM335X_AIN1	CPU.AIN1	C7				
90	AM335X_LCD_PCLK	CPU.[LCD_PCLK/GPMC_A10/PR1_MII0_CRS/PR1_EDIO_DATA_IN4/PR1_EDIO_DATA_OUT4/PR1_PRU1_PRU_R30_10/PR1_PRU1_PRU_R31_10/GPIO2_24]	V5				
91	AM335X_AIN2	CPU.AIN2	B7				
92	DGND	DGND	-				
93	AGND_TSC	AGND	-				
94	AM335X_LCD_VSYNC	CPU.[LCD_VSYNC/GPMC_A8//PR1_EDIO_DATA_IN2/PR1_EDIO_DATA_OUT2/PR1_PRU1_PRU_R30_8/PR1_PRU1_PRU_R31_8/GPIO2_22]	U5				
95	AM335X_AIN3	CPU.AIN3	A7				
96	AM335X_LCD_HSYNC	CPU.[LCD_HSYNC/GPMC_A9//PR1_EDIO_DATA_IN3/PR1_EDIO_DATA_OUT3/PR1_PRU1_PRU_R30_9/PR1_PRU1_PRU_R31_9/GPIO2_23]	R5				
97	AM335X_AIN4	CPU.AIN4	C8				
98	AM335X_LCD_AC_BIAS_EN	CPU.[LCD_AC_BIAS_EN/GPMC_A11/PR1_MII1_CRS/PR1_EDIO_DATA_IN5/PR1_EDIO_DATA_OUT5/PR1_PRU1_PRU_R30_11/PR1_PRU1_PRU_R31_11/GPIO2_25]	R6				
99	AM335X_AIN5	CPU.AIN5	B8				
100	AM335X_LCD_DATA0	CPU.[LCD_DATA0/GPMC_A0/PR1_MII_MT0_CLK/EHRPWM2A//PR1_PRU1_PRU_R30_0/PR1_PRU1_PRU_R31_0/GPIO2_6]	R1				
101	AGND_TSC	AGND	-				

102	AM335X_LCD_DATA1	CPU.[LCD_DATA1/GPMC_A1/PR1_MII0_TXEN/EHRPWM2B//PR1_PRU1_PRU_R30_1/PR1_PRU1_PRU_R31_1/GPIO2_7]	R2				
103	AM335X_AIN6	CPU.AIN6	A8				
104	AM335X_LCD_DATA2	CPU.[LCD_DATA2/GPMC_A2/PR1_MII0_TXD3/EHRPWM2_TRIPZONE_INPUT//PR1_PRU1_PRU_R30_2/PR1_PRU1_PRU_R31_2/GPIO2_8]	R3				
105	AM335X_AIN7	CPU.AIN7	C9				
106	AM335X_LCD_DATA3	CPU.[LCD_DATA3/GPMC_A3/PR1_MII0_TXD2/EHRPWM2_SYNCI_O//PR1_PRU1_PRU_R30_3/PR1_PRU1_PRU_R31_3/GPIO2_9]	R4				
107	AGND_TSC	AGND					
108	AM335X_LCD_DATA4	CPU.[LCD_DATA4/GPMC_A4/PR1_MII0_TXD1/EQEP2A_IN//PR1_PRU1_PRU_R30_4/PR1_PRU1_PRU_R31_4/GPIO2_10]	T1				
109	AM335X_ECAP0_IN_PWM0_OUT	CPU.[ECAP0_IN_PWM0_OUT/UART3_TXD/SPI1_CS1/PR1_ECAP0_ECAP_CAPIN_APWM_O/SPI1_SCLK/MMC0_SDWP/XDMA_EVENT_INTR2/GPIO0_7]	C18				
110	AM335X_LCD_DATA5	CPU.[LCD_DATA5/GPMC_A5/PR1_MII0_TXD0/EQEP2B_IN//PR1_PRU1_PRU_R30_5/PR1_PRU1_PRU_R31_5/GPIO2_11]	T2				
111	AM335X_MMC_D3	CPU.[MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26]	F17				
112	DGND	DGND	-				
113	AM335X_MMC_D2	CPU.[MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27]	F18				
114	AM335X_LCD_DATA6	CPU.[LCD_DATA6/GPMC_A6/PR1_EDIO_DATA_IN6/	T3				

		EQEP2_INDEX/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/GPIO2_12]					
115	AM335X_MMC_D1	CPU.[MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28]	G15				
116	AM335X_LCD_DATA7	CPU.[LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/GPIO2_13]	T4				
117	AM335X_MMC_D0	CPU.[MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29]	G16				
118	AM335X_LCD_DATA8	CPU.[LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/MCASP0_ACLKX/UART5_TXD/PR1_MII0_RXD3/UART2_CTSN/GPIO2_14]	U1				
119	AM335X_MMC_CMD	CPU.[MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31]	G18				
120	AM335X_LCD_DATA9	CPU.[LCD_DATA9/GPMC_A13/EHRPWM1_SYNCO/MCASP0_FSX/UART5_RXD/PR1_MII0_RXD2/UART2_RTSN/GPIO2_15]	U2				
121	DGND	DGND	-				
122	AM335X_LCD_DATA10	CPU.[LCD_DATA10/GPMC_A14/EHRPWM1A/MCASP0_AXR0//PR1_MII0_RXD1/UART3_CTSN/GPIO2_16]	U3				
123	AM335X_MMC_CLK	CPU.[MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30]	G17				
124	AM335X_LCD_DATA11	CPU.[LCD_DATA11/GPMC_A15/EHRPWM1B/MCAS	U4				

		P0_AHCLKR/MCASP0_AXR2/PR1_MII0_RXD0/UART3_RTSN/GPIO2_17]					
125	JTAG_EMU1	CPU.[EMU1///////GPIO3_8]	B14				
126	AM335X_LCD_DATA12	CPU.[LCD_DATA12/GPMC_A16/EQEP1A_IN/MCASP0_ACLKR/MCASP0_AXR2/PR1_MII0_RXLINK/UART4_CTSN/GPIO0_8]	V2				
127	JTAG_EMU0	CPU.[EMU0///////GPIO3_7]	C14				
128	AM335X_LCD_DATA13	CPU.[LCD_DATA13/GPMC_A17/EQEP1B_IN/MCASP0_FSR/MCASP0_AXR3/PR1_MII0_RXER/UART4_RTSN/GPIO0_9]	V3				
129	JTAG_TDO	CPU.TDO	A11				
130	AM335X_LCD_DATA14	CPU.[LCD_DATA14/GPMC_A18/EQEP1_INDEX/MCASP0_AXR1/UART5_RXD/PR1_MII_MR0_CLK/UART5_CTSN/GPIO0_10]	V4				
131	JTAG_TDI	CPU.TDI	B11				
132	DGND	DGND	-				
133	JTAG_TMS	CPU.TMS	C11				
134	AM335X_LCD_DATA15	CPU.[LCD_DATA15/GPMC_A19/EQEP1_STROBE/MCASP0_AHCLKX/MCASP0_AXR3/PR1_MII0_RXDV/UART5_RTSN/GPIO0_11]	T5				
135	JTAG_TRSTn	CPU.TRSTn	B10				
136	AM335X_MCASP0_FSR	CPU.[MCASP0_FSR/EQEP0B_IN/MCASP0_AXR3/MCASP1_FSX/EMU2/PR1_PRU0_PRU_R30_5/PR1_PRU0_PRU_R31_5/GPIO3_19]	C13				
137	JTAG_TCK	CPU.TCK	A12				
138	AM335X_MCASP0_AXR1	CPU.[MCASP0_AXR1/EQEP0_INDEX//MCASP1_AXR0/EMU3/PR1_PRU0_PRU_R30_6/PR1_PRU0_PRU_R31_6/GPIO3_20]	D13				
139	ETH_CTTD						
140	AM335X_MCASP0_FSX	CPU.[MCASP0_FSX/EHRPWM0B//SPI1_D0/MMC1_SDCD/PR1_PRU0_PRU_R30_1/PR1_PRU0_PRU_R31_1/GPIO3_15]	B13				

141	DGND	DGND	-				
142	AM335X_MCASP0_AXR0	CPU.[MCASP0_AXR0/EHRPWM0_TRIPZONE_INPUT//SPI1_D1/MMC2_SDCD/PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16]	D12				
143	ETH_CTRD						
144	AM335X_MCASP0_AHCLKR	CPU.[MCASP0_AHCLKR/EHRPWM0_SYNCI_O/MCASP0_AXR2/SPI1_CS0/ECAP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/PR1_PRU0_PRU_R31_3/GPIO3_17]	C12				
145	ETH_TX-	ETHPHY.TXN	28				
146	AM335X_MCASP0_ACLKR	CPU.[MCASP0_ACLKR/EQEP0A_IN/MCASP0_AXR2/MCASP1_ACLKX/MMC0_SDWP/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18]	B12				
147	ETH_TX+	ETHPHY.TXP	29				
148	AM335X_MCASP0_AHCLKX	CPU.[MCASP0_AHCLKX/EQEP0_STROBE/MCASP0_AXR3/MCASP1_AXR1/EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21]	A14				
149	ETH_RX-	ETHPHY.RXN	30				
150	AM335X_MCASP0_ACLKX	CPU.[MCASP0_ACLKX/EHRPWM0A//SPI1_SCLK/MMC0_SDCD/PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14]	A13				
151	ETH_RX+	ETHPHY.RXP	31				
152	DGND	DGND	-				
153	EMAC0_PHY_LED_SPEED	ETHPHY.LED2/nINTSEL	2				10kOhm pull-down
154	NC/OUT_PMIC_VRTC//OUT_VDD3_SMPS//OUT_VDIG1						By default this pin must not be connected. Optionally it can route power voltages generated by DIVA PSU. This option is meant to allow monitoring of such voltages by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
155	EMAC0_PHY_LED_LINK/ACT	ETHPHY.LED1/nREGOFF	3				

156	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
157	AM335X_GMII1_TXD3	CPU. [GMII1_TXD3/DCAN0_TX/RGMII1_TD3/UART4_RXD/MCASP1_FSX/MMC2_DAT1/MCASP0_FSR/GPIO0_16]	J18				
158	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
159	AM335X_GMII1_TXD2	CPU. [GMII1_TXD2/DCAN0_RX/RGMII1_TD2/UART4_TXD/MCASP1_AXR0/MMC2_DAT2/MCASP0_AHCLKX/GPIO0_17]	K15				Internally connected to the WDT (if present) – HW option
160	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
161	DGND	DGND	-				
162	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow

							monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
163	AM335X_GMII1_RXDV	CPU. [GMII1_RXDV/LCD_MEMORY_CLK/RGMII1_RCTL/UART5_TXD/MCASP1_ACLKX/MMC2_DAT0/MCASP0_ACLKR/GPIO3_4]	J17				
164	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
165	AM335X_GMII1_MDIO_CLK	CPU. [MDIO_CLK/TIMER5/UART5_TXD/UART3_RTSN/MMC0_SDWP/MMC1_CLK/MMC2_CLK/GPIO0_1]	M18				Internally connected to the ETH PHY
166	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
167	AM335X_GMII1_MDIO_DATA	CPU. [MDIO_DATA/TIMER6/UART5_RXD/UART3_CTSN/MMC0_SDCD/MMC1_CMD/MMC2_CMD/GPIO0_0]	M17				Internally connected to the ETH PHY
168	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier

							board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
169	AM335X_GMII1_COL	CPU. [GMII1_COL/RMII2_REFCLK/SPI1_SCLK/UART5_RXD/MCASP1_AXR2/MMC2_DAT3/MCASP0_AXR2/GPIO3_0]	H16				Internally used for DDR power management (if required) – HW option
170	PORSTn_OUT						Please refer to section 5.3 for detailed information
171	AM335X_GMII1_RXD3	CPU. [GMII1_RXD3/UART3_RXD/RGMII1_RD3/MMC0_DAT5/MMC1_DAT2/UART1_DTRN/MCASP0_AXR0/GPIO2_18]	L17				
172	DGND	DGND	-				
173	AM335X_GMII1_RXD2	CPU. [GMII1_RXD2/UART3_TXD/RGMII1_RD2/MMC0_DAT4/MMC1_DAT3/UART1_RIN/MCASP0_AXR1/GPIO2_19]	L16				
174	CB_PWR_GOOD						Please refer to section 5.1 for detailed information
175	AM335X_GMII1_RXCLK	CPU. [GMII1_RXCLK/UART2_TXD/RGMII1_RCLK/MMC0_DAT6/MMC1_DAT1/UART1_DSRN/MCASP0_FSX/GPIO3_10]	L18				
176	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
177	AM335X_GMII1_TXCLK	CPU. [GMII1_TXCLK/UART2_RXD/RGMII1_TCLK/MMC0_DAT7/MMC1_DAT0/UART1_DCDN/MCASP0_ACLKX/GPIO3_9]	K18				
178	NC/Monitoring						By default this pin must not be

							connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
179	PMIC_CLK32OUT	PMIC.CLK32KOUT	PMIC.38				
180	OUT_VAUX33	PMIC.VAUX33	PMIC.4				This signal is used to power carrier board circuitry that interfaces CPU I/O directly. Please refer to section 5.1 for further details.
181	DGND	DGND	-				
182	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
183	PMIC_PWR_EN	CPU.PMIC_PWR_EN, PMIC.PWRHOLD	CPU.C6, PMIC.1				
184	NC/Monitoring						By default this pin must not be connected. Optionally it can route power voltage generated by DIVA PSU. This option is meant to allow monitoring such voltage by carrier board circuitry. It is not meant to power carrier board devices. For more information please contact technical support.
185	PMIC_INT1	PMIC.INT1	45				
186	VIN						
187	PMIC_SLEEP	PMIC.SLEEP	37				
188	VIN						
189	PMIC_PWRON	PMIC.PWRON					

190	VIN						
191	PMIC_nRESPWRON	PMIC.nRESPWRON					Please refer to section 5.3 for detailed information
192	DGND	DGND	-				
193	MRSTn						Please refer to section 5.3 for detailed information
194	VIN						
195	RTC_PWRONRSTn	CPU.RTC_PWRONRSTn	B5				Please refer to section 5.3 for detailed information
196	VIN						
197	WARMRSTn						Please refer to section 5.3 for detailed information
198	VIN						
199	EXT_PORSTn						Please refer to section 5.3 for detailed information
200	VIN						
201	DGND	DGND	-				
202	VIN						
203	PMIC_VBACKUP	PMIC.VBACKUP	27				
204	VIN						

7 Peripheral interfaces

DIVA modules implement a number of peripheral interfaces through the SO-DIMM connector. The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the DIVA module. Each signal's availability is noted in the "Notes" column on the table of each interface.

The signals for each interface are described in the related tables. The following notes summarize the column headers for these tables:

- "Pin name" – The symbolic name of each signal
- "Conn. Pin" – The pin number on the module connectors
- "Function" – Signal description
- "Notes" – This column summarizes configuration requirements and recommendations for each signal.

7.1 Programmable Real-Time Unit and Industrial Communication Subsystem

The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) consists of dual 32-bit RISC cores (Programmable Real-Time Units, or PRUs), memories, interrupt controller, and internal peripherals that enable additional peripheral interfaces and protocols. The programmable nature of the PRUs, along with their access to pins and events, provide flexibility in implementing custom peripheral interfaces, fast real-time responses, power saving techniques, specialized data handling and DMA operations, and in offloading tasks from the other processor cores of the system-on-chip (SoC).

Among the interfaces supported by the PRU-ICSS are the real-time industrial protocols used in master and slave mode, such as:

- EtherCAT®
- PROFINET
- EtherNet/IP™
- PROFIBUS
- POWERLINK
- SERCOS III

The PRU subsystem includes the following main features:

- Two PRUs each with:
  - 8KB program memory
  - 8KB data memory
  - High Performance Interface/OCP Master port for accessing external memories
- Enhanced GPIO (EGPIO) with async capture and serial support
- 12 KB general purpose shared memory
- One Interrupt Controller (INTC)
  - Up to 64 input events supported
  - Interrupt mapping to 10 interrupt channels
  - 10 Host interrupts (2 to PRU0 and PRU1, 8 output to chip level)
  - Each system event can be enabled and disabled
  - Each host event can be enabled and disabled
  - Hardware prioritization of events
- 16 software Events generation by 2 PRUs
- One Ethernet MII_RT module with two MII ports and configurable connections to PRUs*
- One MDIO Port*
- One Industrial Ethernet Peripheral (IEP) to manage/generate Industrial Ethernet functions
  - One Industrial Ethernet timer with 10 capture* and

eight compare events

- Two Industrial Ethernet sync signals*
- Two Industrial Ethernet 16-bit watchdog timers*
- Industrial Ethernet digital IOs*

- One 16550-compatible UART with a dedicated 192-MHz clock
- One Enhanced Capture Module (ECAP)
- Flexible power management support
- Integrated switched central resource (SCR) bus for connecting the various internal and external masters to the resources inside the PRU-ICSS
- Interface/OCP Slave port for external masters to access PRU-ICSS memories
- Optional address translation for PRU transaction to External Host

All memories within the PRU-ICSS support parity

7.1.1 PRU signals

All the PRU signals are routed to the J1 connector, although they are multiplexed with other signals. Please refer to the AM335x datasheet and PRU-ICSS Reference Guide for more information about PRU pinout, configuration and usage.

7.2 Ethernet ports

The AM335x 3PSW (Three Port Switch) Ethernet Subsystem provides ethernet packet communication and can be configured as an ethernet switch. It provides the gigabit media independent interface (GMII), reduced gigabit media independent interface (RGMII), reduced media independent interface (RMII), the management data input output (MDIO) for physical layer device (PHY) management. DIVA provides two ethernet ports, one Fast Ethernet with on-board PHY, and one Gigabit class MAC interface (RGMII).

7.2.1 Ethernet 10/100

On-board Ethernet PHY (SMSC LAN8710Ai) provides interface signals required to implement the 10/100 Ethernet port. It is connected to processor EMAC0 controller through RMII interface.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
EMAC0_PHY_LED_LINK/ACT	J1.155	Link activity LED Indication.	This pin is driven active when a valid link is detected and blinks when activity is detected.
EMAC0_PHY_LED_SPEED	J1.153	Link Speed LED Indication.	This pin is driven active when the operating speed is 100Mbps. It is inactive when the operating speed is 10Mbps or during line isolation.
ETH_CTTD	J1.139	Tx Center Tap	
ETH_CTRD	J1.143	Rx Center Tap	
ETH_TX-	J1.145	Transmit Negative Channel	
ETH_TX+	J1.147	Transmit Positive Channel	
ETH_RX-	J1.149	Receive Negative Channel	
ETH_RX+	J1.151	Receive Positive Channel	

7.2.2 Gigabit EMAC

DIVA provides a Gigabit class ethernet interface connected to processor EMAC1 controller through RGMII interface. When required, an external PHY must be mounted on the carrier board.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
RGMII2_RCLK	J1.44	RGMII Receive Clock	
RGMII2_RCTL	J1.30	RGMII Receive Control	
RGMII2_RD0	J1.54	RGMII Receive Data [3:0]	
RGMII2_RD1	J1.50		
RGMII2_RD2	J1.48		
RGMII2_RD3	J1.46		
RGMII2_TCLK	J1.42	RGMII Transmit Clock	
RGMII2_TCTL	J1.28	RGMII Transmit Enable	
RGMII2_TD0	J1.40	RGMII Transmit Data [3:0]	
RGMII2_TD1	J1.38		
RGMII2_TD2	J1.36		
RGMII2_TD3	J1.34		

7.3 CAN ports

DIVA provides two DCAN interfaces (DCAN0 and DCAN1) for supporting distributed realtime control with a high level of security. The DCAN interfaces implement the CAN protocol version 2.0 part A, B and supports bit rates up to 1 Mbit/s. When required, DCAN ports must be connected to external PHYs.

7.3.1 DCAN0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
DCAN0_RX	J1.25 J1.37 J1.159	DCAN0 Receive Data	
DCAN0_TX	J1.27 J1.39	DCAN0 Transmit Data	

Pin name	Conn. Pin	Function	Notes
	J1.157		

7.3.2 DCAN1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
DCAN1_RX	J1.29 J1.33 J1.119	DCAN1 Receive Data	
DCAN1_TX	J1.31 J1.35 J1.123	DCAN1 Transmit Data	

7.4 UARTs

Up to six UART ports (UART0 – UART5) are routed to DIVA connectors. UART0 provides wakeup capability. Only UART 1 provides full modem control signals. All UARTs support IrDA and CIR modes and RTS/CTS flow control (subject to pin muxing configuration).

7.4.1 UART0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Note
UART0_TXD	J1.25	Uart0 Transmit Data	
UART0_RXD	J1.27	Uart0 Receive Data	
UART0_CTSn	J1.31	Uart0 Clear To Send	
UART0_RTSn	J1.29	Uart0 Request To Send	

7.4.2 UART1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Note
UART1_TXD	J1.33	Uart1 Transmit Data	
UART1_RXD	J1.35	Uart1 Receive Data	
UART1_CTSn	J1.39	Uart1 Clear To Send	
UART1_RTSn	J1.37	Uart1 Request To Send	
UART1_DCDn	J1.111 J1.177	Uart1 Data Carrier Detect	
UART1_DSRn	J1.113 J1.175	Uart1 Data Set Ready	
UART1_DTRn	J1.115 J1.171	Uart1 Data Terminal Ready	
UART1_RIN	J1.117 J1.173	Uart1 Ring indicator	

7.4.3 UART2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Note
UART2_TXD	J1.145 J1.119 J1.175	Uart2 Transmit Data	
UART2_RXD	J1.43 J1.123 J1.177	Uart2 Receive Data	
UART2_CTSn	J1.5 J1.118	Uart2 Clear To Send	
UART2_RTSn	J1.3 J1.120	Uart2 Request To Send	

7.4.4 UART3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART3_TXD	J1.109 J1.117 J1.173	Uart3 Transmit Data	
UART3_RXD	J1.51 J1.115 J1.171	Uart3 Receive Data	
UART3_CTSn	J1.122 J1.123 J1.167	Uart3 Clear To Send	
UART3_RTSn	J1.119 J1.124 J1.165	Uart3 Request To Send	

7.4.5 UART3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART3_TXD	J1.109 J1.117 J1.173	Uart3 Transmit Data	
UART3_RXD	J1.51 J1.115 J1.171	Uart3 Receive Data	
UART3_CTSn	J1.122 J1.123 J1.167	Uart3 Clear To Send	
UART3_RTSn	J1.119 J1.124 J1.165	Uart3 Request To Send	

7.4.6 UART4

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART4_TXD	J1.2 J1.29 J1.159	Uart4 Transmit Data	
UART4_RXD	J1.26 J1.31 J1.157	Uart4 Receive Data	
UART4_CTSn	J1.111 J1.126	Uart4 Clear To Send	
UART4_RTSn	J1.113 J1.128	Uart4 Request To Send	

7.4.7 UART5

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART5_TXD	J1.23 J1.118 J1.163 J1.165	Uart5 Transmit Data	
UART5_RXD	J1.120 J1.130 J1.167 J1.169	Uart5 Receive Data	
UART5_CTSn	J1.115 J1.130	Uart5 Clear To Send	
UART5_RTSn	J1.117 J1.134	Uart5 Request To Send	

7.5 MMC/SD channels

Three standard MMC/SD/SDIO interfaces are available on DIVA module. The processor includes 3 MMC/SD/SDIO interface modules which are compliant with MMC V4.3, Secure Digital Part 1 Physical Layer Specification V2.00 and Secure Digital Input Output (SDIO) V2.00 specifications. High capacity SD cards (SDHC) are supported.

7.5.1 MMC/SD/SDIO0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
MMC0_CLK	J1.123	MMC/SD/SDIO Clock	
MMC0_CMD	J1.119	MMC/SD/SDIO Command	
MMC0_DAT0	J1.117	MMC/SD/SDIO Data bus	
MMC0_DAT1	J1.115	MMC/SD/SDIO Data bus	
MMC0_DAT2	J1.113	MMC/SD/SDIO Data bus	
MMC0_DAT3	J1.111	MMC/SD/SDIO Data bus	
MMC0_DAT4	J1.173	MMC/SD/SDIO Data bus	
MMC0_DAT5	J1.171	MMC/SD/SDIO Data bus	
MMC0_DAT6	J1.175	MMC/SD/SDIO Data bus	
MMC0_DAT7	J1.177	MMC/SD/SDIO Data bus	
MMC0_POW	J1.51 J1.23	MMC/SD Power switch control	
MMC0_SDCD	J1.51 J1.150 J1.167	MMC/SD Card Detect	
MMC0_SDWP	J1.109 J1.146 J1.165	MMC/SD Write Protect	

7.5.2 MMC/SD/SDIO 1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
MMC1_CLK	J1.6	MMC/SD/SDIO	

Pin name	Conn. Pin	Function	Notes
	J1.165	Clock	
MMC1_CMD	J1.8 J1.167	MMC/SD/SDIO Command	
MMC1_DAT0	J1.56 J1.74 J1.177	MMC/SD/SDIO Data bus	
MMC1_DAT1	J1.58 J1.76 J1.175	MMC/SD/SDIO Data bus	
MMC1_DAT2	J1.60 J1.78 J1.171	MMC/SD/SDIO Data bus	
MMC1_DAT3	J1.62 J1.80 J1.173	MMC/SD/SDIO Data bus	
MMC1_DAT4	J1.64 J1.82	MMC/SD/SDIO Data bus	
MMC1_DAT5	J1.66 J1.84	MMC/SD/SDIO Data bus	
MMC1_DAT6	J1.68 J1.86	MMC/SD/SDIO Data bus	
MMC1_DAT7	J1.70 J1.88	MMC/SD/SDIO Data bus	
MMC1_SDCD	J1.26 J1.140	MMC/SD Card Detect	
MMC1_SDWP	J1.35 J1.47	MMC/SD Write Protect	

7.5.3 MMC/SD/SDIO 2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
MMC2_CLK	J1.14 J1.165	MMC/SD/SDIO Clock	
MMC2_CMD	J1.10 J1.167	MMC/SD/SDIO Command	
MMC2_DAT0	J1.30	MMC/SD/SDIO	

Pin name	Conn. Pin	Function	Notes
	J1.82 J1.163	Data bus	
MMC2_DAT1	J1.34 J1.84 J1.157	MMC/SD/SDIO Data bus	
MMC2_DAT2	J1.36 J1.86 J1.159	MMC/SD/SDIO Data bus	
MMC2_DAT3	J1.24 J1.88 J1.169	MMC/SD/SDIO Data bus	
MMC2_DAT4	J1.42 J1.74	MMC/SD/SDIO Data bus	
MMC2_DAT5	J1.44 J1.76	MMC/SD/SDIO Data bus	
MMC2_DAT6	J1.46 J1.78	MMC/SD/SDIO Data bus	
MMC2_DAT7	J1.48 J1.80	MMC/SD/SDIO Data bus	
MMC2_SDCD	J1.2 J1.142	MMC/SD Card Detect	
MMC2_SDWP	J1.33 J1.49	MMC/SD Write Protect	

7.6 USB ports

DIVA provides two USB 2.0 (Full Speed, up to 480 Mbps) ports with integrated PHY and support to the On-The-Go (OTG) specifications.

7.6.1 USB0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
USB0_CE	J1.53	USB0 Charger Enable output	Active high
USB0_DM	J1.59	USB0 Data Minus	

Pin name	Conn. Pin	Function	Notes
USB0_DP	J1.57	USB0 Data Plus	
USB0_DRVVBUS	J1.63	USB0 VBUS control output	Active high
USB0_ID	J1.55	USB0 OTG ID	
USB0_VBUS	J1.65	USB0 VBUS	

7.6.2 USB1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
USB1_CE	J1.73	USB1 Charger Enable output	Active high
USB1_DM	J1.79	USB1 Data Minus	
USB1_DP	J1.77	USB1 Data Plus	
USB1_DRVVBUS	J1.83	USB1 VBUS control output	Active high
USB1_ID	J1.75	USB1 OTG ID	
USB1_VBUS	J1.85	USB1 VBUS	

7.7 Touchscreen / ADC

The AM335x processor provides a touchscreen controller and analog-to-digital converter subsystem (TSC_ADC_SS), which is an 8-channel general-purpose analog-to-digital converter (ADC) with optional support for Touch screens. The TSC_ADC_SS can be configured for use in one of the following applications:

- 8 general-purpose ADC channels
- 4-wire TSC with 4 general-purpose ADC channels
- 5-wire TSC with 3 general-purpose ADC channels
- 8-wire TSC

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
AIN0	J1.87	Analog Input/Output	
AIN1	J1.89	Analog Input/Output	
AIN2	J1.91	Analog Input/Output	
AIN3	J1.95	Analog Input/Output	
AIN4	J1.97	Analog Input	
AIN5	J1.99	Analog Input	
AIN6	J1.103	Analog Input	
AIN7	J1.105	Analog Input	
AGND_TSC	J1.93 J1.101 J1.107	Analog TSC ground	

7.8 LCD controller

The AM335x integrates an LCD Controller which provides support for up to 24-bit data output (RGB, 8 bits-per-pixel) and up to WXGA (1366x768) resolution. It can drive Character, STN, TFT and OLED panels. The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
LCD_AC_BIAS_EN	J1.98	LCD AC bias enable chip select	
LCD_DATA0	J1.100	LCD Data bus	
LCD_DATA1	J1.102	LCD Data bus	
LCD_DATA2	J1.104	LCD Data bus	
LCD_DATA3	J1.106	LCD Data bus	
LCD_DATA4	J1.108	LCD Data bus	
LCD_DATA5	J1.110	LCD Data bus	
LCD_DATA6	J1.114	LCD Data bus	
LCD_DATA7	J1.116	LCD Data bus	

Pin name	Conn. Pin	Function	Notes
LCD_DATA8	J1.118	LCD Data bus	
LCD_DATA9	J1.120	LCD Data bus	
LCD_DATA10	J1.122	LCD Data bus	
LCD_DATA11	J1.124	LCD Data bus	
LCD_DATA12	J1.126	LCD Data bus	
LCD_DATA13	J1.128	LCD Data bus	
LCD_DATA14	J1.130	LCD Data bus	
LCD_DATA15	J1.134	LCD Data bus	
LCD_DATA16	J1.88	LCD Data bus	
LCD_DATA17	J1.86	LCD Data bus	
LCD_DATA18	J1.84	LCD Data bus	
LCD_DATA19	J1.82	LCD Data bus	
LCD_DATA20	J1.80	LCD Data bus	
LCD_DATA21	J1.78	LCD Data bus	
LCD_DATA22	J1.76	LCD Data bus	
LCD_DATA23	J1.74	LCD Data bus	
LCD_HSYNC	J1.96	LCD Horizontal Sync	
LCD_MEMORY_CLK	J1.14 J1.163	LCD Memory Clock	
LCD_PCLK	J1.90	LCD Pixel Clock	
LCD_VSYNC	J1.94	LCD Vertical Sync	

7.9 SPI buses

Up to two SPI channels are available on DIVA, to allow for a duplex, synchronous, serial communication between a CPU and SPI compliant external devices (Slaves and Masters). Each port has a maximum supported frequency of 48 MHz and provides 2 chip selects. Communication parameters (frequency, polarity, phase) are programmable.

7.9.1 SPI channel 0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SPI0_CS0	J1.49	SPI0 Chip Select #0	
SPI0_CS1	J1.51	SPI0 Chip Select #1	
SPI0_D0	J1.45	SPI0 data	
SPI0_D1	J1.47	SPI0 data	
SPI0_SCLK	J1.43	SPI0 clock	

7.9.2 SPI channel 1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SPI1_CS0	J1.27 J1.29 J1.39 J1.144	SPI1 Chip Select #0	
SPI1_CS1	J1.25 J1.37 J1.69 J1.109	SPI1 Chip Select #1	
SPI1_D0	J1.31 J1.140	SPI1 data	
SPI1_D1	J1.29 J1.142	SPI1 data	
SPI1_SCLK	J1.109 J1.150 J1.169	SPI1 clock	

7.10 I2C buses

Up to three I2C channels are available on DIVA to provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 8-bit data to/from the device through the I2C module. The I2C ports support standard (up to 100 Kbps) and fast (up to 400 Kbps) modes; the controller supports the

multi-master mode that allows more than one device capable of controlling the bus to be connected to it.

7.10.1 I2C channel 0

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
I2C0_SCL	J1.3	I2C0 clock	Internally connected to a 10K pull-up resistor
I2C0_SDA	J1.5	I2C0 data	Internally connected to a 10K pull-up resistor

7.10.2 I2C channel 1

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
I2C1_SCL	J1.29 J1.33 J1.49	I2C1 clock	No pull-up/pull-down
I2C1_SDA	J1.31 J1.35 J1.47	I2C1 data	No pull-up/pull-down

7.10.3 I2C channel 2

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
I2C2_SCL	J1.25 J1.37 J1.45	I2C2 clock	No pull-up/pull-down
I2C2_SDA	J1.27 J1.39 J1.43	I2C2 data	No pull-up/pull-down

7.11 EEPROM

One EEPROM is available to provide additional non-volatile storage area for user-specific usage. It is connected to the I2C-0 bus. A1 and A0 bits of address can be configured at carrier board level. Device address is 10100[A1][A0]b.

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EEPROM_A0	J1.17	I²C Address pins	A1 and A0 bits of address can be configured at carrier board level
EEPROM_A1	J1.15		
EEPROM_WP	J1.13	Write protect	Active high

7.12 Local Bus (GPMC)

The general-purpose memory controller (GPMC) is an unified memory controller dedicated to interfacing external memory devices:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (only available in non-multiplexed mode) burst NOR flash devices
- NAND Flash (with BCH and Hamming Error Code Detection)
- Pseudo-SRAM devices

GPMC offers support for the following memory types:

- External asynchronous or synchronous 8-bit width memory or device (non burst device)
- External asynchronous or synchronous 16-bit width memory or device
- External 16-bit non-multiplexed NOR Flash device
- External 16-bit address and data multiplexed NOR Flash device

- External 8-bit and 16-bit NAND flash device
- External 16-bit pSRAM device

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
GPMC_A0	J1.28 J1.100	GPMC Address bit 0	
GPMC_A1	J1.30 J1.94 J1.102	GPMC Address bit 1	
GPMC_A2	J1.34 J1.96 J1.104	GPMC Address bit 2	
GPMC_A3	J1.10 J1.36 J1.106	GPMC Address bit 3	
GPMC_A4	J1.38 J1.108	GPMC Address bit 4	
GPMC_A5	J1.40 J1.110	GPMC Address bit 5	
GPMC_A6	J1.42 J1.114	GPMC Address bit 6	
GPMC_A7	J1.44 J1.116	GPMC Address bit 7	
GPMC_A8	J1.46 J1.94	GPMC Address bit 8	
GPMC_A9	J1.48 J1.96	GPMC Address bit 9	
GPMC_A10	J1.50 J1.90	GPMC Address bit 10	
GPMC_A11	J1.54 J1.98	GPMC Address bit 11	
GPMC_A12	J1.118	GPMC Address bit 12	
GPMC_A13	J1.120	GPMC Address bit 13	
GPMC_A14	J1.122	GPMC Address bit	

Pin name	Conn. Pin	Function	Notes
		14	
GPMC_A15	J1.124	GPMC Address bit 15	
GPMC_A16	J1.28 J1.126	GPMC Address bit 16	
GPMC_A17	J1.30 J1.128	GPMC Address bit 17	
GPMC_A18	J1.34 J1.130	GPMC Address bit 18	
GPMC_A19	J1.36 J1.134	GPMC Address bit 19	
GPMC_A20	J1.38 J1.111	GPMC Address bit 20	
GPMC_A21	J1.40 J1.113	GPMC Address bit 21	
GPMC_A22	J1.42 J1.115	GPMC Address bit 22	
GPMC_A23	J1.44 J1.117	GPMC Address bit 23	
GPMC_A24	J1.46 J1.123	GPMC Address bit 24	
GPMC_A25	J1.48 J1.119	GPMC Address bit 25	
GPMC_A26	J1.50	GPMC Address bit 26	
GPMC_A27	J1.54	GPMC Address bit 27	
GPMC_AD0	J1.56	GPMC Address and Data bit 0	
GPMC_AD1	J1.58	GPMC Address and Data bit 1	
GPMC_AD2	J1.60	GPMC Address and Data bit 2	
GPMC_AD3	J1.62	GPMC Address and Data bit 3	
GPMC_AD4	J1.64	GPMC Address and Data bit 4	

Pin name	Conn. Pin	Function	Notes
GPMC_AD5	J1.66	GPMC Address and Data bit 5	
GPMC_AD6	J1.68	GPMC Address and Data bit 6	
GPMC_AD7	J1.70	GPMC Address and Data bit 7	
GPMC_AD8	J1.74	GPMC Address and Data bit 8	
GPMC_AD9	J1.76	GPMC Address and Data bit 9	
GPMC_AD10	J1.78	GPMC Address and Data bit 10	
GPMC_AD11	J1.80	GPMC Address and Data bit 11	
GPMC_AD12	J1.82	GPMC Address and Data bit 12	
GPMC_AD13	J1.84	GPMC Address and Data bit 13	
GPMC_AD14	J1.86	GPMC Address and Data bit 14	
GPMC_AD15	J1.88	GPMC Address and Data bit 15	
GPMC_ADVn_ALE	J1.20	GPMC Address Valid / Address Latch Enable	
GPMC_BE0n_CLE	J1.22	GPMC Byte Enable 0 / Command Latch Enable	
GPMC_BE1n	J1.8 J1.24	GPMC Byte Enable 1	
GPMC_CLK	J1.6 J1.14	GPMC Clock	
GPMC_CSN0	J1.4	GPMC Chip Select 0	
GPMC_CSN1	J1.6	GPMC Chip Select 1	
GPMC_CSN2	J1.8	GPMC Chip Select	

Pin name	Conn. Pin	Function	Notes
		2	
GPMC_CSN3	J1.10	GPMC Chip Select 3	
GPMC_CSN4	J1.26	GPMC Chip Select 4	
GPMC_CSN5	J1.2	GPMC Chip Select 5	
GPMC_CSN6	J1.24	GPMC Chip Select 6	
GPMC_DIR	J1.24	GPMC Data Direction	
GPMC_OEN_REN	J1.18	GPMC Output / Read Enable	
GPMC_WAIT0	J1.26	GPMC Wait 0	
GPMC_WAIT1	J1.14	GPMC Wait 1	
GPMC_WEN	J1.16	GPMC Write Enable	
GPMC_WPN	J1.2	GPMC Write Protect	

7.13 GPIOs

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs, for connections to external devices. In addition, the GPIO peripheral can produce CPU interrupts in different interrupt generation modes. The device contains four 3.3 V GPIO modules, for up to 118 pins (GP0[0:31], GP1[0:31], GP2[0:31], and GP3[0:21]). Each channel must be properly configured, since GPIO signals are multiplexed with other interfaces signals.

7.14 Timers

The general-purpose timer is an upward counter. It supports 3 functional modes:

- Timer mode
- Capture mode

- Compare mode

By default, after core reset, the capture and compare modes are disabled. Four timers (DMTIMER4 - DMTIMER7) are Pinned Out.

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
TIMER4	J1.5 J1.20 J1.69	Timer trigger event / PWM out	
TIMER5	J1.22 J1.37 J1.111 J1.165	Timer trigger event / PWM out	
TIMER6	J1.16 J1.18 J1.39 J1.113 J1.167	Timer trigger event / PWM out	
TIMER7	J1.3 J1.31 J1.71	Timer trigger event / PWM out	

7.15 Pulse width modulation subsystem (PWMSS)

The Pulse Width Modulation Subsystem (PWMSS) includes a single instance of the Enhanced High Resolution Pulse Width Modulator (eHRPWM), Enhanced Capture (eCAP), and Enhanced Quadrature Encoded Pulse (eQEP) modules. This includes three instantiations of the PWMSS.

7.15.1 eHRPWM 0

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EHRPWM0A	J1.43 J1.150	eHRPWM0 A output.	

Connector Pin	Pin name	Function	Notes
EHRPWM0B	J1.45 J1.140	eHRPWM0 B output.	
EHRPWM0_SYNCI	J1.49 J1.144	Sync input to eHRPWM0 module from an external pin	
EHRPWM0_SYNCO	J1.106	Sync Output from eHRPWM0 module to an external pin	
EHRPWM0_TRIPZONE_INPUT	J1.47 J1.142	eHRPWM0 trip zone input	

7.15.2 eHRPWM 1

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EHRPWM1A	J1.34 J1.122	eHRPWM1 A output.	
EHRPWM1B	J1.36 J1.124	eHRPWM1 B output.	
EHRPWM1_TRIPZONE_INPUT	J1.28 J1.118	eHRPWM1 trip zone input	

7.15.3 eHRPWM 2

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EHRPWM2A	J1.74 J1.100	eHRPWM2 A output.	
EHRPWM2B	J1.76 J1.102	eHRPWM2 B output.	
EHRPWM2_TRIPZONE_INPUT	J1.78 J1.104	eHRPWM2 trip zone input	

7.15.4 eCAP

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
ECAP0_IN_PWM0_OUT	J1.109	Enhanced Capture 0 input or Auxiliary PWM0 output	
ECAP1_IN_PWM1_OUT	J1.3 J1.25 J1.51	Enhanced Capture 1 input or Auxiliary PWM1 output	
ECAP2_IN_PWM2_OUT	J1.5 J1.27 J1.144	Enhanced Capture 2 input or Auxiliary PWM2 output	

7.15.5 eQEP 0

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EQEP0A_IN	J1.146	eQEP0A quadrature input	
EQEP0B_IN	J1.136	eQEP0B quadrature input	
EQEP0_INDEX	J1.138	eQEP0 index	
EQEP0_STROBE	J1.148	eQEP0 strobe	

7.15.6 eQEP 1

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EQEP1A_IN	J1.38 J1.126	eQEP1A quadrature input	
EQEP1B_IN	J1.40 J1.128	eQEP1B quadrature input	
EQEP1_INDEX	J1.42 J1.130	eQEP1 index	
EQEP1_STROBE	J1.44 J1.134	eQEP1 strobe	

7.15.7 eQEP 2

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
EQEP2A_IN	J1.82 J1.108	eQEP2A quadrature input	
EQEP2B_IN	J1.84 J1.110	eQEP2B quadrature input	
EQEP2_INDEX	J1.86 J1.114	eQEP2 index	
EQEP2_STROBE	J1.88 J1.116	eQEP2 strobe	

8 Operational characteristics

8.1 Maximum ratings

This section will be completed in a future version of this manual.

Parameter	Min	Typ	Max	Unit
Main power supply voltage	3.6	5.0 V	5.5V	V

8.2 Recommended ratings

This section will be completed in a future version of this manual.

Parameter	Min	Typ	Max	Unit
Main power supply voltage	3.6	5.0 V	5.5V	V

8.3 Power consumption

The use case here presented should cover a worst-case scenario. So, actual customer application might require less power than values reported here. Generally speaking, application specific requirements have to be taken into consideration in order to size power supply unit and to implement thermal management properly. Please note that DIVA platform is so flexible that it is virtually impossible to test for all possible configurations and applications on the market.

8.3.1 Set 1

Measurements have been performed on the following platform:

- DIVA SOM
- Carrier board: DIVAEVB-Lite on DACU
- System software: DELK preliminary version

The test bench runs the following software:

- burnCortexA8 in continuous loop
- MEMTest: memtester 6M 1 with logddrXXX.txt
- USB:
  - mount
  - head -c 10485760 /dev/urandom
  - md5sum
  - copy
  - md5sum
  - diff md5
  - remount
  - md5sum
  - diff md5
  - umount
- NAND: mtd13 mtd14
  - flash_erase
  - nandbadcount /dev/mtd
- slide_show with fbi

8.3.1.1 Results

With this test bench, the **CPU load is always 100%** and many components are active at the same time, so this is a non-realistic worst case scenario. The average measured power consumption is **2,6 W**.

8.4 Heat Dissipation

This section will be completed in a future version of this manual.

9 Application notes

Please refer to the following documents available on **DAVE Embedded Systems** Developers Wiki:

Document	Location
Integration Guide	http://wiki.dave.eu/index.php/Integration_guide_%28Diva%29
Carrier board design guidelines	http://wiki.dave.eu/index.php/Carrier_board_design_guidelines_%28SOM%29