

DLPC410 DMD Digital Controller

1 Features

- Operates the Following DLP® Chips:
 - DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs
 - DLPA200 DMD Micromirror Driver
 - DLPR410 Configuration PROM
- Enables High Speed DMD Pattern Rates
 - 1-Bit Binary Pattern Rates up to 32 kHz
 - 8-Bit Monochrome Pattern Rates up to 4 kHz
- 400 MHz Input Data Clock Rates
- 64-Bit 2xLVDS Data Bus Interfaces In/Out
- Supports Random Row and LOAD4 DMD Addressing
- Compatible With a Variety of User Defined Processors or FPGAs

2 Applications

- Industrial:
 - Direct Imaging Lithography
 - 3D Printing (SLA and SLS)
 - 3D Machine Vision
 - 3D Scanners for Robotics & Inspection
 - Dynamic Grayscale Laser Marking and Coding
 - Industrial Printing
 - High Speed Projection and Advanced Imaging
 - Ablation and Repair Systems
 - Microscopes

3 Description

The DLPC410 is a digital controller that supports five DMD options: DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV. It is the convenient, high-speed data and control interface between the application electronics and the DMD. The DLPC410 provides DMD Mirror Clocking Pulses (Resets) and timing information to the DLPA200 DMD Micromirror Driver. The device is configured with firmware stored in the DLPR410 PROM.

This family of chipsets enables pixel data rates up to 48 Gigabits per second (Gbps) with the option for single, dual, quad, and global Resets. In addition, random row addressing and LOAD4 capabilities are offered. Often the family of chips is used when designing UV and NIR systems such as direct imaging lithography, 3D printing, and laser marking systems that need fast throughput and pixel accurate control.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-------------|---------------------|
| DLPC410 | FCBGA (676) | 27.00 mm x 27.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application

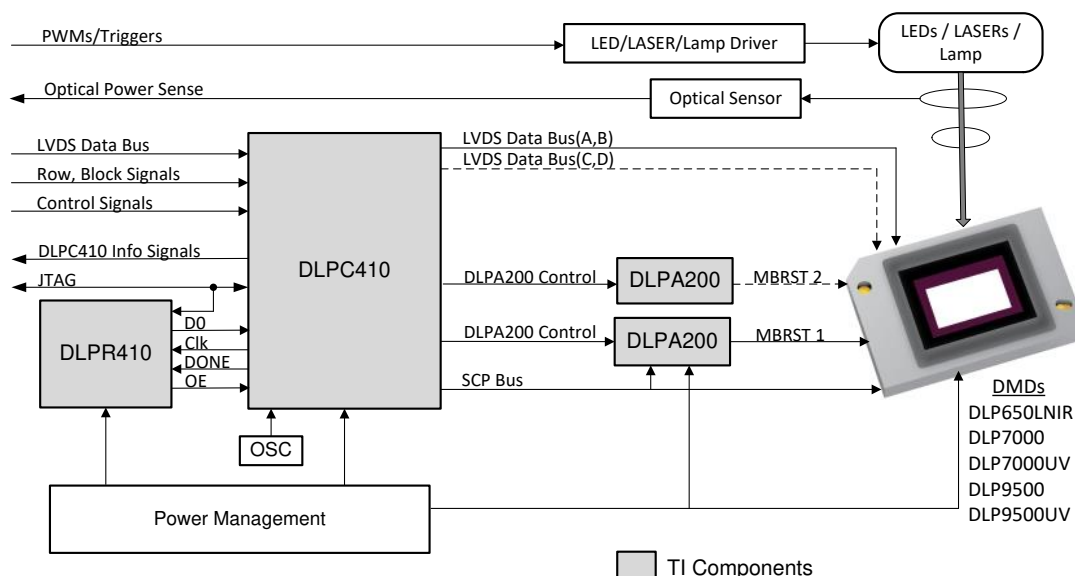


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| 8.4 | Device Functional Modes..... | 49 | 12.6 | Glossary | 77 |
| 8.5 | Programming..... | 58 | 13 | Mechanical, Packaging, and Orderable Information | 77 |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (February 2019) to Revision G | Page |
|--|-------------|
| • Removed extraneous setup/hold diagram (Figure 3) for COMP_DATA and NS_FLIP | 22 |
| • Fixed "BLKAD(10:0)" to "BLKAD(3:0)" on block diagrams | 24 |
| • Changed Figure 8 Row Cycle Diagram to match Table 9 and Table 10 pixel mapping | 37 |
| • Changed DDC_VERSION(3:0) to DDC_VERSION(2:0) to reflect hardware pinout | 49 |
| • Corrected initialization sequence to reflect both DLPA200s configured in two steps | 61 |
| • Deleted "DMD Device OK" debug section as debug signals are not assigned for output on ECP pins (reserved). | 62 |

| Changes from Revision E (January 2019) to Revision F | Page |
|---|-------------|
| • Modified functions for TP4-TP31 | 15 |
| • Corrected DLP650LNIR Bus A Pixel Mapping | 38 |
| • Corrected DLP650LNIR Bus A Pixel Mapping | 39 |
| • Corrected DLP650LNIR Bus B Pixel Mapping | 40 |
| • Corrected DLP650LNIR Bus B Pixel Mapping | 41 |
| • Removed ECP2M calibration feedback pins | 62 |
| • Removed ECP2M DLPA200 Init Status pin | 62 |
| • Removed ECP2M DMD Init Status pin | 62 |
| • Removed the ECP2_M TP20 referring to AA18 instead | 63 |

| Changes from Revision D (December 2018) to Revision E | Page |
|---|-------------|
| • Changed $\overline{\text{ARST}}$ description that was incorrectly described in DLPS024 Revision D. | 48 |

| Changes from Revision C (December 2015) to Revision D | Page |
|---|-------------|
| • Added new DLP650LNIR to supported DMDs (multiple) | 1 |
| • Changed input data clock rate to 400 MHz only | 1 |
| • Updated Applications list for latest markets | 1 |
| • Changed Simplified Diagram to include new DLP650LNIR | 1 |
| • Changed pin DDC_SPARE_0 to $\overline{\text{LOAD4}}$ | 16 |
| • Removed 200MHz - new revision tested at 400MHz only | 21 |
| • Re-organization of <i>Detailed Description</i> for flow, clarity, and readability | 23 |
| • Added DLP650LNIR functional block diagram | 24 |
| • Updated DLP7000 functional block diagram (no technical changes)..... | 25 |
| • Updated DLP9500 functional block diagram (no technical changes)..... | 26 |
| • Added new DLP650LNIR DMD Characteristics to Table 2 | 28 |
| • Added DLP650LNIR DMD to Row Addressing and Table 11 | 41 |
| • Re-worded the Block Operations section for clarity. | 45 |
| • Added new DLP650LNIR DMD Characteristics | 48 |
| • Added/edited LOAD4 sections, enabled by DLPR410A..... | 49 |
| • Removed reference to 200 MHz input data clock. | 49 |
| • Added the DLP650LNIR and its block load time to Table 16 | 51 |
| • Added Table 17 | 54 |
| • Combined Application Example Diagrams to encompass all DLPC410 supported DMDs | 60 |
| • Added DLP650LNIR to Detailed Design procedure section | 61 |
| • Added Figure 24 - DLP650LNIR window transmittance | 61 |
| • Changed "Generate Data" to "Present Data to DLPC410" | 63 |
| • Changed "DLPC410 DMD data signals" to "LVDS data bus differential pairs"..... | 65 |
| • Removed reference to TI part number 2510440-001. | 76 |
| • Removed Discovery Chipset data sheet, added DLP650LNIR data sheet, corrected other device names | 77 |

| Changes from Revision B (June 2013) to Revision C | Page |
|---|-------------|
| • Added <i>ESD Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Removed references to Discovery 4100 and deleted DLPR4101 throughout document..... | 1 |
| • Added DLP7000UV and DLP9500UV to <i>Features and Description</i> | 1 |
| • Added note - Xilinx System Monitor analog supply & ground - "must be connected to ground" (AVDD_0 & AVSS_0)..... | 7 |
| • Changed "DAD A" descriptions to "DLPA200 number 1" and "DAD B" descriptions to "DLPA200 number 2" | 7 |
| • Reversed DDC_Bnn_VR pairs pullups / pulldowns (for nn =12, 15, and 16)) | 8 |
| • Changed Pin # C22 name from DDC_B11_VRP (duplicate) to DDC_B15_VRP | 8 |
| • Added "Not used" to description for DMD_B_RESET and $\overline{\text{DMD_B_SCPEN}}$ | 14 |
| • Added TP14 and TP17 note - Xilinx Temperature Diode | 14 |
| • Added "in Reference Design" to ECP2 Mictor pin notes..... | 14 |
| • Changed ECP2 pin description from "Not Defined" to "Not Used" | 14 |
| • Added ECP2_M_TP[3:29] descriptions and active state..... | 15 |
| • Deleted duplicate pin numbers M13 and M14 | 16 |
| • Changed Description from "DMD Power" to "DMD Power Good indicator" | 16 |
| • Changed duplicate pin name from RSVD_0 to RSVD_1 | 17 |
| • Updated pin description for SCPDI and SCPDO | 17 |

| | |
|---|----|
| • Changed STEPVCC to connect to ground, active "Hi" to "-", and clock to "-" | 17 |
| • Changed Description from "JTAG Data Clock" to "JTAG Data" | 17 |
| • Changed pin names for VCCO_n_n pins to list each pin separately | 18 |
| • Added note about Xilinx System Monitor differential pins (VN_0 & VP_0) and reference voltage (VREFN_0 & VREFP_0)..... | 18 |
| • Changed Description from "DMD Reset Watchdog" to "DMD Mirror Clocking Pulse Watchdog" | 19 |
| • Deleted duplicate pin numbers in "UNUSED" pin list..... | 19 |
| • Updated the functional block diagrams | 25 |
| • Moved DLP7000 / DLP7000UV and DLP9500 / DLP9500UV Example Block Diagrams from Functional Block Diagram section to Typical Application Section | 26 |
| • Deleted the "Step DMD SRAM Memory Voltage" and "Load 4" Enhanced Functionality (with DLPR4101 PROM only)" sections | 48 |
| • Updated the embedded example block diagrams | 60 |
| • Added DLP7000UV and DLP9500UV well suited for direct imaging lithography, 3D printing, and UV applications | 61 |
| • Added Debugging Guidelines section | 61 |
| • Changed maximum differential trace length from 100 to 150 matching Table 13..... | 65 |
| • Added DLP7000UV and DLP9500UV Related Documentation | 77 |

Changes from Revision A (September 2012) to Revision B
Page

| | |
|---|----|
| • Changed Feature From: 1-Bit Binary Pattern Rates up to 32-kHz To: 1-Bit Binary Pattern Rates up to 32-kHz (up to 48-kHz when used with DLPR4101)..... | 1 |
| • Added Section "Load 4" Enhanced Functionality (with DLPR4101 PROM only)..... | 49 |
| • Added DLPR4101 to DLPR410 | 77 |

Changes from Original (August 2012) to Revision A
Page

| | |
|---|---|
| • Changed the device From: Product Preview to Production..... | 1 |
|---|---|

5 Description (continued)

In DLP-based electronics solutions, image data is 100% digital from the DLPC410 input port to the projected image. The image stays in digital form and is never converted into an analog signal. The DLPC410 processes the digital input image and converts the data into a format needed by the image on the DMD. The DMD then steers the light using binary pulse-width modulation (PWM) for each pixel mirror.

The DLPC410 is the DMD digital controller that controls the DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs (see [Functional Block Diagram](#), [Functional Block Diagram](#), and [Functional Block Diagram](#)). The DLPC410 provides developers easy access to the DMD as well as high speed, independent micromirror control. See the list of required chipset components for each DMD solution in [Device Configurations](#) table:

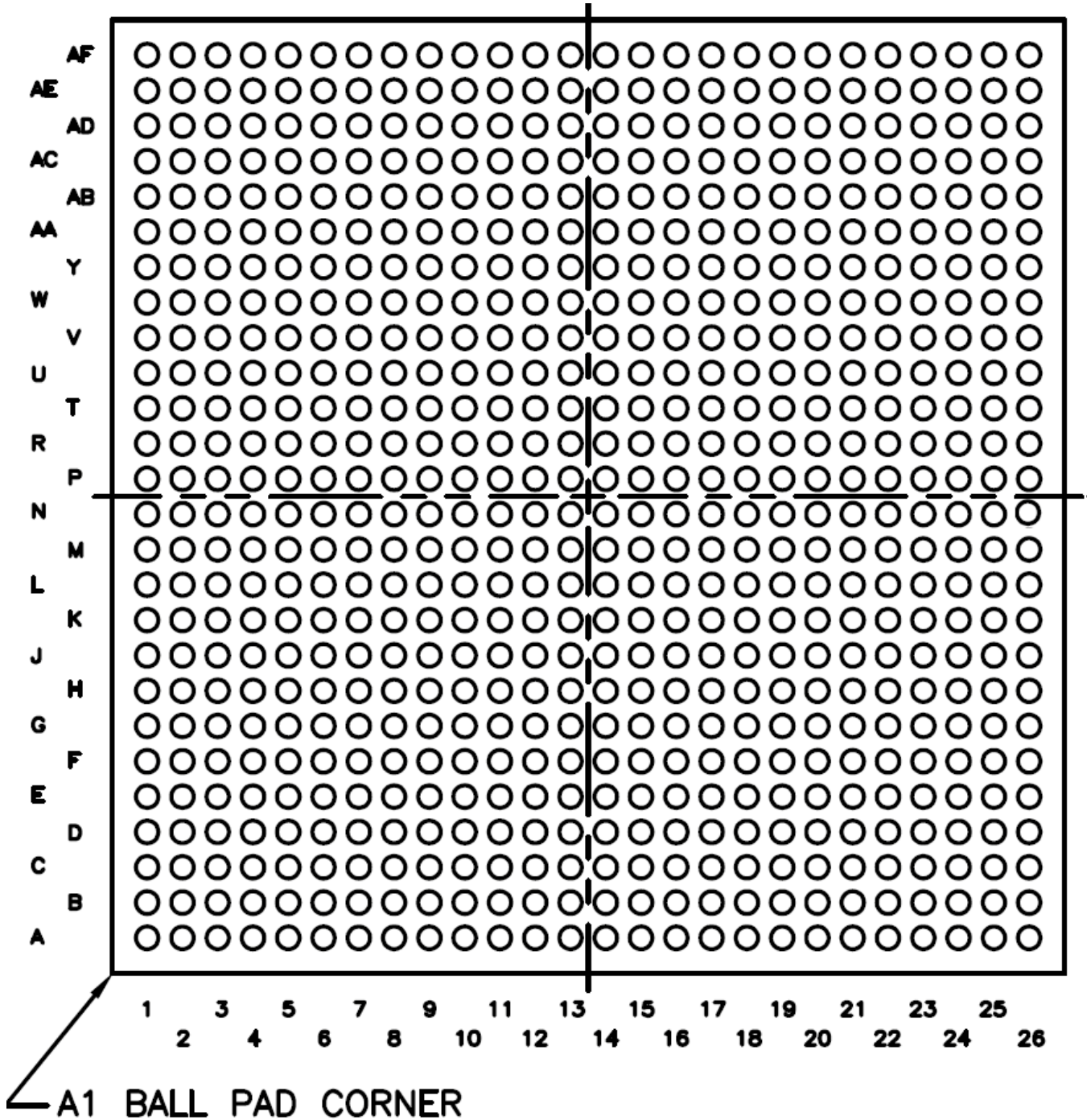
Table 1. DLPC410 Device Configurations

| DMD | DMD MICROMIRROR DRIVER | DMD DIGITAL CONTROLLER |
|---|------------------------|--|
| DLP9500 DLP 0.95 1080p 2xLVDS Type A DMD | 2 ea. DLPA200 | DLPC410 (+ DLPR410 Configuration PROM) |
| DLP9500UV DLP 0.95 UV 1080p 2xLVDS Type A DMD | 2 ea. DLPA200 | |
| DLP7000 DLP 0.7 XGA 2xLVDS Type A DMD | 1 ea. DLPA200 | |
| DLP7000UV DLP 0.7 UV XGA 2xLVDS Type A DMD | 1 ea. DLPA200 | |
| DLP650LNIR 0.65 NIR WXGA S450 DMD | 1 ea. DLPA200 | |

Reliable function and operation of the DLPC410 requires that it be used in conjunction with the other components of the chipset in [DLPC410 Device Configurations](#) table. For more information on the chipset components, see the data sheets in [Related Documentation](#).

6 Pin Configuration and Functions

ZYR Package
676-Pin FCBGA
Bottom View



Pin Functions

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|---------------|------|------|----------------------|--|----------------------|--------------------|--------------|--|
| NAME | NO. | | | | | | | |
| APPS_CNTL_DPN | F7 | - | - | This pair connected with 100 Ω resistor between pair. | - | - | | Not Used |
| APPS_CNTL_DPP | E7 | - | - | | - | - | | Not Used |
| ARST | AC13 | I | LVC MOS25_S_ 12_I | | Lo | - | | DLPC410 Reset |
| AVDD_0 | M14 | - | - | Not used - connect to Ground (no name in Reference Design) | - | - | | Xilinx System Monitor analog supply - (not used - must be connected to ground) |
| AVSS_0 | M13 | - | - | Not used - connect to Ground (no name in Reference Design) | - | - | | Xilinx System Monitor analog ground - (not used - must be connected to ground) |
| BLKAD_0 | E12 | I | LVC MOS25_S_ 12_I | | Hi = 1 | DDC_DCLK_[A,B,C,D] | | Block Address bit 0 |
| BLKAD_1 | D13 | I | LVC MOS25_S_ 12_I | | Hi = 1 | DDC_DCLK_[A,B,C,D] | | Block Address bit 1 |
| BLKAD_2 | E13 | I | LVC MOS25_S_ 12_I | | Hi = 1 | DDC_DCLK_[A,B,C,D] | | Block Address bit 2 |
| BLKAD_3 | F13 | I | LVC MOS25_S_ 12_I | | Hi = 1 | DDC_DCLK_[A,B,C,D] | | Block Address bit 3 |
| BLKMD_0 | H13 | I | LVC MOS25_S_ 12_I | | Hi = 1 | DDC_DCLK_[A,B,C,D] | | Block Mode Bit 0 |
| BLKMD_1 | H14 | I | LVC MOS25_S_ 12_I | | Hi = 1 | DDC_DCLK_[A,B,C,D] | | Block Mode Bit 1 |
| CLKIN_R | AD13 | I | LVC MOS25_S_ 12_I | | - | Reference Clock | | Reference Clock |
| COMP_DATA | G19 | I | LVC MOS25_S_ 12_I | | Hi | DDC_DCLK_[A,B,C,D] | | Compliment Data (0 <-> 1) |
| CS_B_0 | N18 | - | - | 1 kΩ pulldown to ground | Lo | - | | Xilinx Config |
| D_OUT_BUSY_0 | W11 | - | NC | Do not connect | - | - | | Not Used |
| DAD_A_ADDR0 | E1 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 number 1 Address 0 pin | Hi = 1 | - | | DLPA200 Number 1 Reset Block bit 0 |
| DAD_A_ADDR1 | E2 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 Address 1 pin | Hi = 1 | - | | DLPA200 Number 1 Reset Block bit 1 |
| DAD_A_ADDR2 | E3 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 Address 2 pin | Hi = 1 | - | | DLPA200 Number 1 Reset Block bit 2 |
| DAD_A_ADDR3 | F3 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 Address 3 pin | Hi = 1 | - | | DLPA200 Number 1 Reset Block bit 3 |
| DAD_A_MODE0 | C1 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 Mode 0 pin | Hi = 1 | - | | DLPA200 Number 1 Mode bit 0 |
| DAD_A_MODE1 | D1 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 Mode 1 pin | Hi = 1 | - | | DLPA200 Number 1 Mode bit 1 |
| DAD_A_SCPEN | AE3 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 SCPEN pin | Lo | - | | DLPA200 Number 1 SCP Communication Enable |
| DAD_A_SEL0 | AB12 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 SEL 0 pin | Hi = 1 | - | | DLPA200 Number 1 Address bit 0 |
| DAD_A_SEL1 | AC12 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 SEL 1 pin | Hi = 1 | - | | DLPA200 Number 1 Address bit 1 |
| DAD_A_STROBE | AF3 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 1 STROBE pin | Hi | - | | DLPA200 Number 1 Transition Strobe |
| DAD_B_ADDR0 | E26 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 Address 1 pin | Hi = 1 | - | | DLPA200 Number 2 Reset Block bit 0 |
| DAD_B_ADDR1 | E25 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 Address 2 pin | Hi = 1 | - | | DLPA200 Number 2 Reset Block bit 1 |
| DAD_B_ADDR2 | F25 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 Address 3 pin | Hi = 1 | - | | DLPA200 Number 2 Reset Block bit 2 |
| DAD_B_ADDR3 | F24 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 Address 0 pin | Hi = 1 | - | | DLPA200 Number 2 Reset Block bit 3 |
| DAD_B_MODE0 | D26 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 Mode 0 pin | Hi = 1 | - | | DLPA200 Number 2 Mode bit 0 |
| DAD_B_MODE1 | D25 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 Mode 1 pin | Hi = 1 | - | | DLPA200 Number 2 Mode bit 1 |
| DAD_B_SCPEN | AB19 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 SCPEN pin | Lo | - | | DLPA200 Number 2 SCP Communication Enable |
| DAD_B_SEL0 | R22 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 SEL 0 pin | Hi = 1 | - | | DLPA200 Number 2 Address bit 0 |
| DAD_B_SEL1 | R23 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 SEL 1 pin | Hi = 1 | - | | DLPA200 Number 2 Address bit 1 |
| DAD_B_STROBE | AB20 | O | LVC MOS25_F_ 12_O | Connected to DLPA200 Number 2 STROBE pin | Hi | - | | DLPA200 Number 2 Transition Strobe |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|-------------------|------|------|------------------|---|-------------------|------------|-----------|---|
| NAME | NO. | | | | | | | |
| DAD_INIT | AF4 | O | LVC MOS25_F_12_O | Connected to DLPA200 Number 1 and Number 2 RESET pin | Hi | - | | DLPA200 Number 1 / Number 2 Init |
| DAD_OE | AF5 | O | LVC MOS25_F_12_O | Connected to DLPA200 Number 1 and Number 2 OE pin | Lo | - | | DLPA200 Number 1 / Number 2 Output Enable |
| DDC_B11_VRN | L23 | - | REFERENCE | 51.1 Ω pullup to 2.5 V | - | - | | Reference Voltage |
| DDC_B11_VRP | L22 | - | REFERENCE | 51.1 Ω pulldown to ground | - | - | | Reference Ground |
| DDC_B12_VRN | M5 | - | REFERENCE | 51.1 Ω pullup to 2.5 V | - | - | | Reference Voltage |
| DDC_B12_VRP | M6 | - | REFERENCE | 51.1 Ω pulldown to ground | - | - | | Reference Ground |
| DDC_B15_VRN | D23 | - | REFERENCE | 51.1 Ω pullup to 2.5 V | - | - | | Reference Voltage |
| DDC_B15_VRP | C22 | - | REFERENCE | 51.1 Ω pulldown to ground | - | - | | Reference Ground |
| DDC_B16_VRN | A4 | - | REFERENCE | 51.1 Ω pullup to 2.5 V | - | - | | Reference Voltage |
| DDC_B16_VRP | A5 | - | REFERENCE | 51.1 Ω pulldown to ground | - | - | | Reference Ground |
| DDC_DCLK_A_DPN | B21 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | - | | Bank A Input Clock (Neg) |
| DDC_DCLK_A_DPP | C21 | I | LVDS_25_I | | - | - | | Bank A Input Clock (Pos) |
| DDC_DCLK_B_DPN | A7 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | - | | Bank B Input Clock (Neg) |
| DDC_DCLK_B_DPP | B7 | I | LVDS_25_I | | - | - | | Bank B Input Clock (Pos) |
| DDC_DCLK_C_DPN | K20 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | - | | Bank C Input Clock (Neg) |
| DDC_DCLK_C_DPP | K21 | I | LVDS_25_I | | - | - | | Bank C Input Clock (Pos) |
| DDC_DCLK_D_DPN | L5 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | - | | Bank D Input Clock (Neg) |
| DDC_DCLK_D_DPP | K5 | I | LVDS_25_I | | - | - | | Bank D Input Clock (Pos) |
| DDC_DCLKOUT_A_DPN | N1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | - | | Bank A Output Clock (Neg) |
| DDC_DCLKOUT_A_DPP | M1 | O | LVDS_25_O | | - | - | | Bank A Output Clock (Pos) |
| DDC_DCLKOUT_B_DPN | Y5 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | - | | Bank B Output Clock (Neg) |
| DDC_DCLKOUT_B_DPP | Y6 | O | LVDS_25_O | | - | - | | Bank B Output Clock (Pos) |
| DDC_DCLKOUT_C_DPN | AA22 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | - | | Bank C Output Clock (Neg) |
| DDC_DCLKOUT_C_DPP | AB22 | O | LVDS_25_O | | - | - | | Bank C Output Clock (Pos) |
| DDC_DCLKOUT_D_DPN | M26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | - | | Bank D Output Clock (Neg) |
| DDC_DCLKOUT_D_DPP | M25 | O | LVDS_25_O | | - | - | | Bank D Output Clock (Pos) |
| DDC_DIN_A0_DPN | A15 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 0 Input (Neg) |
| DDC_DIN_A0_DPP | A14 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 0 Input (Pos) |
| DDC_DIN_A1_DPN | B14 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 1 Input (Neg) |
| DDC_DIN_A1_DPP | C14 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 1 Input (Pos) |
| DDC_DIN_A2_DPN | B16 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 2 Input (Neg) |
| DDC_DIN_A2_DPP | B15 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 2 Input (Pos) |
| DDC_DIN_A3_DPN | C16 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 3 Input (Neg) |
| DDC_DIN_A3_DPP | D16 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 3 Input (Pos) |
| DDC_DIN_A4_DPN | A17 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 4 Input (Neg) |
| DDC_DIN_A4_DPP | B17 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 4 Input (Pos) |
| DDC_DIN_A5_DPN | C17 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 5 Input (Neg) |
| DDC_DIN_A5_DPP | D18 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 5 Input (Pos) |
| DDC_DIN_A6_DPN | A19 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 6 Input (Neg) |
| DDC_DIN_A6_DPP | A18 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 6 Input (Pos) |
| DDC_DIN_A7_DPN | C18 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 7 Input (Neg) |
| DDC_DIN_A7_DPP | B19 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 7 Input (Pos) |
| DDC_DIN_A8_DPN | D19 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 8 Input (Neg) |
| DDC_DIN_A8_DPP | C19 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 8 Input (Pos) |
| DDC_DIN_A9_DPN | B20 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 9 Input (Neg) |
| DDC_DIN_A9_DPP | A20 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 9 Input (Pos) |
| DDC_DIN_A10_DPN | A22 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 10 Input (Neg) |
| DDC_DIN_A10_DPP | B22 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 10 Input (Pos) |
| DDC_DIN_A11_DPN | A24 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 11 Input (Neg) |
| DDC_DIN_A11_DPP | A23 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 11 Input (Pos) |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|-----------------|-----|------|-----------|---|-------------------|------------|-----------|---------------------------|
| NAME | NO. | | | | | | | |
| DDC_DIN_A12_DPN | C23 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 12 Input (Neg) |
| DDC_DIN_A12_DPP | B24 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 12 Input (Pos) |
| DDC_DIN_A13_DPN | C24 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 13 Input (Neg) |
| DDC_DIN_A13_DPP | D24 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 13 Input (Pos) |
| DDC_DIN_A14_DPN | A25 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 14 Input (Neg) |
| DDC_DIN_A14_DPP | B25 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 14 Input (Pos) |
| DDC_DIN_A15_DPN | C26 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | DDR | Data A bit 15 Input (Neg) |
| DDC_DIN_A15_DPP | B26 | I | LVDS_25_I | | - | DDC_DCLK_A | DDR | Data A bit 15 Input (Pos) |
| DDC_DIN_B0_DPN | A12 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 0 Input (Neg) |
| DDC_DIN_B0_DPP | A13 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 0 Input (Pos) |
| DDC_DIN_B1_DPN | B12 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 1 Input (Neg) |
| DDC_DIN_B1_DPP | C13 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 1 Input (Pos) |
| DDC_DIN_B2_DPN | D10 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 2 Input (Neg) |
| DDC_DIN_B2_DPP | D11 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 2 Input (Pos) |
| DDC_DIN_B3_DPN | C12 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 3 Input (Neg) |
| DDC_DIN_B3_DPP | C11 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 3 Input (Pos) |
| DDC_DIN_B4_DPN | A10 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 4 Input (Neg) |
| DDC_DIN_B4_DPP | B11 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 4 Input (Pos) |
| DDC_DIN_B5_DPN | D9 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 5 Input (Neg) |
| DDC_DIN_B5_DPP | C9 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 5 Input (Pos) |
| DDC_DIN_B6_DPN | B10 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 6 Input (Neg) |
| DDC_DIN_B6_DPP | B9 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 6 Input (Pos) |
| DDC_DIN_B7_DPN | A8 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 7 Input (Neg) |
| DDC_DIN_B7_DPP | A9 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 7 Input (Pos) |
| DDC_DIN_B8_DPN | D6 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 8 Input (Neg) |
| DDC_DIN_B8_DPP | D5 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 8 Input (Pos) |
| DDC_DIN_B9_DPN | C7 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 9 Input (Neg) |
| DDC_DIN_B9_DPP | C6 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 9 Input (Pos) |
| DDC_DIN_B10_DPN | B6 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 10 Input (Neg) |
| DDC_DIN_B10_DPP | B5 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 10 Input (Pos) |
| DDC_DIN_B11_DPN | D4 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 11 Input (Neg) |
| DDC_DIN_B11_DPP | D3 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 11 Input (Pos) |
| DDC_DIN_B12_DPN | B4 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 12 Input (Neg) |
| DDC_DIN_B12_DPP | C4 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 12 Input (Pos) |
| DDC_DIN_B13_DPN | C3 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 13 Input (Neg) |
| DDC_DIN_B13_DPP | C2 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 13 Input (Pos) |
| DDC_DIN_B14_DPN | A3 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 14 Input (Neg) |
| DDC_DIN_B14_DPP | A2 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 14 Input (Pos) |
| DDC_DIN_B15_DPN | B2 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | DDR | Data B bit 15 Input (Neg) |
| DDC_DIN_B15_DPP | B1 | I | LVDS_25_I | | - | DDC_DCLK_B | DDR | Data B bit 15 Input (Pos) |
| DDC_DIN_C0_DPN | E20 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 0 Input (Neg) |
| DDC_DIN_C0_DPP | E21 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 0 Input (Pos) |
| DDC_DIN_C1_DPN | F20 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 1 Input (Neg) |
| DDC_DIN_C1_DPP | G20 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 1 Input (Pos) |
| DDC_DIN_C2_DPN | H19 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 2 Input (Neg) |
| DDC_DIN_C2_DPP | J19 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 2 Input (Pos) |
| DDC_DIN_C3_DPN | E23 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 3 Input (Neg) |
| DDC_DIN_C3_DPP | E22 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 3 Input (Pos) |
| DDC_DIN_C4_DPN | F23 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 4 Input (Neg) |
| DDC_DIN_C4_DPP | F22 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 4 Input (Pos) |
| DDC_DIN_C5_DPN | G22 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 5 Input (Neg) |
| DDC_DIN_C5_DPP | G21 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 5 Input (Pos) |
| DDC_DIN_C6_DPN | J20 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 6 Input (Neg) |
| DDC_DIN_C6_DPP | J21 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 6 Input (Pos) |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|-----------------|-----|------|-----------|---|-------------------|---------------|-----------|---------------------------|
| NAME | NO. | | | | | | | |
| DDC_DIN_C7_DPN | H22 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 7 Input (Neg) |
| DDC_DIN_C7_DPP | H21 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 7 Input (Pos) |
| DDC_DIN_C8_DPN | J23 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 8 Input (Neg) |
| DDC_DIN_C8_DPP | H23 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 8 Input (Pos) |
| DDC_DIN_C9_DPN | K22 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 9 Input (Neg) |
| DDC_DIN_C9_DPP | K23 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 9 Input (Pos) |
| DDC_DIN_C10_DPN | M19 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 10 Input (Neg) |
| DDC_DIN_C10_DPP | M20 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 10 Input (Pos) |
| DDC_DIN_C11_DPN | M21 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 11 Input (Neg) |
| DDC_DIN_C11_DPP | M22 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 11 Input (Pos) |
| DDC_DIN_C12_DPN | N19 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 12 Input (Neg) |
| DDC_DIN_C12_DPP | P19 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 12 Input (Pos) |
| DDC_DIN_C13_DPN | N21 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 13 Input (Neg) |
| DDC_DIN_C13_DPP | N22 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 13 Input (Pos) |
| DDC_DIN_C14_DPN | P20 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 14 Input (Neg) |
| DDC_DIN_C14_DPP | P21 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 14 Input (Pos) |
| DDC_DIN_C15_DPN | N23 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | DDR | Data C bit 15 Input (Neg) |
| DDC_DIN_C15_DPP | P23 | I | LVDS_25_I | | - | DDC_DCLK_C | DDR | Data C bit 15 Input (Pos) |
| DDC_DIN_D0_DPN | T3 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 0 Input (Neg) |
| DDC_DIN_D0_DPP | R3 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 0 Input (Pos) |
| DDC_DIN_D1_DPN | R5 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 1 Input (Neg) |
| DDC_DIN_D1_DPP | R6 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 1 Input (Pos) |
| DDC_DIN_D2_DPN | R7 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 2 Input (Neg) |
| DDC_DIN_D2_DPP | P6 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 2 Input (Pos) |
| DDC_DIN_D3_DPN | N3 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 3 Input (Neg) |
| DDC_DIN_D3_DPP | P3 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 3 Input (Pos) |
| DDC_DIN_D4_DPN | P4 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 4 Input (Neg) |
| DDC_DIN_D4_DPP | P5 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 4 Input (Pos) |
| DDC_DIN_D5_DPN | N6 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 5 Input (Neg) |
| DDC_DIN_D5_DPP | N7 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 5 Input (Pos) |
| DDC_DIN_D6_DPN | N4 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 6 Input (Neg) |
| DDC_DIN_D6_DPP | M4 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 6 Input (Pos) |
| DDC_DIN_D7_DPN | M7 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 7 Input (Neg) |
| DDC_DIN_D7_DPP | L7 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 7 Input (Pos) |
| DDC_DIN_D8_DPN | K7 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 8 Input (Neg) |
| DDC_DIN_D8_DPP | K6 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 8 Input (Pos) |
| DDC_DIN_D9_DPN | J4 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 9 Input (Neg) |
| DDC_DIN_D9_DPP | J5 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 9 Input (Pos) |
| DDC_DIN_D10_DPN | H7 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 10 Input (Neg) |
| DDC_DIN_D10_DPP | J6 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 10 Input (Pos) |
| DDC_DIN_D11_DPN | G4 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 11 Input (Neg) |
| DDC_DIN_D11_DPP | H4 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 11 Input (Pos) |
| DDC_DIN_D12_DPN | G5 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 12 Input (Neg) |
| DDC_DIN_D12_DPP | H6 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 12 Input (Pos) |
| DDC_DIN_D13_DPN | G7 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 13 Input (Neg) |
| DDC_DIN_D13_DPP | G6 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 13 Input (Pos) |
| DDC_DIN_D14_DPN | F4 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 14 Input (Neg) |
| DDC_DIN_D14_DPP | F5 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 14 Input (Pos) |
| DDC_DIN_D15_DPN | E5 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | DDR | Data D bit 15 Input (Neg) |
| DDC_DIN_D15_DPP | E6 | I | LVDS_25_I | | - | DDC_DCLK_D | DDR | Data D bit 15 Input (Pos) |
| DDC_DOUT_A0_DPN | AE2 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 0 Output (Neg) |
| DDC_DOUT_A0_DPP | AF2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 0 Output (Pos) |
| DDC_DOUT_A1_DPN | AD1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 1 Output (Neg) |
| DDC_DOUT_A1_DPP | AE1 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 1 Output (Pos) |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|------------------|-----|------|-----------|---|----------------------|---------------|--------------|----------------------------|
| NAME | NO. | | | | | | | |
| DDC_DOUT_A2_DPN | AC1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 2 Output (Neg) |
| DDC_DOUT_A2_DPP | AC2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 2 Output (Pos) |
| DDC_DOUT_A3_DPN | AB1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 3 Output (Neg) |
| DDC_DOUT_A3_DPP | AB2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 3 Output (Pos) |
| DDC_DOUT_A4_DPN | Y2 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 4 Output (Neg) |
| DDC_DOUT_A4_DPP | AA2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 4 Output (Pos) |
| DDC_DOUT_A5_DPN | W1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 5 Output (Neg) |
| DDC_DOUT_A5_DPP | Y1 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 5 Output (Pos) |
| DDC_DOUT_A6_DPN | V1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 6 Output (Neg) |
| DDC_DOUT_A6_DPP | V2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 6 Output (Pos) |
| DDC_DOUT_A7_DPN | U1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 7 Output (Neg) |
| DDC_DOUT_A7_DPP | U2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 7 Output (Pos) |
| DDC_DOUT_A8_DPN | R2 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 8 Output (Neg) |
| DDC_DOUT_A8_DPP | T2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 8 Output (Pos) |
| DDC_DOUT_A9_DPN | N2 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 9 Output (Neg) |
| DDC_DOUT_A9_DPP | M2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 9 Output (Pos) |
| DDC_DOUT_A10_DPN | K1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 10 Output (Neg) |
| DDC_DOUT_A10_DPP | L2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 10 Output (Pos) |
| DDC_DOUT_A11_DPN | K2 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 11 Output (Neg) |
| DDC_DOUT_A11_DPP | K3 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 11 Output (Pos) |
| DDC_DOUT_A12_DPN | J3 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 12 Output (Neg) |
| DDC_DOUT_A12_DPP | H3 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 12 Output (Pos) |
| DDC_DOUT_A13_DPN | H2 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 13 Output (Neg) |
| DDC_DOUT_A13_DPP | J1 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 13 Output (Pos) |
| DDC_DOUT_A14_DPN | H1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 14 Output (Neg) |
| DDC_DOUT_A14_DPP | G1 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 14 Output (Pos) |
| DDC_DOUT_A15_DPN | G2 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Data A bit 15 Output (Neg) |
| DDC_DOUT_A15_DPP | F2 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Data A bit 15 Output (Pos) |
| DDC_DOUT_B0_DPN | AE5 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 0 Output (Neg) |
| DDC_DOUT_B0_DPP | AE6 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 0 Output (Pos) |
| DDC_DOUT_B1_DPN | AD3 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 1 Output (Neg) |
| DDC_DOUT_B1_DPP | AD4 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 1 Output (Pos) |
| DDC_DOUT_B2_DPN | AD5 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 2 Output (Neg) |
| DDC_DOUT_B2_DPP | AD6 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 2 Output (Pos) |
| DDC_DOUT_B3_DPN | AC3 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 3 Output (Neg) |
| DDC_DOUT_B3_DPP | AC4 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 3 Output (Pos) |
| DDC_DOUT_B4_DPN | AB5 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 4 Output (Neg) |
| DDC_DOUT_B4_DPP | AB6 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 4 Output (Pos) |
| DDC_DOUT_B5_DPN | AB7 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 5 Output (Neg) |
| DDC_DOUT_B5_DPP | AC6 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 5 Output (Pos) |
| DDC_DOUT_B6_DPN | AA5 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 6 Output (Neg) |
| DDC_DOUT_B6_DPP | AA4 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 6 Output (Pos) |
| DDC_DOUT_B7_DPN | AA7 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 7 Output (Neg) |
| DDC_DOUT_B7_DPP | Y7 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 7 Output (Pos) |
| DDC_DOUT_B8_DPN | Y3 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 8 Output (Neg) |
| DDC_DOUT_B8_DPP | W3 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 8 Output (Pos) |
| DDC_DOUT_B9_DPN | W4 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 9 Output (Neg) |
| DDC_DOUT_B9_DPP | V4 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 9 Output (Pos) |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|------------------|------|------|-----------|---|-------------------|---------------|-----------|----------------------------|
| NAME | NO. | | | | | | | |
| DDC_DOUT_B10_DPN | W6 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 10 Output (Neg) |
| DDC_DOUT_B10_DPP | W5 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 10 Output (Pos) |
| DDC_DOUT_B11_DPN | V7 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 11 Output (Neg) |
| DDC_DOUT_B11_DPP | V6 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 11 Output (Pos) |
| DDC_DOUT_B12_DPN | U4 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 12 Output (Neg) |
| DDC_DOUT_B12_DPP | V3 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 12 Output (Pos) |
| DDC_DOUT_B13_DPN | T4 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 13 Output (Neg) |
| DDC_DOUT_B13_DPP | T5 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 13 Output (Pos) |
| DDC_DOUT_B14_DPN | U6 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 14 Output (Neg) |
| DDC_DOUT_B14_DPP | U5 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 14 Output (Pos) |
| DDC_DOUT_B15_DPN | U7 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Data B bit 15 Output (Neg) |
| DDC_DOUT_B15_DPP | T7 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Data B bit 15 Output (Pos) |
| DDC_DOUT_C0_DPN | T22 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 0 Output (Neg) |
| DDC_DOUT_C0_DPP | T23 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 0 Output (Pos) |
| DDC_DOUT_C1_DPN | R20 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 1 Output (Neg) |
| DDC_DOUT_C1_DPP | R21 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 1 Output (Pos) |
| DDC_DOUT_C2_DPN | T19 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 2 Output (Neg) |
| DDC_DOUT_C2_DPP | T20 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 2 Output (Pos) |
| DDC_DOUT_C3_DPN | U21 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 3 Output (Neg) |
| DDC_DOUT_C3_DPP | U22 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 3 Output (Pos) |
| DDC_DOUT_C4_DPN | U20 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 4 Output (Neg) |
| DDC_DOUT_C4_DPP | U19 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 4 Output (Pos) |
| DDC_DOUT_C5_DPN | V23 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 5 Output (Neg) |
| DDC_DOUT_C5_DPP | V24 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 5 Output (Pos) |
| DDC_DOUT_C6_DPN | V22 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 6 Output (Neg) |
| DDC_DOUT_C6_DPP | V21 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 6 Output (Pos) |
| DDC_DOUT_C7_DPN | W19 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 7 Output (Neg) |
| DDC_DOUT_C7_DPP | V19 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 7 Output (Pos) |
| DDC_DOUT_C8_DPN | W23 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 8 Output (Neg) |
| DDC_DOUT_C8_DPP | W24 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 8 Output (Pos) |
| DDC_DOUT_C9_DPN | Y22 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 9 Output (Neg) |
| DDC_DOUT_C9_DPP | Y23 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 9 Output (Pos) |
| DDC_DOUT_C10_DPN | Y20 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 10 Output (Neg) |
| DDC_DOUT_C10_DPP | Y21 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 10 Output (Pos) |
| DDC_DOUT_C11_DPN | AA24 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 11 Output (Neg) |
| DDC_DOUT_C11_DPP | AA23 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 11 Output (Pos) |
| DDC_DOUT_C12_DPN | AA19 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 12 Output (Neg) |
| DDC_DOUT_C12_DPP | AA20 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 12 Output (Pos) |
| DDC_DOUT_C13_DPN | AC24 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 13 Output (Neg) |
| DDC_DOUT_C13_DPP | AB24 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 13 Output (Pos) |
| DDC_DOUT_C14_DPN | AC19 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 14 Output (Neg) |
| DDC_DOUT_C14_DPP | AD19 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 14 Output (Pos) |
| DDC_DOUT_C15_DPN | AC22 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Data C bit 15 Output (Neg) |
| DDC_DOUT_C15_DPP | AC23 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Data C bit 15 Output (Pos) |
| DDC_DOUT_D0_DPN | AB26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 0 Output (Neg) |
| DDC_DOUT_D0_DPP | AC26 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 0 Output (Pos) |
| DDC_DOUT_D1_DPN | AA25 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 1 Output (Neg) |
| DDC_DOUT_D1_DPP | AB25 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 1 Output (Pos) |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|------------------|------|------|------------------|---|----------------------|---------------|--------------|--------------------------------------|
| NAME | NO. | | | | | | | |
| DDC_DOUT_D2_DPN | Y26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 2 Output (Neg) |
| DDC_DOUT_D2_DPP | Y25 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 2 Output (Pos) |
| DDC_DOUT_D3_DPN | W26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 3 Output (Neg) |
| DDC_DOUT_D3_DPP | W25 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 3 Output (Pos) |
| DDC_DOUT_D4_DPN | U26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 4 Output (Neg) |
| DDC_DOUT_D4_DPP | V26 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 4 Output (Pos) |
| DDC_DOUT_D5_DPN | U25 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 5 Output (Neg) |
| DDC_DOUT_D5_DPP | U24 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 5 Output (Pos) |
| DDC_DOUT_D6_DPN | T25 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 6 Output (Neg) |
| DDC_DOUT_D6_DPP | T24 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 6 Output (Pos) |
| DDC_DOUT_D7_DPN | R26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 7 Output (Neg) |
| DDC_DOUT_D7_DPP | R25 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 7 Output (Pos) |
| DDC_DOUT_D8_DPN | P24 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 8 Output (Neg) |
| DDC_DOUT_D8_DPP | P25 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 8 Output (Pos) |
| DDC_DOUT_D9_DPN | N24 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 9 Output (Neg) |
| DDC_DOUT_D9_DPP | M24 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 9 Output (Pos) |
| DDC_DOUT_D10_DPN | L25 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 10 Output (Neg) |
| DDC_DOUT_D10_DPP | L24 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 10 Output (Pos) |
| DDC_DOUT_D11_DPN | K26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 11 Output (Neg) |
| DDC_DOUT_D11_DPP | K25 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 11 Output (Pos) |
| DDC_DOUT_D12_DPN | J26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 12 Output (Neg) |
| DDC_DOUT_D12_DPP | J25 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 12 Output (Pos) |
| DDC_DOUT_D13_DPN | J24 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 13 Output (Neg) |
| DDC_DOUT_D13_DPP | H24 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 13 Output (Pos) |
| DDC_DOUT_D14_DPN | H26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 14 Output (Neg) |
| DDC_DOUT_D14_DPP | G26 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 14 Output (Pos) |
| DDC_DOUT_D15_DPN | G25 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Data D bit 15 Output (Neg) |
| DDC_DOUT_D15_DPP | G24 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Data D bit 15 Output (Pos) |
| DDC_M0 | W18 | - | NC | 4.7 kΩ pullup to 2.5V | Hi | - | - | Xilinx Configuration |
| DDC_M1 | Y17 | - | NC | 4.7 kΩ pullup to 2.5V | Hi | - | - | Xilinx Configuration |
| DDC_M2 | V18 | - | NC | 4.7 kΩ pullup to 2.5V | Hi | - | - | Xilinx Configuration |
| DDC_SCTRL_AN | R1 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_A | DDR | Bank A Serial Control Data (Neg) |
| DDC_SCTRL_AP | P1 | O | LVDS_25_O | | - | DDC_DCLKOUT_A | DDR | Bank A Serial Control Data (Pos) |
| DDC_SCTRL_BN | AA3 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_B | DDR | Bank B Serial Control Data (Neg) |
| DDC_SCTRL_BP | AB4 | O | LVDS_25_O | | - | DDC_DCLKOUT_B | DDR | Bank B Serial Control Data (Pos) |
| DDC_SCTRL_CN | W20 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_C | DDR | Bank C Serial Control Data (Neg) |
| DDC_SCTRL_CP | W21 | O | LVDS_25_O | | - | DDC_DCLKOUT_C | DDR | Bank C Serial Control Data (Pos) |
| DDC_SCTRL_DN | N26 | O | LVDS_25 | Pair connected to DMD (LVDS terminated internally in DMD - 100 Ω) | - | DDC_DCLKOUT_D | DDR | Bank D Serial Control Data (Neg) |
| DDC_SCTRL_DP | P26 | O | LVDS_25_O | | - | DDC_DCLKOUT_D | DDR | Bank D Serial Control Data (Pos) |
| DDC_VERSION_0 | F18 | O | LVC MOS25_F_12_O | | Hi = 1 | - | | DLPC410 Firmware Rev Number bit 0 |
| DDC_VERSION_1 | G17 | O | LVC MOS25_F_12_O | | Hi = 1 | - | | DLPC410 Firmware Rev Number bit 1 |
| DDC_VERSION_2 | H18 | O | LVC MOS25_F_12_O | | Hi = 1 | - | | DLPC410 Firmware Rev Number bit 2 |
| DDC_SPARE_1 | AC21 | - | LVC MOS25_F_12_O | Do not connect | - | - | | Not Used |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|---------------|------|------|------------------|--|-------------------|------------|-----------|--|
| NAME | NO. | | | | | | | |
| DMD_A_RESET | AD14 | O | LVC MOS25_F_12_O | Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (signal name DMD_A_RESET_FILT after resistor - connects to DMD signal DMDRST) | Lo | - | | DMD Circuitry Reset (not data reset) |
| DMD_A_SCPEN | AB14 | O | LVC MOS25_F_12_O | Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (called DMD_A_SCPEN# in Reference Design- signal name DMD_A_SCPEN#_FILT after resistor - connects to DMD signal DMDSEL) | Lo | - | | DMD SCP Output Enable |
| DMD_B_RESET | AA12 | O | LVC MOS25_S_12_O | Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (signal name DMD_B_RESET_FILT after resistor - NC after that point) | - | - | | Not Used |
| DMD_B_SCPEN | AC14 | O | LVC MOS25_S_12_O | Connected in Reference Design to 36 Ω resistor with 27 pF cap to ground (called DMD_B_SCPEN# in Reference Design - signal name DMD_B_SCPEN#_FILT after resistor - NC after that point) | - | - | | Not Used |
| DMD_TYPE_0 | AA17 | O | LVC MOS25_F_12_O | | Hi = 1 | - | | DMD Attached Type bit 0 |
| DMD_TYPE_1 | AC16 | O | LVC MOS25_F_12_O | | Hi = 1 | - | | DMD Attached Type bit 1 |
| DMD_TYPE_2 | AB17 | O | LVC MOS25_F_12_O | | Hi = 1 | - | | DMD Attached Type bit 2 |
| DMD_TYPE_3 | AD15 | O | LVC MOS25_F_12_O | | Hi = 1 | - | | DMD Attached Type bit 3 |
| DONE_DDC | K10 | O | - | 4.7 kΩ pullup to 2.5V - connected to DLPR410 \overline{CE} pin and LED D3 pin 3 (cathode) in series with 62 Ω resistor to 3.3 V | Hi | - | | DLPR410 Initialization Routine Complete |
| DVALID_A_DPN | D20 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_A | | Bank A Valid Input Signal (Neg) |
| DVALID_A_DPP | D21 | I | LVDS_25_I | | - | DDC_DCLK_A | | Bank A Valid Input Signal (Pos) |
| DVALID_B_DPN | C8 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_B | | Bank B Valid Input Signal (Neg) |
| DVALID_B_DPP | D8 | I | LVDS_25_I | | - | DDC_DCLK_B | | Bank B Valid Input Signal (Pos) |
| DVALID_C_DPN | L19 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_C | | Bank C Valid Input Signal (Neg) |
| DVALID_C_DPP | L20 | I | LVDS_25_I | | - | DDC_DCLK_C | | Bank C Valid Input Signal (Pos) |
| DVALID_D_DPN | L3 | I | LVDS_25 | 100 Ω across pair (not terminated in the DLPC410) | - | DDC_DCLK_D | | Bank D Valid Input Signal (Neg) |
| DVALID_D_DPP | L4 | I | LVDS_25_I | | - | DDC_DCLK_D | | Bank D Valid Input Signal (Pos) |
| DXN_0 | R13 | - | NC | TP17 in Reference Design | - | - | | Dedicated Xilinx Temperature Diode (anode); Not Used in Reference Design |
| DXP_0 | R14 | - | NC | TP14 in Reference Design | - | - | | Dedicated Xilinx Temperature Diode (cathode); Not Used in Reference Design |
| ECP2_FINISHED | Y18 | O | LVC MOS25_F_12_O | Connected to LED D3 pin 2 (anode) in series with 62 Ω resistor to 3.3 V | Hi | - | | DLPR410 Initialization Routine Complete |
| ECP2_M_TP0 | AD11 | - | LVC MOS25_F_12_O | Mictor J8 Pin 2 in Reference Design | - | - | | Not Used - do not connect |
| ECP2_M_TP1 | AD10 | - | LVC MOS25_F_12_O | Mictor J8 Pin 4 in Reference Design | - | - | | Reserved - do not connect |
| ECP2_M_TP2 | AD8 | - | LVC MOS25_F_12_O | Mictor J8 Pin 6 in Reference Design | - | - | | Reserved - do not connect |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|-------------|------|------|------------------|--------------------------------------|----------------------|-------|--------------|----------------------------------|
| NAME | NO. | | | | | | | |
| ECP2_M_TP3 | AC8 | O | LVC MOS25_F_12_O | Mictor J8 Pin 8 in Reference Design | - | - | | Buffered data clock - test point |
| ECP2_M_TP4 | AC7 | O | LVC MOS25_F_12_O | Mictor J8 Pin 10 in Reference Design | - | - | | Reserved - do not connect |
| ECP2_M_TP5 | AC9 | O | LVC MOS25_F_12_O | Mictor J8 Pin 12 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP6 | AB9 | O | LVC MOS25_F_12_O | Mictor J8 Pin 14 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP7 | AA8 | O | LVC MOS25_F_12_O | Mictor J8 Pin 16 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP8 | AA9 | O | LVC MOS25_F_12_O | Mictor J8 Pin 18 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP9 | Y8 | O | LVC MOS25_F_12_O | Mictor J8 Pin 20 in Reference Design | - | - | | Reserved - do not connect |
| ECP2_M_TP10 | AB10 | O | LVC MOS25_F_12_O | Mictor J8 Pin 22 in Reference Design | Lo | | | Reserved - do not connect |
| ECP2_M_TP11 | AA10 | O | LVC MOS25_F_12_O | Mictor J8 Pin 24 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP12 | Y10 | O | LVC MOS25_F_12_O | Mictor J8 Pin 26 in Reference Design | Hi | | | DMD A/B bus OK - test point |
| ECP2_M_TP13 | AC11 | O | LVC MOS25_F_12_O | Mictor J8 Pin 28 in Reference Design | Hi | | | DMD C/D bus OK - test point |
| ECP2_M_TP14 | Y12 | O | LVC MOS25_F_12_O | Mictor J8 Pin 30 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP15 | Y11 | O | LVC MOS25_F_12_O | Mictor J8 Pin 32 in Reference Design | - | | | Reserved - do not connect |
| ECP2_M_TP16 | AB11 | O | LVC MOS25_F_12_O | Mictor J8 Pin 34 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP17 | H8 | O | LVC MOS25_F_12_O | Mictor J8 Pin 36 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP18 | H9 | O | LVC MOS25_F_12_O | Mictor J8 Pin 38 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP19 | F12 | O | LVC MOS25_F_12_O | Mictor J8 Pin 37 in Reference Design | - | - | | Reserved - do not connect |
| ECP2_M_TP20 | G11 | O | LVC MOS25_F_12_O | Mictor J8 Pin 35 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP21 | G12 | O | LVC MOS25_F_12_O | Mictor J8 Pin 33 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP22 | E11 | O | LVC MOS25_F_12_O | Mictor J8 Pin 31 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP23 | E10 | O | LVC MOS25_F_12_O | Mictor J8 Pin 29 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP24 | E8 | O | LVC MOS25_F_12_O | Mictor J8 Pin 27 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP25 | F10 | O | LVC MOS25_F_12_O | Mictor J8 Pin 25 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP26 | F9 | O | LVC MOS25_F_12_O | Mictor J8 Pin 23 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP27 | F8 | O | LVC MOS25_F_12_O | Mictor J8 Pin 21 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP28 | G10 | O | LVC MOS25_F_12_O | Mictor J8 Pin 19 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP29 | G9 | O | LVC MOS25_F_12_O | Mictor J8 Pin 17 in Reference Design | Hi | | | Reserved - do not connect |
| ECP2_M_TP30 | H11 | O | LVC MOS25_F_12_O | Mictor J8 Pin 15 in Reference Design | - | - | | Reserved - do not connect |
| ECP2_M_TP31 | H12 | O | LVC MOS25_F_12_O | Mictor J8 Pin 13 in Reference Design | - | - | | Reserved - do not connect |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|--------------|---|------|-------------------|---|-------------------|--------------|-----------|---------------------------------------|
| NAME | NO. | | | | | | | |
| GND | A1, A6, A11, A16, A21, A26, AA1, AA11, AA21, AA26, AB8, AB18, AC5, AC15, AC25, AD2, AD12, AD22, AE4, AE9, AE14, AE19, AF1, AF6, AF11, AF16, AF21, AF26, B3, B8, B13, B18, C5, C15, C25, D2, D12, D22, E9, E19, F1, F6, F16, F26, G3, G13, G18, G23, H10, H20, J7, J9, J13, J15, J17, K4, K8, K12, K14, K16, K19, K24, L1, L9, L11, L13, L15, L17, L21, L26, M3, M8, M10, M12, M16, M18, N5, N9, N11, N15, N17, N25, P2, P7, P8, P10, P12, P16, P22, R9, R11, R15, R17, R19, T1, T6, T8, T10, T12, T14, T16, T26, U3, U9, U13, U15, U17, U18, U23, V8, V10, V14, V16, V20, W7, W9, W13, W15, W17, Y4, Y14, Y16, Y19, Y24 | - | GND | | - | - | | Connect to Ground |
| HSWAPEN | L18 | - | - | 4.7 kΩ pullup to 2.5 V | - | - | | Xilinx Configuration |
| INIT_ACTIVE | AA18 | O | LVCNOS25_F_12_O | | Hi | - | | DLPC410 Initialization Routine Active |
| INTB_DDC | J11 | - | - | 4.7 kΩ pullup to 2.5 V connected to DLPR410 OE/RESET | Hi | - | | Xilinx Configuration |
| LOAD4 | AB21 | - | LVCNOS25_F_12_I/O | Previously DDC_SPARE_0, connected to Applications FPGA (U5) pin AD19 in Reference Design. Weak internal pull-up. Pull-up to logic '1' if LOAD4 is unused. | - | - | | LOAD4 mode enable |
| NS_FLIP | F19 | I | LVCNOS25_S_12_I | | Hi | - | | Top/Bottom image flip on DMD |
| PROGB_DDC | J18 | | - | 4.7 kΩ pullup to 2.5 V connected to DLPR410 CF | Hi | - | | Xilinx Configuration |
| PROM_CCK_DDC | J10 | I | LVCNOS25_S_12 | Connected to center of voltage divider (100/100 Ω) and through R53 to DLPR410 CLKOUT | - | PROM_CCK_DDC | | Configuration PROM Clock |
| PROM_D0_DDC | K11 | - | - | Connected to DLPR410 Data 0 (D0) | - | PROM_CCK_DDC | | Configuration PROM Data Out |
| PWR_FLOAT | AC17 | I | LVCNOS25_S_12_I | Connected to output of U22 NOR Gate (inputs V5_PWR_FLOAT and PWRGD) | Hi | - | | DMD Power Good indicator |
| RDWR_B | P18 | - | - | 1 kΩ pulldown to ground | - | - | | Xilinx Configuration |
| ROWAD_0 | D14 | I | LVCNOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 0 |
| ROWAD_1 | D15 | I | LVCNOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 1 |
| ROWAD_2 | E15 | I | LVCNOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 2 |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|--------------|------|------|------------------|---|-------------------|----------|-----------|-------------------------------------|
| NAME | NO. | | | | | | | |
| ROWAD_3 | F14 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 3 |
| ROWAD_4 | G14 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 4 |
| ROWAD_5 | E16 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 5 |
| ROWAD_6 | F15 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 6 |
| ROWAD_7 | G15 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 7 |
| ROWAD_8 | E17 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 8 |
| ROWAD_9 | F17 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 9 |
| ROWAD_10 | G16 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Address bit 10 |
| ROWMD_0 | H17 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Mode bit 0 |
| ROWMD_1 | H16 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | DMD Row Mode bit 1 |
| RST_ACTIVE | AB16 | I | LVC MOS25_F_12_O | | Hi = 1 | - | | DMD Reset in Progress |
| RST2BLK | E18 | I | LVC MOS25_S_12_I | | Hi = 1 | - | | Dual Block Reset bit |
| RSVD_0 | R18 | - | - | Connect to Ground | - | - | | Not Used - must be tied to Ground |
| RSVD_1 | T18 | - | - | Connect to Ground | - | - | | Not Used - must be tied to Ground |
| SCPCLK | AB15 | | LVC MOS25_F_12_O | Connected to DLPA200 Number 1 and Number 2 SCPCLK and to R105 36 Ω filter resistor with 27 pF cap after - called DMD_A_SCPCLK_FILTER after - connects to DMD SCPCLK (also connects to R97 filter resistor with 27 pF cap after - called DMD_B_SCPCLK_FILTER but NC after) | - | SCPCLK | | SCP Clock |
| SCPDI | AA15 | I | LVC MOS25_S_12_I | 1 kΩ pullup to 2.5 V - connects to DLPA200 Number 1 and Number 2 SCPDO and to DMD SCPDO through flex A - on DMD board there is an LCR filter [2 x 100 pF caps, inductor and 34 Ω resistor] also connects to flex B but NC on other end. | - | SCPCLK | | SCP data input to DLPC410 |
| SCPDO | AA14 | O | LVC MOS25_F_12_O | 1 kΩ pullup to 2.5 V - connects to DLPA200 Number 1 and Number 2 SCPDI and to R96 filter cap with 27 pF cap after - called DMD_A_FILTER - connect through flex A to DMD SCPDI - also connects to R71 36 Ω filter resistor with 27 pF cap to DMD_B_SCPDO_FILTER but NC on other end. | - | SCPCLK | | SCP data output from DLPC410 |
| STEPVCC | Y13 | - | LVC MOS25_S_12_I | 1 kΩ pulldown to ground | - | - | | Not Used |
| TCK_JTAG | U11 | | - | Connects to DLPC410, DLPR410, and JTAG header TCK (if user has JTAG they must build their chain accordingly) | - | TCK_JTAG | | JTAG Clock |
| TDO_DDC | W10 | | - | Connects to JTAG return TDO on JTAG header | - | TCK_JTAG | | JTAG data out of DLPC410 |
| TDO_XCF16DDC | V11 | | - | Connects to DLPR410 TDO (DLPC410 internal signal TDI_0) | - | TCK_JTAG | | JTAG data out of DLPR410 to DLPC410 |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|-----------|---|------|------------------|---|-------------------|----------|-----------|--|
| NAME | NO. | | | | | | | |
| TMS_JTAG | V12 | | - | Connects to DLPC410, DLPR410, and JTAG header TMS | Hi | TCK_JTAG | | JTAG |
| VBATT_0 | K18 | | - | Connected to 4.7 kΩ pullup to 2.5 V | - | - | | Not Used |
| VCCAUX | J8, K17, L8, M17, N8, P17, R8, T17, U8, V17, W8, W16 | | POWER | VCC_2P5V | - | - | | Aux Power |
| VCCINT | H15, J12, J14, J16, K9, K13, K15, L10, L12, L14, L16, M9, M11, M15, N10, N12, N16, P9, P11, P15, R10, R12, R16, T9, T11, T13, T15, U10, U12, U14, U16, V9, V13, V15, W14, Y15 | | POWER | VCC_1P0V | - | - | | Power |
| VCCO_0_1 | Y9 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_0_2 | W12 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_1_1 | C10 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_1_2 | F11 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_2_1 | AA16 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_2_2 | AD17 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_3_1 | E14 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_3_2 | D17 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_4_1 | AC10 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_4_2 | AB13 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_11_1 | F21 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_11_2 | J22 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_11_3 | H25 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_12_1 | J2 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_12_2 | H5 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_12_3 | L6 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_13_1 | R24 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_13_2 | M23 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_13_3 | N20 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_14_1 | V5 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_14_2 | R4 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_14_3 | W2 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_15_1 | E24 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_15_2 | B23 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_15_3 | C20 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_16_1 | G8 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_16_2 | D7 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_16_3 | E4 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_17_1 | V25 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_17_2 | W22 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_17_3 | T21 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_18_1 | AD7 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_18_2 | AA6 | | POWER | VCC_2P5V | - | - | | Power |
| VCCO_18_3 | AB3 | | POWER | VCC_2P5V | - | - | | Power |
| VLED0 | AC18 | O | LVC MOS25_F_12_O | Connects to LED D9 in series with 22.1 Ω resistor to 2.5 V | Hi = On | - | | Power Indicator LED Output |
| VLED1 | AD18 | O | LVC MOS25_F_12_O | Connects to LED D10 in series with 22.1 Ω resistor to 2.5 V | Hi = On | - | | Heartbeat Indicator LED Output |
| VN_0 | P13 | - | - | Connect to Ground | - | - | | Xilinx System Monitor (not used - must be connected to ground) |

Pin Functions (continued)

| PIN | | TYPE | SIGNAL | TERMINATION /NOTES | ACTIVE (Hi or Lo) | CLOCK | DATA RATE | DESCRIPTION |
|----------|--|------|------------------|---|-------------------|-------|-----------|--|
| NAME | NO. | | | | | | | |
| VP_0 | N14 | - | - | Connect to Ground | - | - | | Xilinx System Monitor (not used - must be connected to ground) |
| VREFN_0 | N13 | - | LVC MOS25_S_12 | Connect to Ground | - | - | | Xilinx System Monitor reference voltage (not used - must be connected to ground) |
| VREFP_0 | P14 | - | LVC MOS25_S_12 | Connect to Ground | - | - | | Xilinx System Monitor reference ground (not used - must be connected to ground) |
| WDT_ENBL | AA13 | I | LVC MOS25_S_12_I | | Lo | - | | DMD Mirror Clocking Pulse Watchdog Timer Enable |
| UNUSED | AB23, AC20, AD9, AD16, AD20, AD21, AD23, AD24, AD25, AD26, AE7, AE8, AE10, AE11, AE12, AE13, AE15, AE16, AE17, AE18, AE20, AE21, AE22, AE23, AE24, AE25, AE26, AF7, AF8, AF9, AF10, AF12, AF13, AF14, AF15, AF17, AF18, AF19, AF20, AF22, AF23, AF24, AF25 | | NC | No Connection (listed as Xilinx NC0 - NC42) | - | - | | Unused Pins |

7 Specifications

NOTE

The information contained in the following sections has been adapted from the Xilinx XC5VLX30 data sheet. For any information beyond what is listed here, consult the Xilinx XC5VLX30 data sheet. Where appropriate, DLPC410 specific values have been substituted in place of generic parameters.

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|-------------------------------|---|-------|-------|------------------------|---|
| ELECTRICAL | | | | | |
| Supply voltage ⁽²⁾ | V _{CCINT} | –0.5 | 1.05 | V | |
| | V _{CCO} | –0.5 | 3.45 | V | |
| | V _{CCAUX} | 2.35 | 2.625 | V | |
| V _I | Input voltage ⁽³⁾ | 2.5 V | –0.75 | V _{CCO} + 0.5 | V |
| V _O | Output voltage ⁽⁴⁾ | 2.5 V | –0.3 | V _{CCO} + 0.3 | V |
| ENVIRONMENTAL | | | | | |
| T _A | Operating free-air temperature ⁽⁵⁾ | 0 | 85 | °C | |
| T _{stg} | Storage temperature | –65 | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Applies to external input and bidirectional buffers.
- (4) Applies to external output and bidirectional buffers.
- (5) Maximum Ambient Temperature may be further limited by the device's power dissipation (which is data and configuration dependent), air flow and resultant junction temperature.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--|---|-------|------|
| V _(ESD) | Electrostatic discharge | | |
| | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 2000 | V |
| Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 400 | | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--------------------|---|------------|-------|------------------|------|
| V _{CCINT} | 1-V Supply voltage, core logic | 0.95 | 1.00 | 1.05 | V |
| V _{CCO} | 2.5-V Supply voltage, I/O | 1.14 | 2.50 | 3.45 | V |
| V _{CCAUX} | 2.5-V Supply voltage, I/O | 2.375 | 2.500 | 2.625 | V |
| V _I | Input voltage | 2.5-V CMOS | 0 | V _{CCO} | V |
| | | 2.5-V LVDS | 0.3 | 2.2 | |
| V _O | Output voltage | 2.5-V CMOS | 0 | V _{CCO} | V |
| | | 2.5-V LVDS | 0.825 | 1.675 | |
| T _J | Operating junction temperature ⁽¹⁾ | 0 | | 125 | °C |
| P _D | Continuous total power dissipation | | 2.7 | 2.8 | W |

- (1) Thermal analysis and design should be carefully considered to ensure that the junction temperature is maintained within the above specifications.

7.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------------|-----------------|---------------------|-----|-----|------|
| V _{IH} | High-level Input voltage | 2.5-V CMOS | 1.7 | | | V |
| V _{IL} | Low-level Input voltage | 2.5-V CMOS | | | 0.7 | V |
| V _{OH} | High-level output voltage | 2.5-V Interface | V _{CCO} -4 | | | V |
| | | 2.5-V LVDS | 1.38 | | | |
| V _{OL} | Low-level output voltage | 2.5-V Interface | | | 0.4 | V |
| | | 2.5-V LVDS | 1.03 | | | |
| C _I | Input capacitance | 2.5-V Interface | 8 | | | pF |
| | | 2.5-V LVDS | 8 | | | |
| I _{CCINT} | Supply voltage range, core supply | | 300 | | | mA |
| I _{CCO} | Supply voltage range, I/O supply | | 850 | | | mA |

7.5 Timing Requirements

 (see ⁽¹⁾)

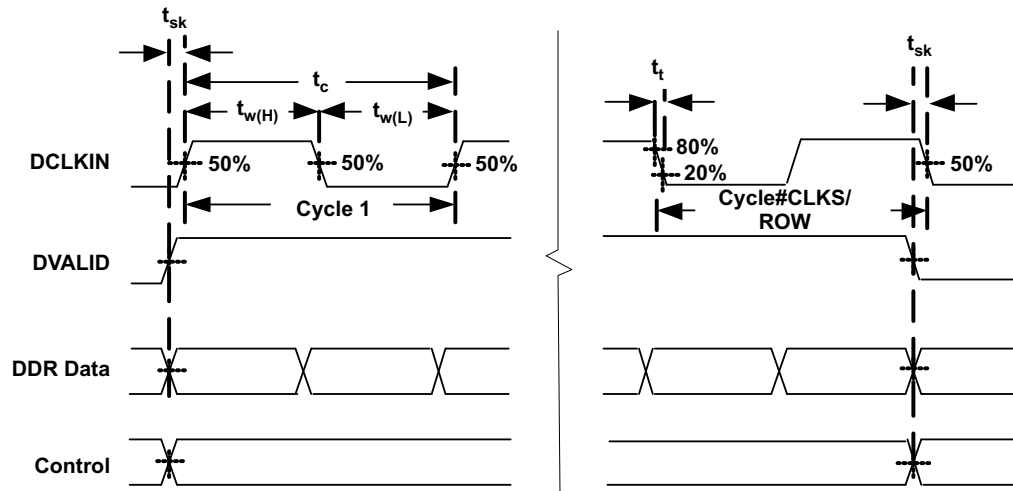
| | | | MIN | NOM | MAX | UNIT |
|-------------------|---|--------------------------------------|------|------|------|------|
| f _{cd} | Clock frequency, DCLKIN_n ⁽²⁾ | | 395 | 400 | 400 | MHz |
| f _{cr} | Clock frequency, CLK_R | | | 50 | | MHz |
| t _c | Cycle time, DCLKIN_n | | 2.5 | 2.5 | 2.53 | ns |
| t _{w(H)} | Pulse duration, high | 50% to 50% reference points (signal) | 1.25 | 1.25 | 1.27 | ns |
| t _{w(L)} | Pulse duration, low | 50% to 50% reference points (signal) | 1.25 | 1.25 | 1.27 | ns |
| t _t | Transition time, t _t = t _r / t _f | 20% to 80% reference points (signal) | | | .6 | ns |
| t _{jp} | Period Jitter DCLKIN_n ⁽³⁾ | | | 150 | | ps |
| t _{sk} | Skew, DIN_A(15-0) to DCLKIN_A | | -150 | | 150 | ps |
| | Skew, DIN_B(15-0) to DCLKIN_B | | -150 | | 150 | |
| | Skew, DIN_C(15-0) to DCLKIN_C | | -150 | | 150 | |
| | Skew, DIN_D(15-0) to DCLKIN_D | | -150 | | 150 | |
| | Skew, DVALID_n to DCLKIN_n↑ | | -150 | | 150 | |
| | Skew, BLK_MD BLK_AD to DCLKIN_n↑ ⁽⁴⁾ | | -150 | | 150 | |
| | Skew, ROWMD or ROWAD to DCLKIN_n↑ ⁽⁴⁾ | | -150 | | 150 | |
| | Skew, STEPVCC to DCLKIN↑ ⁽⁴⁾ | | -150 | | 150 | |

(1) It is recommended that the COMP_DATA, NS_FLIP and RST2BLK inputs be set to one value and not adjusted during normal system operation.

(2) Preferred DCLKIN_n duty cycle = 50%

(3) This is the deviation in period from ideal period due solely to high frequency jitter.

(4) First edge of DIN*, ROW*, BLK* and STEPVCC should be synchronous to DVALID rising edge


Figure 2. Input Interface Timing
NOTE

Dynamic changes to $\overline{RST2BLK}$, NS_FLIP and COMP_DATA during normal operation are not recommended.

8 Detailed Description

8.1 Overview

The DLPC410 DMD Digital Controller enables customers to stream binary pattern data to the DLP650LNIR, DLP7000(UV), or DLP9500(UV) DMD for very high speed binary pattern imaging applications. The DLPC410 receives customer input binary pattern data on a row by row basis and passes the pattern data to the connected DMD. Concurrent with the receipt of data, the DLPC410 captures the customer requested ROW mode and ROW address which determines if row loading starts at the top (or bottom) of the DMD and increments (or decrements) to the next row for the next Row Cycle, or if a specific row address is specified for loading the next pattern data. Each DMD micromirror is individually configurable through this data loading process which enables precise, predictable control of each and every micromirror in the DMD Micromirror array.

The DLPC410 also receives customer input control information instructing the DLPC410 to command the DLPA200 device(s) to generate the Mirror Clocking Pulses (MCPs) to the DMD – these MCPs are necessary for the DMD micromirrors to transition from their current state to their new state, the new state being determined by the new data just loaded into the DMD. A feedback signal from the DLPC410 frames the MCP such that the customer knows the MCP request has been received by the DLPC410 and when the MCP is completed.

The DLPC410 supports multiple MCP modes of operation. The DMD Micromirror arrays are arranged into horizontal Reset Blocks – there are typically 16 horizontal Reset Blocks per DMD where each Reset Block receives a single MCP to initiate the Micromirror state change. DMD blocks can be Reset one at a time or all at once. In certain modes, adjacent blocks of 2 or of 4 Reset Blocks can be Reset at the same time. This flexibility provides great advantages to optimizing the time certain DMD blocks are in certain states, which in turn can provide speed advantages or extend DMD illumination windows (the duration for which a solid state illuminator should be illuminating).

Behind the scenes, the DLPC410 also communicates directly with the control logic of the DMD to read part type and status information and to configure the DMD for proper operation. The DLPC410 is always paired with the DLPR410 PROM as the DLPR410 provides the configuration bit stream which configures the DLPC410 to be a DMD Digital Controller. The DLPC410 also drives one DMD at a time, and that DMD could require either one or two DLPA200 devices depending on the DMD type. For further information, refer to [Table 11](#) or the individual DMD datasheets (links can be found in [Table 25](#)).

8.2 Functional Block Diagrams

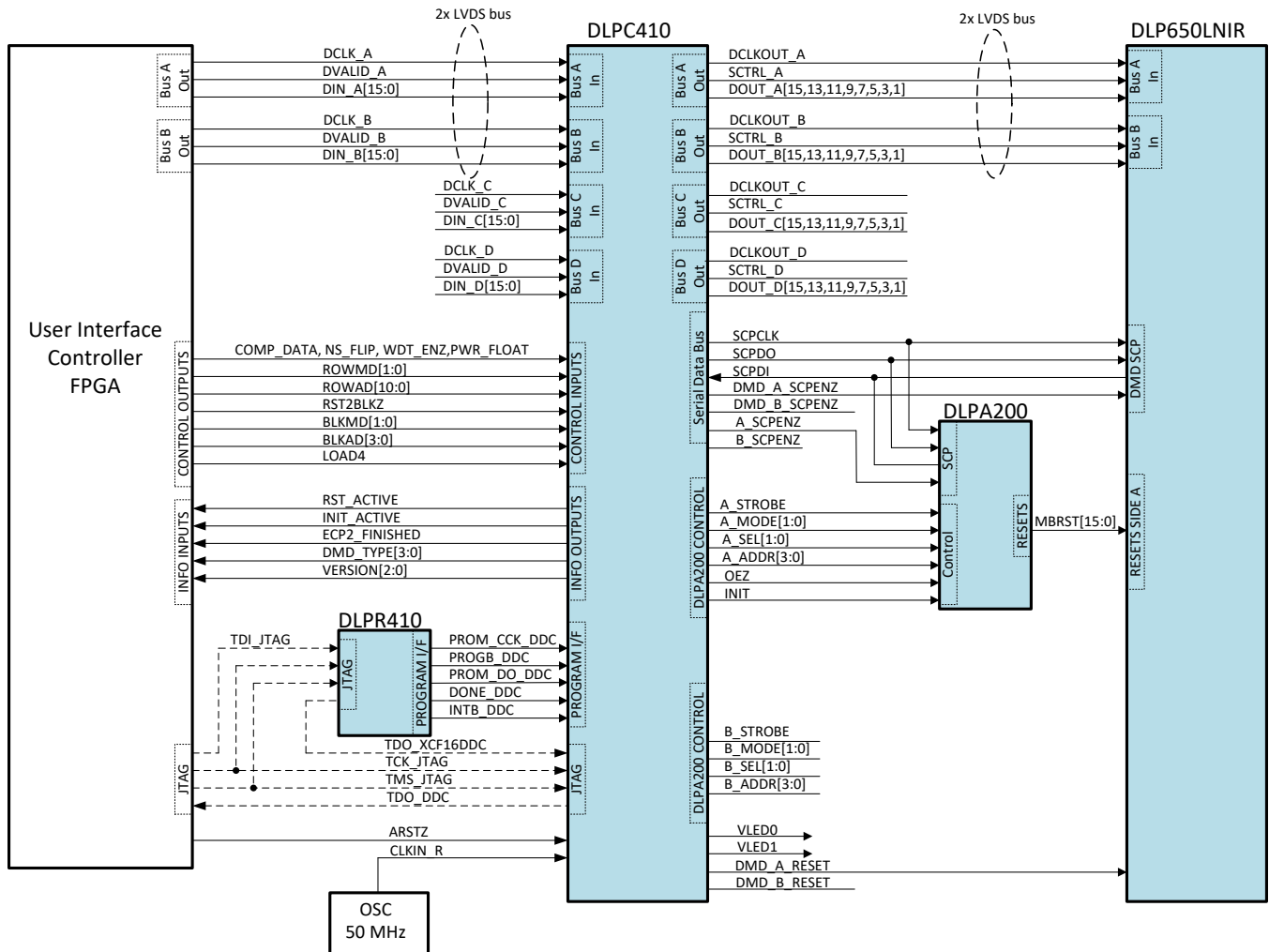


Figure 3. DLPC410 and DLP650LNIR DMD Functional Block Diagram

Functional Block Diagrams (continued)

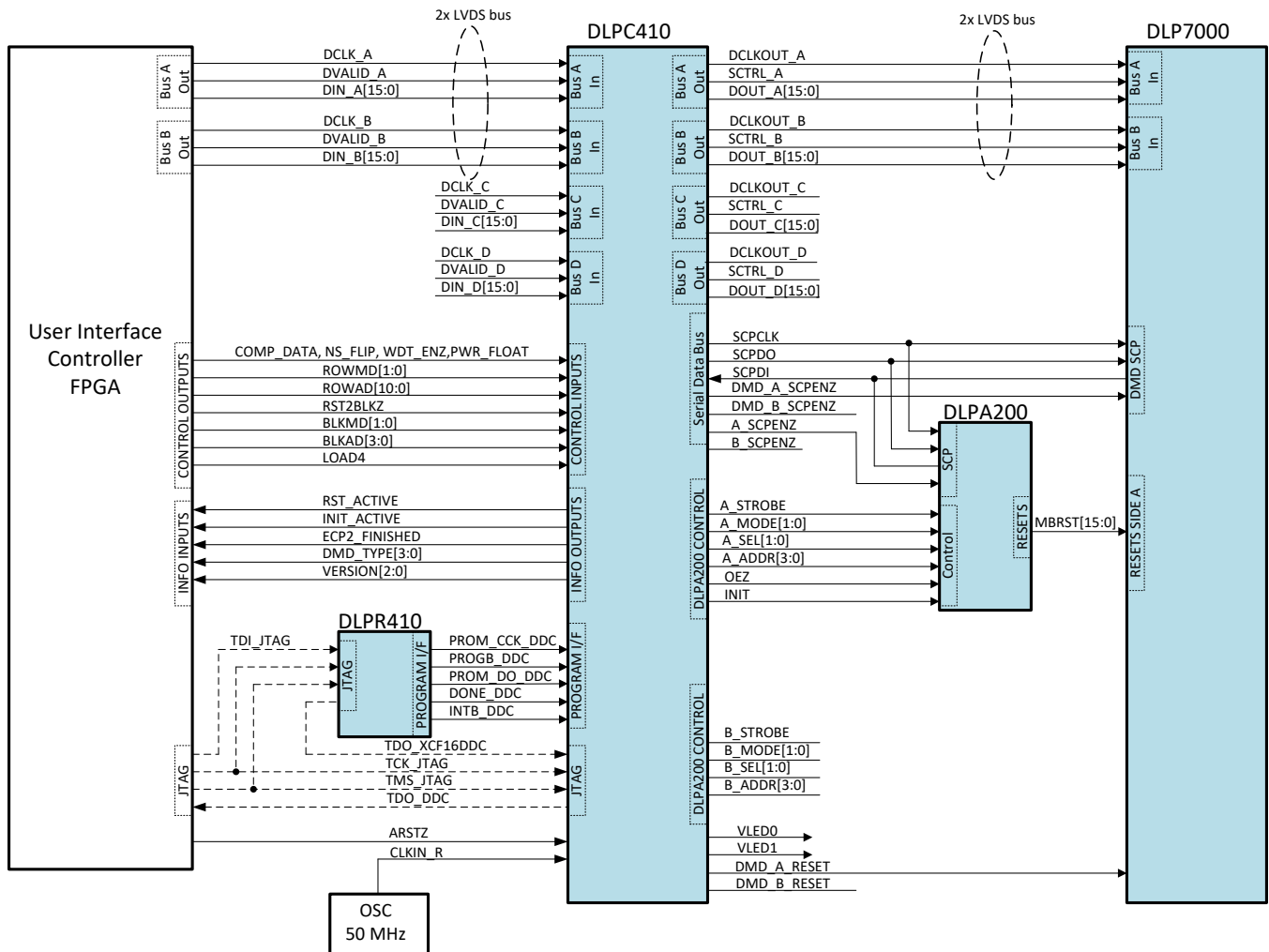


Figure 4. DLPC410 and DLP7000 / DLP7000UV Functional Block Diagram

Functional Block Diagrams (continued)

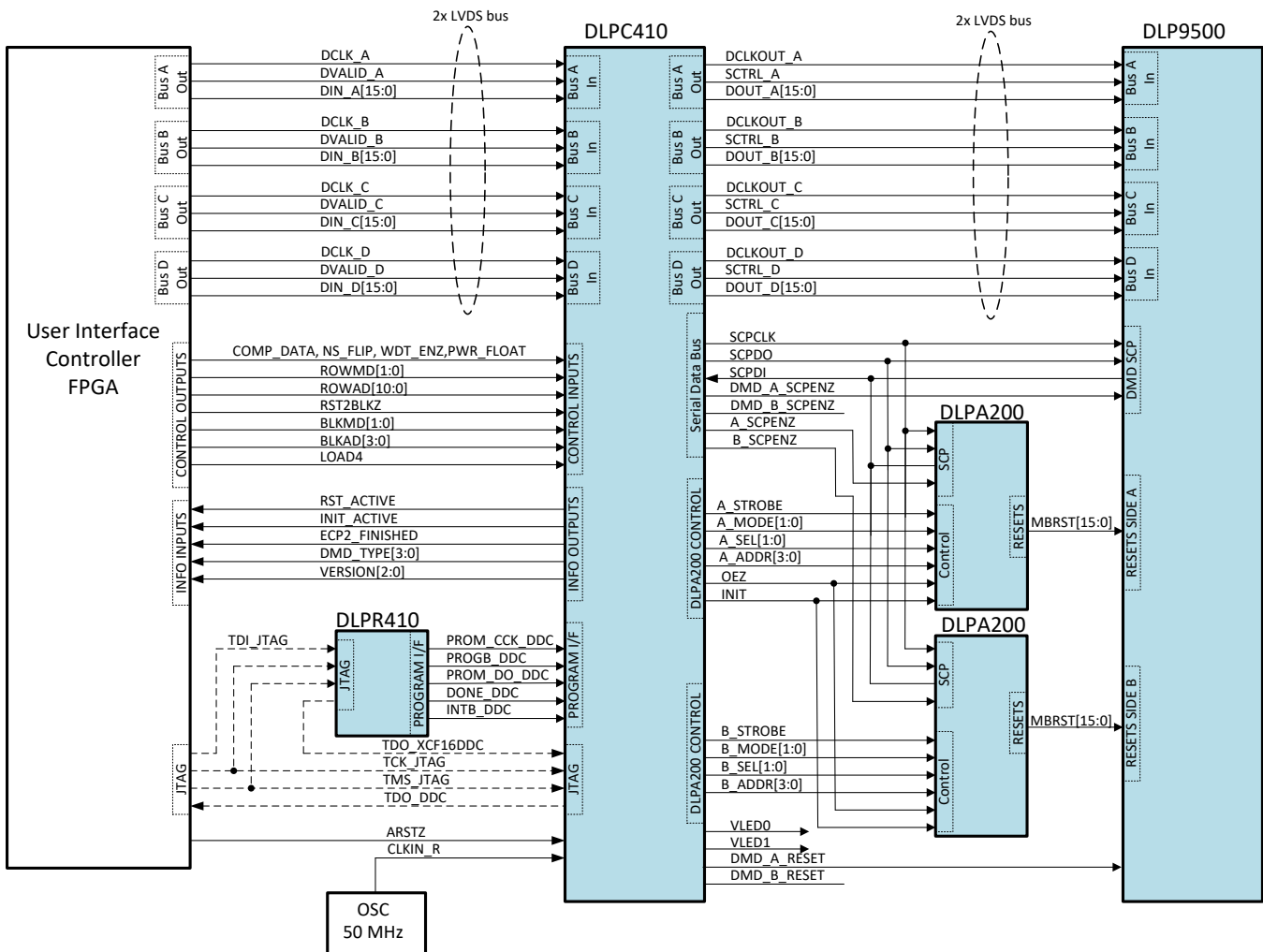


Figure 5. DLPC410 and DLP9500 / DLP9500UV Functional Block Diagram

8.3 Feature Description

8.3.1 DLPC410 Binary Pattern Data Path

The DLPC410 receives binary pattern input data from the customer application formatted specifically for display on one of the DLPC410 compatible DMDs. This data is captured on a row by row basis using specific data formats with multiple signals which frame the data and provided control information from the customer defining where in the DMD the data is destined. The DLPC410 then sends the pattern data to the DMD and uses the received control information to decode and provide the correct control information to the DMD and other DLP components.

8.3.1.1 DIN_A, DIN_B, DIN_C, DIN_D Input Data Buses

The DLPC410 has four differential 16-bit input data buses (A/B/C/D). Which of these input data bus signals are used at any given time is specific to the DMD connected to the DLPC410 in the system. The data buses are 2xLVDS double-data-rate (DDR) buses which can transfer data at 800 MHz data rates per input. Data should be synchronous and edge aligned with the input clocks for each specific data bus (A, B, C, or D). Depending on the design, skewing the clock to data relationship may cause a problem. For timing constraints for the input data clock to either the input data and/or DVALID, refer to [Timing Requirements](#)

Feature Description (continued)

8.3.1.2 DCLKIN Input Clocks

DCLKIN is the differential input clock for each DLPC410 input data bus. There are four input clocks, one for each bus (A/B/C/D). DCLKIN is a 400 MHz clock to the DMD which should be synchronous and edge aligned with all data and control signals for that specific bus (A, B, C, or D). Depending on the design, skewing the clock to data relationship may cause a problem. For timing constraints for the input data clock to either the input data and/or DVALID, refer to [Timing Requirements](#). Care should be taken to keep clock jitter of these signals to a minimum.

8.3.1.3 DVALID Input Signals

The DVALID signal is a differential input signal, one for each input data bus (A/B/C/D), which indicates that data being presented to the DLPC410 is valid. DVALID assertion latches the following types of data into the DLPC410 for decoding or passing information to the DMD:

- Binary pattern data on input data buses A/B/C/D
- Row Mode
- Row Address
- Block Mode
- Block Address
- RST2BLK signal

DVALID and all other inputs listed above should be synchronous to DCLKIN. DVALID can be asserted in one of the three following ways:

- DVALID can frame (remain active) individual DMD row loads with breaks between rows.
- DVALID can frame continuous DMD block loads of multiple rows with breaks between blocks
- DVALID can frame (remain active) the entire DMD device load (all rows) without any breaks.

If the DVALID frames individual blocks or the entire DMD, ensure that block and row controls are adjusted at the proper locations in the data stream. See section [DLPC410 Initialization and Training](#) for further information.

NOTE

After an active DVALID signal transitions inactive (low), DVALID should only transition to active again on even number of clocks later, i.e. 2, 4, 6, etc.

8.3.1.4 DOUT_A, DOUT_B, DOUT_C, DOUT_D Output Data Buses

The DLPC410, having captured the incoming pattern data on its input data buses, provides this data on an equivalent number of output data buses. The DLPC410 has four differential 16-bit output data buses (A/B/C/D), which are aligned to its input data buses. Which of these input data bus signals are used at any given time is specific to the DMD connected to the DLPC410 in the system. The data buses are 2xLVDS double-data-rate (DDR) buses which can transfer data at 800 MHz data rates per output. Data should be synchronous and edge aligned with the output clocks for each specific data bus (A, B, C, or D). Depending on the design, skewing the clock to data relationship may cause a problem. For timing constraints for the output data clock to the output data, refer to [Timing Requirements](#).

8.3.1.5 DCLKOUT Output Clocks

DCLKOUT is the differential output clock for each DLPC410 output data bus. There are four output data clocks, one for each bus (A/B/C/D) to the DMD. DCLKOUT is a 400 MHz clock to the DMD which should be synchronous and edge aligned with all data and control signals for that specific bus (A, B, C, or D). Depending on the design, skewing the clock to data relationship may cause a problem. For timing constraints for the output data clocks to either the output data and/or SCTRL signals, refer to [Timing Requirements](#).

Feature Description (continued)

8.3.1.6 SCTRL Output Signals

The SCTRL signal is a differential output signal to the DMD which provides DMD control information. There are four SCTRL differential pair signals, one for each bus (A/B/C/D). The control information is generated internally to the DLPC410 and is specific to the connected DMD. Data should be synchronous and edge aligned with the output clocks for each specific data bus (A, B, C, or D). Depending on the design, skewing the clock to SCTRL relationship may cause a problem. For timing constraints for the output data clock to the SCTRL signals, refer to [Timing Requirements](#).

8.3.1.7 Supported DMD Bus Sizes

The DLPC410 supports the 2xLVDS Data Bus DMD types as shown in [Table 11](#).

Table 2. DMD Row Sizes, Bus Widths, and Row Lengths

| TYPE | PIXELS PER ROW | INPUT / OUTPUT BUSS | NO. OF DATA LINES | CLOCKS PER ROW |
|----------------------------|----------------|--|-------------------|----------------|
| DLP650LNIR DMD | 1280 | A[15,13,11,9,7,5,3,1] B[15,13,11,9,7,5,3,1] | 16 | 40 |
| DLP7000 and DLP7000UV DMDs | 1024 | A[15:0] B[15:0] | 32 | 16 |
| DLP9500 and DLP9500UV DMDs | 1920 (2048) | A[15:0] B[15:0] C[15:0] D[15:0] | 64 | 16 |

8.3.1.8 Row Cycle definition

A Row Cycle relates to specific number of input data clocks it takes for the customer to send one row of input binary pattern data to one row of the DMD. DVALID starts the Row Cycle by transitioning to an active (logic '1') state. The row cycle ends after the appropriate number of clock cycles per row are applied. Any input data on the DIN input data buses should be appropriately provided during the Row Cycle. [Table 2](#) shows the number of input data clocks needing to populate one row of the DMD using the number of data lines identified in the table. Other Row and Block related signals are captured at the start of a row cycle and will be discussed later.

There is also a unique row cycle called a No-Op Row Cycle which does not provide any valid input data nor any valid block command. It is typically used to do nothing except provide the DLPC410 and DMD time to perform internal actions already in process. The No-Op Row Cycle is discussed in [No-Op Row Cycle Description](#).

8.3.1.9 DLP9500 and DLP9500UV Input Data Formatting

Figure 6 details one Row Cycle of input data formatting for the DLP9500 and DLP9500UV DMDs. For brevity, only two data bits of all four 16 bit data bus (A/B/C/D) signals are shown, but there is enough information presented to allow extrapolation to all data bus signals not shown.

Table 3, Table 4, Table 5, and Table 6 show how each pixel of the DLP9500 and DLP9500UV DMDs maps to individual data bus inputs and input clock edges within each row cycle. Because these DMDs are actually 2048 pixels per row with only 1920 micromirrors per row, no visible data is loaded for the first clock cycle for A and B data and for the last clock cycle for C and D data for each row load operation. This only applies to the DLP9500 and DLP9500UV. For readability purposes, input buses DIN_A, DIN_B, DIN_C, and DIN_D are abbreviated as D_A, D_B, D_C, and D_D. DCLKIN has been shortened to DCLK.

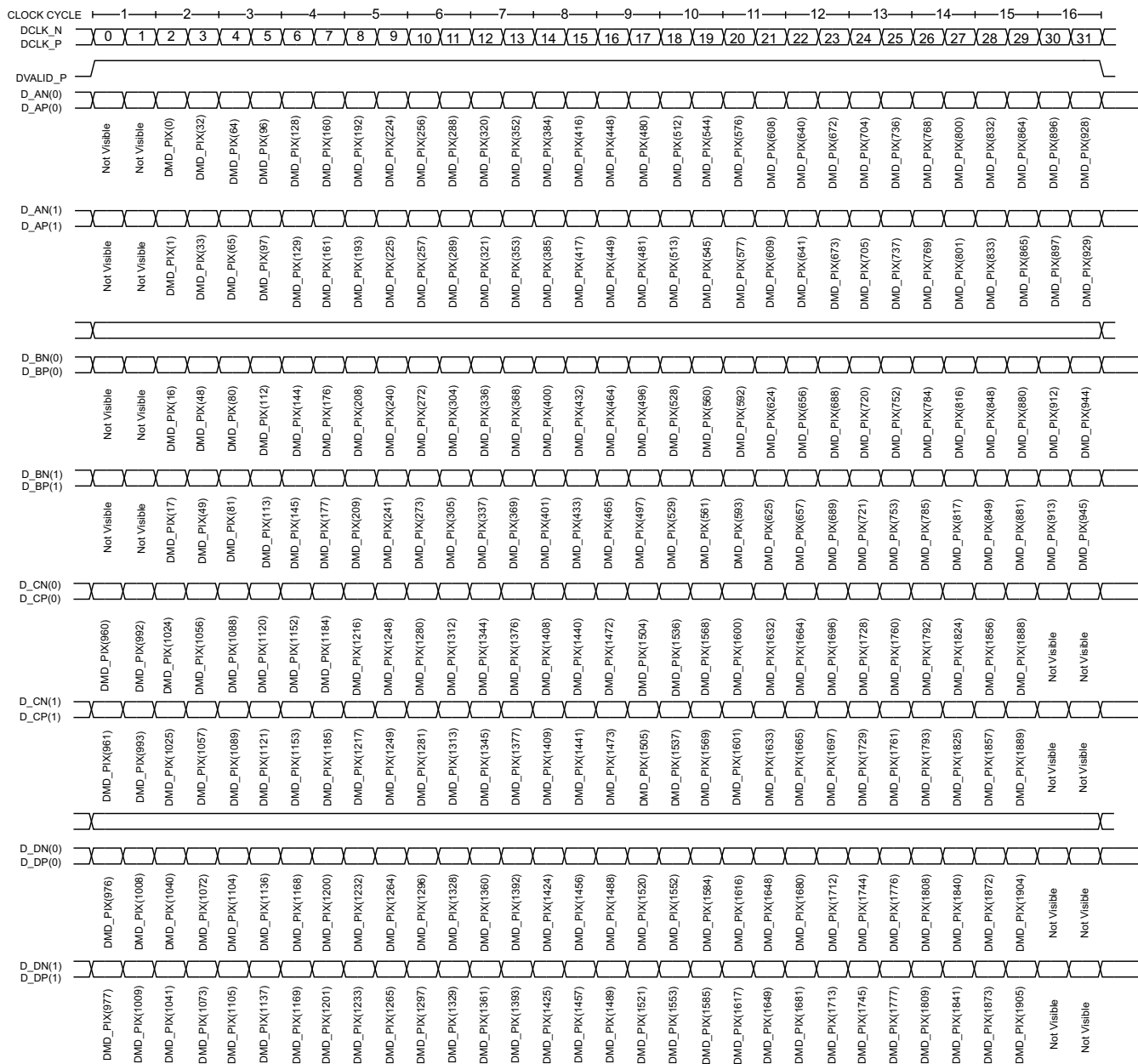


Figure 6. DLP9500 / DLP9500UV 2XLVDS DMD Input Data Bus

Table 3. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_A(15:0)

| DCLK EDGE | D_A(0) | D_A(1) | D_A(2) | D_A(3) | D_A(4) | D_A(5) | D_A(6) | D_A(7) | D_A(8) | D_A(9) | D_A(10) | D_A(11) | D_A(12) | D_A(13) | D_A(14) | D_A(15) |
|-----------|-------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|
| 0 | Not Visible | | | | | | | | | | | | | | | |
| 1 | Not Visible | | | | | | | | | | | | | | | |
| 2 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 3 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| 4 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 |
| 5 | 96 | 97 | 98 | 99 | 100 | 101 | 102 | 103 | 104 | 105 | 106 | 107 | 108 | 109 | 110 | 111 |
| 6 | 128 | 129 | 130 | 131 | 132 | 133 | 134 | 135 | 136 | 137 | 138 | 139 | 140 | 141 | 142 | 143 |
| 7 | 160 | 161 | 162 | 163 | 164 | 165 | 166 | 167 | 168 | 169 | 170 | 171 | 172 | 173 | 174 | 175 |
| 8 | 192 | 193 | 194 | 195 | 196 | 197 | 198 | 199 | 200 | 201 | 202 | 203 | 204 | 205 | 206 | 207 |
| 9 | 224 | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 232 | 233 | 234 | 235 | 236 | 237 | 238 | 239 |
| 10 | 256 | 257 | 258 | 259 | 260 | 261 | 262 | 263 | 264 | 265 | 266 | 267 | 268 | 269 | 270 | 271 |
| 11 | 288 | 289 | 290 | 291 | 292 | 293 | 294 | 295 | 296 | 297 | 298 | 299 | 300 | 301 | 302 | 303 |
| 12 | 320 | 321 | 322 | 323 | 324 | 325 | 326 | 327 | 328 | 329 | 330 | 331 | 332 | 333 | 334 | 335 |
| 13 | 352 | 353 | 354 | 355 | 356 | 357 | 358 | 359 | 360 | 361 | 362 | 363 | 364 | 365 | 366 | 367 |
| 14 | 384 | 385 | 386 | 387 | 388 | 389 | 390 | 391 | 392 | 393 | 394 | 395 | 396 | 397 | 398 | 399 |
| 15 | 416 | 417 | 418 | 419 | 420 | 421 | 422 | 423 | 424 | 425 | 426 | 427 | 428 | 429 | 430 | 431 |
| 16 | 448 | 449 | 450 | 451 | 452 | 453 | 454 | 455 | 456 | 457 | 458 | 459 | 460 | 461 | 462 | 463 |
| 17 | 480 | 481 | 482 | 483 | 484 | 485 | 486 | 487 | 488 | 489 | 490 | 491 | 492 | 493 | 494 | 495 |
| 18 | 512 | 513 | 514 | 515 | 516 | 517 | 518 | 519 | 520 | 521 | 522 | 523 | 524 | 525 | 526 | 527 |
| 19 | 544 | 545 | 546 | 547 | 548 | 549 | 550 | 551 | 552 | 553 | 554 | 555 | 556 | 557 | 558 | 559 |
| 20 | 576 | 577 | 578 | 579 | 580 | 581 | 582 | 583 | 584 | 585 | 586 | 587 | 588 | 589 | 590 | 591 |
| 21 | 608 | 609 | 610 | 611 | 612 | 613 | 614 | 615 | 616 | 617 | 618 | 619 | 620 | 621 | 622 | 623 |
| 22 | 640 | 641 | 642 | 643 | 644 | 645 | 646 | 647 | 648 | 649 | 650 | 651 | 652 | 653 | 654 | 655 |
| 23 | 672 | 673 | 674 | 675 | 676 | 677 | 678 | 679 | 680 | 681 | 682 | 683 | 684 | 685 | 686 | 687 |
| 24 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | 712 | 713 | 714 | 715 | 716 | 717 | 718 | 719 |
| 25 | 736 | 737 | 738 | 739 | 740 | 741 | 742 | 743 | 744 | 745 | 746 | 747 | 748 | 749 | 750 | 751 |
| 26 | 768 | 769 | 770 | 771 | 772 | 773 | 774 | 775 | 776 | 777 | 778 | 779 | 780 | 781 | 782 | 783 |
| 27 | 800 | 801 | 802 | 803 | 804 | 805 | 806 | 807 | 808 | 809 | 810 | 811 | 812 | 813 | 814 | 815 |
| 28 | 832 | 833 | 834 | 835 | 836 | 837 | 838 | 839 | 840 | 841 | 842 | 843 | 844 | 845 | 846 | 847 |
| 29 | 864 | 865 | 866 | 867 | 868 | 869 | 870 | 871 | 872 | 873 | 874 | 875 | 876 | 877 | 878 | 879 |
| 30 | 896 | 897 | 898 | 899 | 900 | 901 | 902 | 903 | 904 | 905 | 906 | 907 | 908 | 909 | 910 | 911 |
| 31 | 928 | 929 | 930 | 931 | 932 | 933 | 934 | 935 | 936 | 937 | 938 | 939 | 940 | 941 | 942 | 943 |

Table 4. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_B(15:0)

| DCLK EDGE | D_B(0) | D_B(1) | D_B(2) | D_B(3) | D_B(4) | D_B(5) | D_B(6) | D_B(7) | D_B(8) | D_B(9) | D_B(10) | D_B(11) | D_B(12) | D_B(13) | D_B(14) | D_B(15) |
|-----------|-------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|
| 0 | Not Visible | | | | | | | | | | | | | | | |
| 1 | Not Visible | | | | | | | | | | | | | | | |
| 2 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| 3 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |
| 4 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 |
| 5 | 112 | 113 | 114 | 115 | 116 | 117 | 118 | 119 | 120 | 121 | 122 | 123 | 124 | 125 | 126 | 127 |
| 6 | 144 | 145 | 146 | 147 | 148 | 149 | 150 | 151 | 152 | 153 | 154 | 155 | 156 | 157 | 158 | 159 |
| 7 | 176 | 177 | 178 | 179 | 180 | 181 | 182 | 183 | 184 | 185 | 186 | 187 | 188 | 189 | 190 | 191 |
| 8 | 208 | 209 | 210 | 211 | 212 | 213 | 214 | 215 | 216 | 217 | 218 | 219 | 220 | 221 | 222 | 223 |
| 9 | 240 | 241 | 242 | 243 | 244 | 245 | 246 | 247 | 248 | 249 | 250 | 251 | 252 | 253 | 254 | 255 |
| 10 | 272 | 273 | 274 | 275 | 276 | 277 | 278 | 279 | 280 | 281 | 282 | 283 | 284 | 285 | 286 | 287 |
| 11 | 304 | 305 | 306 | 307 | 308 | 309 | 310 | 311 | 312 | 313 | 314 | 315 | 316 | 317 | 318 | 319 |
| 12 | 336 | 337 | 338 | 339 | 340 | 341 | 342 | 343 | 344 | 345 | 346 | 347 | 348 | 349 | 350 | 351 |
| 13 | 368 | 369 | 370 | 371 | 372 | 373 | 374 | 375 | 376 | 377 | 378 | 379 | 380 | 381 | 382 | 383 |
| 14 | 400 | 401 | 402 | 403 | 404 | 405 | 406 | 407 | 408 | 409 | 410 | 411 | 412 | 413 | 414 | 415 |
| 15 | 432 | 433 | 434 | 435 | 436 | 437 | 438 | 439 | 440 | 441 | 442 | 443 | 444 | 445 | 446 | 447 |
| 16 | 464 | 465 | 466 | 467 | 468 | 469 | 470 | 471 | 472 | 473 | 474 | 475 | 476 | 477 | 478 | 479 |
| 17 | 496 | 497 | 498 | 499 | 500 | 501 | 502 | 503 | 504 | 505 | 506 | 507 | 508 | 509 | 510 | 511 |
| 18 | 528 | 529 | 530 | 531 | 532 | 533 | 534 | 535 | 536 | 537 | 538 | 539 | 540 | 541 | 542 | 543 |
| 19 | 560 | 561 | 562 | 563 | 564 | 565 | 566 | 567 | 568 | 569 | 570 | 571 | 572 | 573 | 574 | 575 |
| 20 | 592 | 593 | 594 | 595 | 596 | 597 | 598 | 599 | 600 | 601 | 602 | 603 | 604 | 605 | 606 | 607 |
| 21 | 624 | 625 | 626 | 627 | 628 | 629 | 630 | 631 | 632 | 633 | 634 | 635 | 636 | 637 | 638 | 639 |
| 22 | 656 | 657 | 658 | 659 | 660 | 661 | 662 | 663 | 664 | 665 | 666 | 667 | 668 | 669 | 670 | 671 |
| 23 | 688 | 689 | 690 | 691 | 692 | 693 | 694 | 695 | 696 | 697 | 698 | 699 | 700 | 701 | 702 | 703 |
| 24 | 720 | 721 | 722 | 723 | 724 | 725 | 726 | 727 | 728 | 729 | 730 | 731 | 732 | 733 | 734 | 735 |
| 25 | 752 | 753 | 754 | 755 | 756 | 757 | 758 | 759 | 760 | 761 | 762 | 763 | 764 | 765 | 766 | 767 |
| 26 | 784 | 785 | 786 | 787 | 788 | 789 | 790 | 791 | 792 | 793 | 794 | 795 | 796 | 797 | 798 | 799 |
| 27 | 816 | 817 | 818 | 819 | 820 | 821 | 822 | 823 | 824 | 825 | 826 | 827 | 828 | 829 | 830 | 831 |
| 28 | 848 | 849 | 850 | 851 | 852 | 853 | 854 | 855 | 856 | 857 | 858 | 859 | 860 | 861 | 862 | 863 |
| 29 | 880 | 881 | 882 | 883 | 884 | 885 | 886 | 887 | 888 | 889 | 890 | 891 | 892 | 893 | 894 | 895 |
| 30 | 912 | 913 | 914 | 915 | 916 | 917 | 918 | 919 | 920 | 921 | 922 | 923 | 924 | 925 | 926 | 927 |
| 31 | 944 | 945 | 946 | 947 | 948 | 949 | 950 | 951 | 952 | 953 | 954 | 955 | 956 | 957 | 958 | 959 |

Table 5. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_C(15:0)

| DCLK EDGE | D_C(0) | D_C(1) | D_C(2) | D_C(3) | D_C(4) | D_C(5) | D_C(6) | D_C(7) | D_C(8) | D_C(9) | D_C(10) | D_C(11) | D_C(12) | D_C(13) | D_C(14) | D_C(15) |
|-----------|-------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|
| 0 | 960 | 961 | 962 | 963 | 964 | 965 | 966 | 967 | 968 | 969 | 970 | 971 | 972 | 973 | 974 | 975 |
| 1 | 992 | 993 | 994 | 995 | 996 | 997 | 998 | 999 | 1000 | 1001 | 1002 | 1003 | 1004 | 1005 | 1006 | 1007 |
| 2 | 1024 | 1025 | 1026 | 1027 | 1028 | 1029 | 1030 | 1031 | 1032 | 1033 | 1034 | 1035 | 1036 | 1037 | 1038 | 1039 |
| 3 | 1056 | 1057 | 1058 | 1059 | 1060 | 1061 | 1062 | 1063 | 1064 | 1065 | 1066 | 1067 | 1068 | 1069 | 1070 | 1071 |
| 4 | 1088 | 1089 | 1090 | 1091 | 1092 | 1093 | 1094 | 1095 | 1096 | 1097 | 1098 | 1099 | 1100 | 1101 | 1102 | 1103 |
| 5 | 1120 | 1121 | 1122 | 1123 | 1124 | 1125 | 1126 | 1127 | 1128 | 1129 | 1130 | 1131 | 1132 | 1133 | 1134 | 1135 |
| 6 | 1152 | 1153 | 1154 | 1155 | 1156 | 1157 | 1158 | 1159 | 1160 | 1161 | 1162 | 1163 | 1164 | 1165 | 1166 | 1167 |
| 7 | 1184 | 1185 | 1186 | 1187 | 1188 | 1189 | 1190 | 1191 | 1192 | 1193 | 1194 | 1195 | 1196 | 1197 | 1198 | 1199 |
| 8 | 1216 | 1217 | 1218 | 1219 | 1220 | 1221 | 1222 | 1223 | 1224 | 1225 | 1226 | 1227 | 1228 | 1229 | 1230 | 1231 |
| 9 | 1248 | 1249 | 1250 | 1251 | 1252 | 1253 | 1254 | 1255 | 1256 | 1257 | 1258 | 1259 | 1260 | 1261 | 1262 | 1263 |
| 10 | 1280 | 1281 | 1282 | 1283 | 1284 | 1285 | 1286 | 1287 | 1288 | 1289 | 1290 | 1291 | 1292 | 1293 | 1294 | 1295 |
| 11 | 1312 | 1313 | 1314 | 1315 | 1316 | 1317 | 1318 | 1319 | 1320 | 1321 | 1322 | 1323 | 1324 | 1325 | 1326 | 1327 |
| 12 | 1344 | 1345 | 1346 | 1347 | 1348 | 1349 | 1350 | 1351 | 1352 | 1353 | 1354 | 1355 | 1356 | 1357 | 1358 | 1359 |
| 13 | 1376 | 1377 | 1378 | 1379 | 1380 | 1381 | 1382 | 1383 | 1384 | 1385 | 1386 | 1387 | 1388 | 1389 | 1390 | 1391 |
| 14 | 1408 | 1409 | 1410 | 1411 | 1412 | 1413 | 1414 | 1415 | 1416 | 1417 | 1418 | 1419 | 1420 | 1421 | 1422 | 1423 |
| 15 | 1440 | 1441 | 1442 | 1443 | 1444 | 1445 | 1446 | 1447 | 1448 | 1449 | 1450 | 1451 | 1452 | 1453 | 1454 | 1455 |
| 16 | 1472 | 1473 | 1474 | 1475 | 1476 | 1477 | 1478 | 1479 | 1480 | 1481 | 1482 | 1483 | 1484 | 1485 | 1486 | 1487 |
| 17 | 1504 | 1505 | 1506 | 1507 | 1508 | 1509 | 1510 | 1511 | 1512 | 1513 | 1514 | 1515 | 1516 | 1517 | 1518 | 1519 |
| 18 | 1536 | 1537 | 1538 | 1539 | 1540 | 1541 | 1542 | 1543 | 1544 | 1545 | 1546 | 1547 | 1548 | 1549 | 1550 | 1551 |
| 19 | 1568 | 1569 | 1570 | 1571 | 1572 | 1573 | 1574 | 1575 | 1576 | 1577 | 1578 | 1579 | 1580 | 1581 | 1582 | 1583 |
| 20 | 1600 | 1601 | 1602 | 1603 | 1604 | 1605 | 1606 | 1607 | 1608 | 1609 | 1610 | 1611 | 1612 | 1613 | 1614 | 1615 |
| 21 | 1632 | 1633 | 1634 | 1635 | 1636 | 1637 | 1638 | 1639 | 1640 | 1641 | 1642 | 1643 | 1644 | 1645 | 1646 | 1647 |
| 22 | 1664 | 1665 | 1666 | 1667 | 1668 | 1669 | 1670 | 1671 | 1672 | 1673 | 1674 | 1675 | 1676 | 1677 | 1678 | 1679 |
| 23 | 1696 | 1697 | 1698 | 1699 | 1700 | 1701 | 1702 | 1703 | 1704 | 1705 | 1706 | 1707 | 1708 | 1709 | 1710 | 1711 |
| 24 | 1728 | 1729 | 1730 | 1731 | 1732 | 1733 | 1734 | 1735 | 1736 | 1737 | 1738 | 1739 | 1740 | 1741 | 1742 | 1743 |
| 25 | 1760 | 1761 | 1762 | 1763 | 1764 | 1765 | 1766 | 1767 | 1768 | 1769 | 1770 | 1771 | 1772 | 1773 | 1774 | 1775 |
| 26 | 1792 | 1793 | 1794 | 1795 | 1796 | 1797 | 1798 | 1799 | 1800 | 1801 | 1802 | 1803 | 1804 | 1805 | 1806 | 1807 |
| 27 | 1824 | 1825 | 1826 | 1827 | 1828 | 1829 | 1830 | 1831 | 1832 | 1833 | 1834 | 1835 | 1836 | 1837 | 1838 | 1839 |
| 28 | 1856 | 1857 | 1858 | 1859 | 1860 | 1861 | 1862 | 1863 | 1864 | 1865 | 1866 | 1867 | 1868 | 1869 | 1870 | 1871 |
| 29 | 1888 | 1889 | 1890 | 1891 | 1892 | 1893 | 1894 | 1895 | 1896 | 1897 | 1898 | 1899 | 1900 | 1901 | 1902 | 1903 |
| 30 | Not Visible | | | | | | | | | | | | | | | |
| 31 | | | | | | | | | | | | | | | | |

Table 6. DLP9500 / DLP9500UV 2XLVDS DMD Data Pixel Mapping D_D(15:0)

| DCLK EDGE | D_D(0) | D_D(1) | D_D(2) | D_D(3) | D_D(4) | D_D(5) | D_D(6) | D_D(7) | D_D(8) | D_D(9) | D_D(10) | D_D(11) | D_D(12) | D_D(13) | D_D(14) | D_D(15) |
|-----------|-------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|
| 0 | 976 | 977 | 978 | 979 | 980 | 981 | 982 | 983 | 984 | 985 | 986 | 987 | 988 | 989 | 990 | 991 |
| 1 | 1008 | 1009 | 1010 | 1011 | 1012 | 1013 | 1014 | 1015 | 1016 | 1017 | 1018 | 1019 | 1020 | 1021 | 1022 | 1023 |
| 2 | 1040 | 1041 | 1042 | 1043 | 1044 | 1045 | 1046 | 1047 | 1048 | 1049 | 1050 | 1051 | 1052 | 1053 | 1054 | 1055 |
| 3 | 1072 | 1073 | 1074 | 1075 | 1076 | 1077 | 1078 | 1079 | 1080 | 1081 | 1082 | 1083 | 1084 | 1085 | 1086 | 1087 |
| 4 | 1104 | 1105 | 1106 | 1107 | 1108 | 1109 | 1110 | 1111 | 1112 | 1113 | 1114 | 1115 | 1116 | 1117 | 1118 | 1119 |
| 5 | 1136 | 1137 | 1138 | 1139 | 1140 | 1141 | 1142 | 1143 | 1144 | 1145 | 1146 | 1147 | 1148 | 1149 | 1150 | 1151 |
| 6 | 1168 | 1169 | 1170 | 1171 | 1172 | 1173 | 1174 | 1175 | 1176 | 1177 | 1178 | 1179 | 1180 | 1181 | 1182 | 1183 |
| 7 | 1200 | 1201 | 1202 | 1203 | 1204 | 1205 | 1206 | 1207 | 1208 | 1209 | 1210 | 1211 | 1212 | 1213 | 1214 | 1215 |
| 8 | 1232 | 1233 | 1234 | 1235 | 1236 | 1237 | 1238 | 1239 | 1240 | 1241 | 1242 | 1243 | 1244 | 1245 | 1246 | 1247 |
| 9 | 1264 | 1265 | 1266 | 1267 | 1268 | 1269 | 1270 | 1271 | 1272 | 1273 | 1274 | 1275 | 1276 | 1277 | 1278 | 1279 |
| 10 | 1296 | 1297 | 1298 | 1299 | 1300 | 1301 | 1302 | 1303 | 1304 | 1305 | 1306 | 1307 | 1308 | 1309 | 1310 | 1311 |
| 11 | 1328 | 1329 | 1330 | 1331 | 1332 | 1333 | 1334 | 1335 | 1336 | 1337 | 1338 | 1339 | 1340 | 1341 | 1342 | 1343 |
| 12 | 1360 | 1361 | 1362 | 1363 | 1364 | 1365 | 1366 | 1367 | 1368 | 1369 | 1370 | 1371 | 1372 | 1373 | 1374 | 1375 |
| 13 | 1392 | 1393 | 1394 | 1395 | 1396 | 1397 | 1398 | 1399 | 1400 | 1401 | 1402 | 1403 | 1404 | 1405 | 1406 | 1407 |
| 14 | 1424 | 1425 | 1426 | 1427 | 1428 | 1429 | 1430 | 1431 | 1432 | 1433 | 1434 | 1435 | 1436 | 1437 | 1438 | 1439 |
| 15 | 1456 | 1457 | 1458 | 1459 | 1460 | 1461 | 1462 | 1463 | 1464 | 1465 | 1466 | 1467 | 1468 | 1469 | 1470 | 1471 |
| 16 | 1488 | 1489 | 1490 | 1491 | 1492 | 1493 | 1494 | 1495 | 1496 | 1497 | 1498 | 1499 | 1500 | 1501 | 1502 | 1503 |
| 17 | 1520 | 1521 | 1522 | 1523 | 1524 | 1525 | 1526 | 1527 | 1528 | 1529 | 1530 | 1531 | 1532 | 1533 | 1534 | 1535 |
| 18 | 1552 | 1553 | 1554 | 1555 | 1556 | 1557 | 1558 | 1559 | 1560 | 1561 | 1562 | 1563 | 1564 | 1565 | 1566 | 1567 |
| 19 | 1584 | 1585 | 1586 | 1587 | 1588 | 1589 | 1590 | 1591 | 1592 | 1593 | 1594 | 1595 | 1596 | 1597 | 1598 | 1599 |
| 20 | 1616 | 1617 | 1618 | 1619 | 1620 | 1621 | 1622 | 1623 | 1624 | 1625 | 1626 | 1627 | 1628 | 1629 | 1630 | 1631 |
| 21 | 1648 | 1649 | 1650 | 1651 | 1652 | 1653 | 1654 | 1655 | 1656 | 1657 | 1658 | 1659 | 1660 | 1661 | 1662 | 1663 |
| 22 | 1680 | 1681 | 1682 | 1683 | 1684 | 1685 | 1686 | 1687 | 1688 | 1689 | 1690 | 1691 | 1692 | 1693 | 1694 | 1695 |
| 23 | 1712 | 1713 | 1714 | 1715 | 1716 | 1717 | 1718 | 1719 | 1720 | 1721 | 1722 | 1723 | 1724 | 1725 | 1726 | 1727 |
| 24 | 1744 | 1745 | 1746 | 1747 | 1748 | 1749 | 1750 | 1751 | 1752 | 1753 | 1754 | 1755 | 1756 | 1757 | 1758 | 1759 |
| 25 | 1776 | 1777 | 1778 | 1779 | 1780 | 1781 | 1782 | 1783 | 1784 | 1785 | 1786 | 1787 | 1788 | 1789 | 1790 | 1791 |
| 26 | 1808 | 1809 | 1810 | 1811 | 1812 | 1813 | 1814 | 1815 | 1816 | 1817 | 1818 | 1819 | 1820 | 1821 | 1822 | 1823 |
| 27 | 1840 | 1841 | 1842 | 1843 | 1844 | 1845 | 1846 | 1847 | 1848 | 1849 | 1850 | 1851 | 1852 | 1853 | 1854 | 1855 |
| 28 | 1872 | 1873 | 1874 | 1875 | 1876 | 1877 | 1878 | 1879 | 1880 | 1881 | 1882 | 1883 | 1884 | 1885 | 1886 | 1887 |
| 29 | 1904 | 1905 | 1906 | 1907 | 1908 | 1909 | 1910 | 1911 | 1912 | 1913 | 1914 | 1915 | 1916 | 1917 | 1918 | 1919 |
| 30 | Not Visible | | | | | | | | | | | | | | | |
| 31 | | | | | | | | | | | | | | | | |

8.3.1.10 DLP7000 and DLP7000UV Input Data Bus

Figure 7 details one row cycle of input data formatting for the DLP7000 and DLP7000UV DMDs. For brevity, only two data bits of both 16 bit data bus (A/B) signals are shown, but there is enough information presented to allow extrapolation to data bus signals not shown.

Table 7 and Table 8 show how each pixel of the DLP7000 and DLP7000UV DMDs maps to individual data bus inputs and input clock edges within each row load operation.

NOTE

In the following charts, for readability purposes input buses DIN_A, DIN_B are abbreviated as D_A, D_B. DCLKIN has been shortened to DCLK.

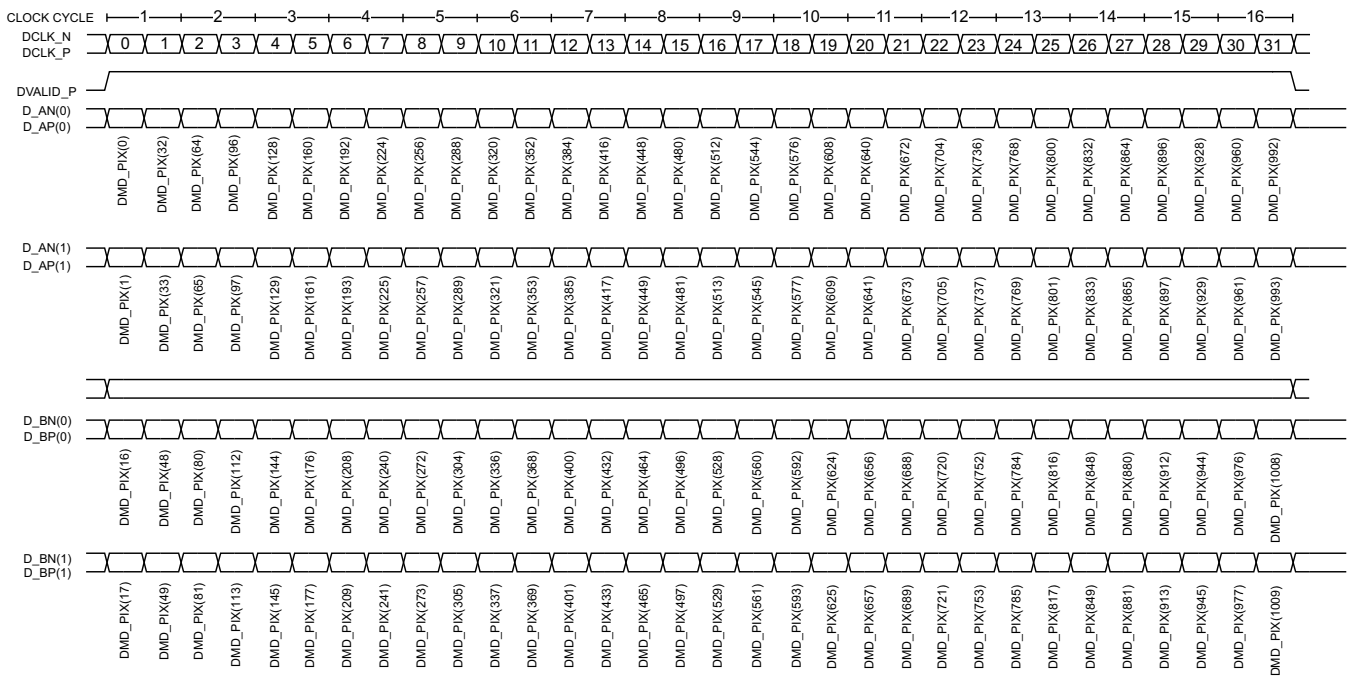


Figure 7. DLP7000 / DLP7000UV 2XLVDS DMD Input Data Bus

Table 7. DLP7000 / DLP7000UV 2XLVDS DMD Data Pixel Mapping D_A(15:0)

| DCLK EDGE | D_A(0) | D_A(1) | D_A(2) | D_A(3) | D_A(4) | D_A(5) | D_A(6) | D_A(7) | D_A(8) | D_A(9) | D_A(10) | D_A(11) | D_A(12) | D_A(13) | D_A(14) | D_A(15) |
|-----------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|
| 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 1 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| 2 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 |
| 3 | 96 | 97 | 98 | 99 | 100 | 101 | 102 | 103 | 104 | 105 | 106 | 107 | 108 | 109 | 110 | 111 |
| 4 | 128 | 129 | 130 | 131 | 132 | 133 | 134 | 135 | 136 | 137 | 138 | 139 | 140 | 141 | 142 | 143 |
| 5 | 160 | 161 | 162 | 163 | 164 | 165 | 166 | 167 | 168 | 169 | 170 | 171 | 172 | 173 | 174 | 175 |
| 6 | 192 | 193 | 194 | 195 | 196 | 197 | 198 | 199 | 200 | 201 | 202 | 203 | 204 | 205 | 206 | 207 |
| 7 | 224 | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 232 | 233 | 234 | 235 | 236 | 237 | 238 | 239 |
| 8 | 256 | 257 | 258 | 259 | 260 | 261 | 262 | 263 | 264 | 265 | 266 | 267 | 268 | 269 | 270 | 271 |
| 9 | 288 | 289 | 290 | 291 | 292 | 293 | 294 | 295 | 296 | 297 | 298 | 299 | 300 | 301 | 302 | 303 |
| 10 | 320 | 321 | 322 | 323 | 324 | 325 | 326 | 327 | 328 | 329 | 330 | 331 | 332 | 333 | 334 | 335 |
| 11 | 352 | 353 | 354 | 355 | 356 | 357 | 358 | 359 | 360 | 361 | 362 | 363 | 364 | 365 | 366 | 367 |
| 12 | 384 | 385 | 386 | 387 | 388 | 389 | 390 | 391 | 392 | 393 | 394 | 395 | 396 | 397 | 398 | 399 |
| 13 | 416 | 417 | 418 | 419 | 420 | 421 | 422 | 423 | 424 | 425 | 426 | 427 | 428 | 429 | 430 | 431 |
| 14 | 448 | 449 | 450 | 451 | 452 | 453 | 454 | 455 | 456 | 457 | 458 | 459 | 460 | 461 | 462 | 463 |
| 15 | 480 | 481 | 482 | 483 | 484 | 485 | 486 | 487 | 488 | 489 | 490 | 491 | 492 | 493 | 494 | 495 |
| 16 | 512 | 513 | 514 | 515 | 516 | 517 | 518 | 519 | 520 | 521 | 522 | 523 | 524 | 525 | 526 | 527 |
| 17 | 544 | 545 | 546 | 547 | 548 | 549 | 550 | 551 | 552 | 553 | 554 | 555 | 556 | 557 | 558 | 559 |
| 18 | 576 | 577 | 578 | 579 | 580 | 581 | 582 | 583 | 584 | 585 | 586 | 587 | 588 | 589 | 590 | 591 |
| 19 | 608 | 609 | 610 | 611 | 612 | 613 | 614 | 615 | 616 | 617 | 618 | 619 | 620 | 621 | 622 | 623 |
| 20 | 640 | 641 | 642 | 643 | 644 | 645 | 646 | 647 | 648 | 649 | 650 | 651 | 652 | 653 | 654 | 655 |
| 21 | 672 | 673 | 674 | 675 | 676 | 677 | 678 | 679 | 680 | 681 | 682 | 683 | 684 | 685 | 686 | 687 |
| 22 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | 712 | 713 | 714 | 715 | 716 | 717 | 718 | 719 |
| 23 | 736 | 737 | 738 | 739 | 740 | 741 | 742 | 743 | 744 | 745 | 746 | 747 | 748 | 749 | 750 | 751 |
| 24 | 768 | 769 | 770 | 771 | 772 | 773 | 774 | 775 | 776 | 777 | 778 | 779 | 780 | 781 | 782 | 783 |
| 25 | 800 | 801 | 802 | 803 | 804 | 805 | 806 | 807 | 808 | 809 | 810 | 811 | 812 | 813 | 814 | 815 |
| 26 | 832 | 833 | 834 | 835 | 836 | 837 | 838 | 839 | 840 | 841 | 842 | 843 | 844 | 845 | 846 | 847 |
| 27 | 864 | 865 | 866 | 867 | 868 | 869 | 870 | 871 | 872 | 873 | 874 | 875 | 876 | 877 | 878 | 879 |
| 28 | 896 | 897 | 898 | 899 | 900 | 901 | 902 | 903 | 904 | 905 | 906 | 907 | 908 | 909 | 910 | 911 |
| 29 | 928 | 929 | 930 | 931 | 932 | 933 | 934 | 935 | 936 | 937 | 938 | 939 | 940 | 941 | 942 | 943 |
| 30 | 960 | 961 | 962 | 963 | 964 | 965 | 966 | 967 | 968 | 969 | 970 | 971 | 972 | 973 | 974 | 975 |
| 31 | 992 | 993 | 994 | 995 | 996 | 997 | 998 | 999 | 1000 | 1001 | 1002 | 1003 | 1004 | 1005 | 1006 | 1007 |

Table 8. DLP7000 / DLP7000UV 2XLVDS DMD Data Pixel Mapping D_B(15:0)

| DCLK EDGE | D_B(0) | D_B(1) | D_B(2) | D_B(3) | D_B(4) | D_B(5) | D_B(6) | D_B(7) | D_B(8) | D_B(9) | D_B(10) | D_B(11) | D_B(12) | D_B(13) | D_B(14) | D_B(15) |
|-----------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|
| 0 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| 1 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |
| 2 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | 88 | 89 | 90 | 91 | 92 | 93 | 94 | 95 |
| 3 | 112 | 113 | 114 | 115 | 116 | 117 | 118 | 119 | 120 | 121 | 122 | 123 | 124 | 125 | 126 | 127 |
| 4 | 144 | 145 | 146 | 147 | 148 | 149 | 150 | 151 | 152 | 153 | 154 | 155 | 156 | 157 | 158 | 159 |
| 5 | 176 | 177 | 178 | 179 | 180 | 181 | 182 | 183 | 184 | 185 | 186 | 187 | 188 | 189 | 190 | 191 |
| 6 | 208 | 209 | 210 | 211 | 212 | 213 | 214 | 215 | 216 | 217 | 218 | 219 | 220 | 221 | 222 | 223 |
| 7 | 240 | 241 | 242 | 243 | 244 | 245 | 246 | 247 | 248 | 249 | 250 | 251 | 252 | 253 | 254 | 255 |
| 8 | 272 | 273 | 274 | 275 | 276 | 277 | 278 | 279 | 280 | 281 | 282 | 283 | 284 | 285 | 286 | 287 |
| 9 | 304 | 305 | 306 | 307 | 308 | 309 | 310 | 311 | 312 | 313 | 314 | 315 | 316 | 317 | 318 | 319 |
| 10 | 336 | 337 | 338 | 339 | 340 | 341 | 342 | 343 | 344 | 345 | 346 | 347 | 348 | 349 | 350 | 351 |
| 11 | 368 | 369 | 370 | 371 | 372 | 373 | 374 | 375 | 376 | 377 | 378 | 379 | 380 | 381 | 382 | 383 |
| 12 | 400 | 401 | 402 | 403 | 404 | 405 | 406 | 407 | 408 | 409 | 410 | 411 | 412 | 413 | 414 | 415 |
| 13 | 432 | 433 | 434 | 435 | 436 | 437 | 438 | 439 | 440 | 441 | 442 | 443 | 444 | 445 | 446 | 447 |
| 14 | 464 | 465 | 466 | 467 | 468 | 469 | 470 | 471 | 472 | 473 | 474 | 475 | 476 | 477 | 478 | 479 |
| 15 | 496 | 497 | 498 | 499 | 500 | 501 | 502 | 503 | 504 | 505 | 506 | 507 | 508 | 509 | 510 | 511 |
| 16 | 528 | 529 | 530 | 531 | 532 | 533 | 534 | 535 | 536 | 537 | 538 | 539 | 540 | 541 | 542 | 543 |
| 17 | 560 | 561 | 562 | 563 | 564 | 565 | 566 | 567 | 568 | 569 | 570 | 571 | 572 | 573 | 574 | 575 |
| 18 | 592 | 593 | 594 | 595 | 596 | 597 | 598 | 599 | 600 | 601 | 602 | 603 | 604 | 605 | 606 | 607 |
| 19 | 624 | 625 | 626 | 627 | 628 | 629 | 630 | 631 | 632 | 633 | 634 | 635 | 636 | 637 | 638 | 639 |
| 20 | 656 | 657 | 658 | 659 | 660 | 661 | 662 | 663 | 664 | 665 | 666 | 667 | 668 | 669 | 670 | 671 |
| 21 | 688 | 689 | 690 | 691 | 692 | 693 | 694 | 695 | 696 | 697 | 698 | 699 | 700 | 701 | 702 | 703 |
| 22 | 720 | 721 | 722 | 723 | 724 | 725 | 726 | 727 | 728 | 729 | 730 | 731 | 732 | 733 | 734 | 735 |
| 23 | 752 | 753 | 754 | 755 | 756 | 757 | 758 | 759 | 760 | 761 | 762 | 763 | 764 | 765 | 766 | 767 |
| 24 | 784 | 785 | 786 | 787 | 788 | 789 | 790 | 791 | 792 | 793 | 794 | 795 | 796 | 797 | 798 | 799 |
| 25 | 816 | 817 | 818 | 819 | 820 | 821 | 822 | 823 | 824 | 825 | 826 | 827 | 828 | 829 | 830 | 831 |
| 26 | 848 | 849 | 850 | 851 | 852 | 853 | 854 | 855 | 856 | 857 | 858 | 859 | 860 | 861 | 862 | 863 |
| 27 | 880 | 881 | 882 | 883 | 884 | 885 | 886 | 887 | 888 | 889 | 890 | 891 | 892 | 893 | 894 | 895 |
| 28 | 912 | 913 | 914 | 915 | 916 | 917 | 918 | 919 | 920 | 921 | 922 | 923 | 924 | 925 | 926 | 927 |
| 29 | 944 | 945 | 946 | 947 | 948 | 949 | 950 | 951 | 952 | 953 | 954 | 955 | 956 | 957 | 958 | 959 |
| 30 | 976 | 977 | 978 | 979 | 980 | 981 | 982 | 983 | 984 | 985 | 986 | 987 | 988 | 989 | 990 | 991 |
| 31 | 1008 | 1009 | 1010 | 1011 | 1012 | 1013 | 1014 | 1015 | 1016 | 1017 | 1018 | 1019 | 1020 | 1021 | 1022 | 1023 |

8.3.1.11 DLP650LNIR Input Data Bus

Figure 8 details one row cycle of input data formatting for the DLP650LNIR DMD. For brevity, only two data bits of both 8 bit data bus (A/B) signals are shown, but there is enough information presented to allow extrapolation to data bus signals not shown.

Table 9 and Table 10 show how each pixel of the DLP650LNIR DMD maps to individual data bus inputs and input clock edges within each row load operation.

NOTE

In the following charts, for readability purposes input buses DIN_A, DIN_B are abbreviated as D_A, D_B. DCLKIN has been shortened to DCLK.

Since showing the entire 40 clock row cycle would make this chart unreadable, the chart has been broken in the middle. However, there is enough information available to allow extrapolation of the missing data.

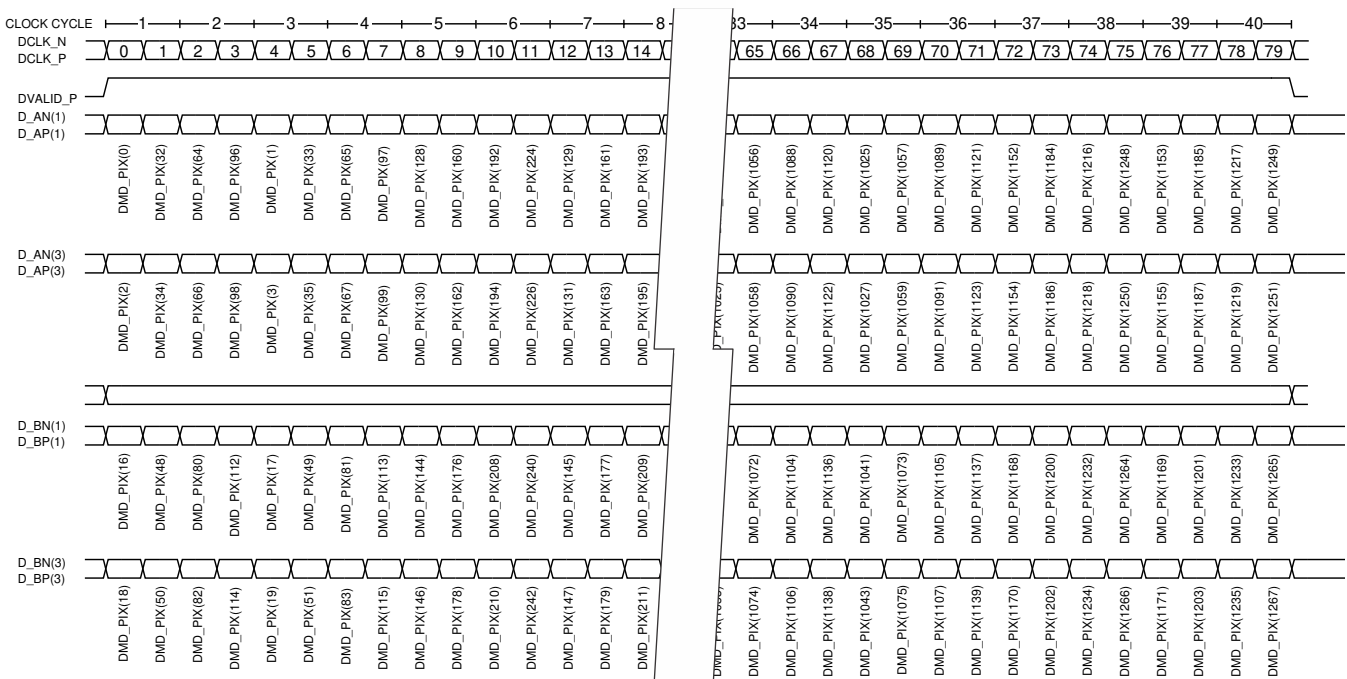


Figure 8. DLP650LNIR 2xLVDS DMD Input Data Bus

Table 9. DLP650LNIR 2xLVDS DMD Data Pixel Mapping D_A(15,13,11,9,7,5,3,1)

| DCLK EDGE | D_A(1) | D_A(3) | D_A(5) | D_A(7) | D_A(9) | D_A(11) | D_A(13) | D_A(15) |
|-----------|--------|--------|--------|--------|--------|---------|---------|---------|
| 0 | 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 |
| 1 | 32 | 34 | 36 | 38 | 40 | 42 | 44 | 46 |
| 2 | 64 | 66 | 68 | 70 | 72 | 74 | 76 | 78 |
| 3 | 96 | 98 | 100 | 102 | 104 | 106 | 108 | 110 |
| 4 | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 |
| 5 | 33 | 35 | 37 | 39 | 41 | 43 | 45 | 47 |
| 6 | 65 | 67 | 69 | 71 | 73 | 75 | 77 | 79 |
| 7 | 97 | 99 | 101 | 103 | 105 | 107 | 109 | 111 |
| 8 | 128 | 130 | 132 | 134 | 136 | 138 | 140 | 142 |
| 9 | 160 | 162 | 164 | 166 | 168 | 170 | 172 | 174 |
| 10 | 192 | 194 | 196 | 198 | 200 | 202 | 204 | 206 |
| 11 | 224 | 226 | 228 | 230 | 232 | 234 | 236 | 238 |
| 12 | 129 | 131 | 133 | 135 | 137 | 139 | 141 | 143 |
| 13 | 161 | 163 | 165 | 167 | 169 | 171 | 173 | 175 |
| 14 | 193 | 195 | 197 | 199 | 201 | 203 | 205 | 207 |
| 15 | 225 | 227 | 229 | 231 | 233 | 235 | 237 | 239 |
| 16 | 256 | 258 | 260 | 262 | 264 | 266 | 268 | 270 |
| 17 | 288 | 290 | 292 | 294 | 296 | 298 | 300 | 302 |
| 18 | 320 | 322 | 324 | 326 | 328 | 330 | 332 | 334 |
| 19 | 352 | 354 | 356 | 358 | 360 | 362 | 364 | 366 |
| 20 | 257 | 259 | 261 | 263 | 265 | 267 | 269 | 271 |
| 21 | 289 | 291 | 293 | 295 | 297 | 299 | 301 | 303 |
| 22 | 321 | 323 | 325 | 327 | 329 | 331 | 333 | 335 |
| 23 | 353 | 355 | 357 | 359 | 361 | 363 | 365 | 367 |
| 24 | 384 | 386 | 388 | 390 | 392 | 394 | 396 | 398 |
| 25 | 416 | 418 | 420 | 422 | 424 | 426 | 428 | 430 |
| 26 | 448 | 450 | 452 | 454 | 456 | 458 | 460 | 462 |
| 27 | 480 | 482 | 484 | 486 | 488 | 490 | 492 | 494 |
| 28 | 385 | 387 | 389 | 391 | 393 | 395 | 397 | 399 |
| 29 | 417 | 419 | 421 | 423 | 425 | 427 | 429 | 431 |
| 30 | 449 | 451 | 453 | 455 | 457 | 459 | 461 | 463 |
| 31 | 481 | 483 | 485 | 487 | 489 | 491 | 493 | 495 |
| 32 | 512 | 514 | 516 | 518 | 520 | 522 | 524 | 526 |
| 33 | 544 | 546 | 548 | 550 | 552 | 554 | 556 | 558 |
| 34 | 576 | 578 | 580 | 582 | 584 | 586 | 588 | 590 |
| 35 | 608 | 610 | 612 | 614 | 616 | 618 | 620 | 622 |
| 36 | 513 | 515 | 517 | 519 | 521 | 523 | 525 | 527 |
| 37 | 545 | 547 | 549 | 551 | 553 | 555 | 557 | 559 |
| 38 | 577 | 579 | 581 | 583 | 585 | 587 | 589 | 591 |
| 39 | 609 | 611 | 613 | 615 | 617 | 619 | 621 | 623 |
| 40 | 640 | 642 | 644 | 646 | 648 | 650 | 652 | 654 |
| 41 | 672 | 674 | 676 | 678 | 680 | 682 | 684 | 686 |
| 42 | 704 | 706 | 708 | 710 | 712 | 714 | 716 | 718 |
| 43 | 736 | 738 | 740 | 742 | 744 | 746 | 748 | 750 |
| 44 | 641 | 643 | 645 | 647 | 649 | 651 | 653 | 655 |
| 45 | 673 | 675 | 677 | 679 | 681 | 683 | 685 | 687 |
| 46 | 705 | 707 | 709 | 711 | 713 | 715 | 717 | 719 |
| 47 | 737 | 739 | 741 | 743 | 745 | 747 | 749 | 751 |
| 48 | 768 | 770 | 772 | 774 | 776 | 778 | 780 | 782 |
| 49 | 800 | 802 | 804 | 806 | 808 | 810 | 812 | 814 |
| 50 | 832 | 834 | 836 | 838 | 840 | 842 | 844 | 846 |
| 51 | 864 | 866 | 868 | 870 | 872 | 874 | 876 | 878 |
| 52 | 769 | 771 | 773 | 775 | 777 | 779 | 781 | 783 |
| 53 | 801 | 803 | 805 | 807 | 809 | 811 | 813 | 815 |
| 54 | 833 | 835 | 837 | 839 | 841 | 843 | 845 | 847 |
| 55 | 865 | 867 | 869 | 871 | 873 | 875 | 877 | 879 |

Table 9. DLP650LNIR 2xLVDS DMD Data Pixel Mapping D_A(15,13,11,9,7,5,3,1) (continued)

| DCCLK EDGE | D_A(1) | D_A(3) | D_A(5) | D_A(7) | D_A(9) | D_A(11) | D_A(13) | D_A(15) |
|------------|--------|--------|--------|--------|--------|---------|---------|---------|
| 56 | 896 | 898 | 900 | 902 | 904 | 906 | 908 | 910 |
| 57 | 928 | 930 | 832 | 934 | 936 | 938 | 940 | 942 |
| 58 | 960 | 962 | 964 | 966 | 968 | 970 | 972 | 974 |
| 59 | 992 | 994 | 996 | 998 | 1000 | 1002 | 1004 | 1006 |
| 60 | 897 | 899 | 901 | 903 | 905 | 907 | 909 | 911 |
| 61 | 929 | 931 | 933 | 935 | 937 | 939 | 941 | 943 |
| 62 | 961 | 963 | 965 | 967 | 969 | 971 | 973 | 975 |
| 63 | 993 | 995 | 997 | 999 | 1001 | 1003 | 1005 | 1007 |
| 64 | 1024 | 1026 | 1028 | 1030 | 1032 | 1034 | 1036 | 1038 |
| 65 | 1056 | 1058 | 1060 | 1062 | 1064 | 1066 | 1068 | 1070 |
| 66 | 1088 | 1090 | 1092 | 1094 | 1096 | 1098 | 1100 | 1102 |
| 67 | 1120 | 1122 | 1124 | 1126 | 1128 | 1130 | 1132 | 1134 |
| 68 | 1025 | 1027 | 1029 | 1031 | 1033 | 1035 | 1037 | 1039 |
| 69 | 1057 | 1059 | 1061 | 1063 | 1065 | 1067 | 1069 | 1071 |
| 70 | 1089 | 1091 | 1093 | 1095 | 1097 | 1099 | 1101 | 1103 |
| 71 | 1121 | 1123 | 1125 | 1127 | 1129 | 1131 | 1133 | 1135 |
| 72 | 1152 | 1154 | 1156 | 1158 | 1160 | 1162 | 1164 | 1166 |
| 73 | 1184 | 1186 | 1188 | 1190 | 1192 | 1194 | 1196 | 1198 |
| 74 | 1216 | 1218 | 1220 | 1222 | 1224 | 1226 | 1228 | 1230 |
| 75 | 1248 | 1250 | 1252 | 1254 | 1256 | 1258 | 1260 | 1262 |
| 76 | 1153 | 1155 | 1157 | 1159 | 1161 | 1163 | 1165 | 1167 |
| 77 | 1185 | 1187 | 1189 | 1191 | 1193 | 1195 | 1197 | 1199 |
| 78 | 1217 | 1219 | 1221 | 1223 | 1225 | 1227 | 1229 | 1231 |
| 79 | 1249 | 1251 | 1253 | 1255 | 1257 | 1259 | 1261 | 1263 |

Table 10. DLP650LNIR 2xLVDS DMD Data Pixel Mapping D_B(15,13,11,9,7,5,3,1)

| DCLK EDGE | D_B(1) | D_B(3) | D_B(5) | D_B(7) | D_B(9) | D_B(11) | D_B(13) | D_B(15) |
|-----------|--------|--------|--------|--------|--------|---------|---------|---------|
| 0 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 |
| 1 | 48 | 50 | 52 | 54 | 56 | 58 | 60 | 62 |
| 2 | 80 | 82 | 84 | 86 | 88 | 90 | 92 | 94 |
| 3 | 112 | 114 | 116 | 118 | 120 | 122 | 124 | 126 |
| 4 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | 31 |
| 5 | 49 | 51 | 53 | 55 | 57 | 59 | 61 | 63 |
| 6 | 81 | 83 | 85 | 87 | 89 | 91 | 93 | 95 |
| 7 | 113 | 115 | 117 | 119 | 121 | 123 | 125 | 127 |
| 8 | 144 | 146 | 148 | 150 | 152 | 154 | 156 | 158 |
| 9 | 176 | 178 | 180 | 182 | 184 | 186 | 188 | 190 |
| 10 | 208 | 210 | 212 | 214 | 216 | 218 | 220 | 222 |
| 11 | 240 | 242 | 244 | 246 | 248 | 250 | 252 | 254 |
| 12 | 145 | 147 | 149 | 151 | 153 | 155 | 157 | 159 |
| 13 | 177 | 179 | 181 | 183 | 185 | 187 | 189 | 191 |
| 14 | 209 | 211 | 213 | 215 | 217 | 219 | 221 | 223 |
| 15 | 241 | 243 | 245 | 247 | 249 | 251 | 253 | 255 |
| 16 | 272 | 274 | 276 | 278 | 280 | 282 | 284 | 286 |
| 17 | 304 | 306 | 308 | 310 | 312 | 314 | 316 | 318 |
| 18 | 336 | 338 | 340 | 342 | 344 | 346 | 348 | 350 |
| 19 | 368 | 370 | 372 | 374 | 376 | 378 | 380 | 382 |
| 20 | 273 | 275 | 277 | 279 | 281 | 283 | 285 | 287 |
| 21 | 305 | 307 | 309 | 311 | 313 | 315 | 317 | 319 |
| 22 | 337 | 339 | 341 | 343 | 345 | 347 | 349 | 351 |
| 23 | 369 | 371 | 373 | 375 | 377 | 379 | 381 | 383 |
| 24 | 400 | 402 | 404 | 406 | 408 | 410 | 412 | 414 |
| 25 | 432 | 434 | 436 | 438 | 440 | 442 | 444 | 446 |
| 26 | 464 | 466 | 468 | 470 | 472 | 474 | 476 | 478 |
| 27 | 496 | 498 | 500 | 502 | 504 | 506 | 508 | 510 |
| 28 | 401 | 403 | 405 | 407 | 409 | 411 | 413 | 415 |
| 29 | 433 | 435 | 437 | 439 | 441 | 443 | 445 | 447 |
| 30 | 465 | 467 | 469 | 471 | 473 | 475 | 477 | 479 |
| 31 | 497 | 499 | 501 | 503 | 505 | 507 | 509 | 511 |
| 32 | 528 | 530 | 532 | 534 | 536 | 538 | 540 | 542 |
| 33 | 560 | 562 | 564 | 566 | 568 | 570 | 572 | 574 |
| 34 | 592 | 594 | 596 | 598 | 600 | 602 | 604 | 606 |
| 35 | 624 | 626 | 628 | 630 | 632 | 634 | 636 | 638 |
| 36 | 529 | 531 | 533 | 535 | 537 | 539 | 541 | 543 |
| 37 | 561 | 563 | 565 | 567 | 569 | 571 | 573 | 575 |
| 38 | 593 | 595 | 597 | 599 | 601 | 603 | 605 | 607 |
| 39 | 625 | 627 | 629 | 631 | 633 | 635 | 637 | 639 |
| 40 | 656 | 658 | 660 | 662 | 664 | 666 | 668 | 670 |
| 41 | 688 | 690 | 692 | 694 | 696 | 698 | 700 | 702 |
| 42 | 720 | 722 | 724 | 726 | 728 | 730 | 732 | 734 |
| 43 | 752 | 754 | 756 | 758 | 760 | 762 | 764 | 766 |
| 44 | 657 | 659 | 661 | 663 | 665 | 667 | 669 | 671 |
| 45 | 689 | 691 | 693 | 695 | 697 | 699 | 701 | 703 |
| 46 | 721 | 723 | 725 | 727 | 729 | 731 | 733 | 735 |
| 47 | 753 | 755 | 757 | 759 | 761 | 763 | 765 | 767 |
| 48 | 784 | 786 | 788 | 790 | 792 | 794 | 796 | 798 |
| 49 | 816 | 818 | 820 | 822 | 824 | 826 | 828 | 830 |
| 50 | 848 | 850 | 852 | 854 | 856 | 858 | 860 | 862 |
| 51 | 880 | 882 | 884 | 886 | 888 | 890 | 892 | 894 |
| 52 | 785 | 787 | 789 | 791 | 793 | 795 | 797 | 799 |
| 53 | 817 | 819 | 821 | 823 | 825 | 827 | 829 | 831 |
| 54 | 849 | 851 | 853 | 855 | 857 | 859 | 861 | 863 |
| 55 | 881 | 883 | 885 | 887 | 889 | 891 | 893 | 895 |

Table 10. DLP650LNIR 2xLVDS DMD Data Pixel Mapping D_B(15,13,11,9,7,5,3,1) (continued)

| DCLK EDGE | D_B(1) | D_B(3) | D_B(5) | D_B(7) | D_B(9) | D_B(11) | D_B(13) | D_B(15) |
|-----------|--------|--------|--------|--------|--------|---------|---------|---------|
| 56 | 912 | 914 | 916 | 918 | 920 | 922 | 924 | 926 |
| 57 | 944 | 946 | 948 | 950 | 952 | 954 | 956 | 958 |
| 58 | 976 | 978 | 980 | 982 | 984 | 986 | 988 | 990 |
| 59 | 1008 | 1010 | 1012 | 1014 | 1016 | 1018 | 1020 | 1022 |
| 60 | 913 | 915 | 917 | 919 | 921 | 923 | 925 | 927 |
| 61 | 945 | 947 | 949 | 951 | 953 | 955 | 957 | 959 |
| 62 | 977 | 979 | 981 | 983 | 985 | 987 | 989 | 991 |
| 63 | 1009 | 1011 | 1013 | 1015 | 1017 | 1019 | 1021 | 1023 |
| 64 | 1040 | 1042 | 1044 | 1046 | 1048 | 1050 | 1052 | 1054 |
| 65 | 1072 | 1074 | 1076 | 1078 | 1080 | 1082 | 1084 | 1086 |
| 66 | 1104 | 1106 | 1108 | 1110 | 1112 | 1114 | 1116 | 1118 |
| 67 | 1136 | 1138 | 1140 | 1142 | 1144 | 1146 | 1148 | 1150 |
| 68 | 1041 | 1043 | 1045 | 1047 | 1049 | 1051 | 1053 | 1055 |
| 69 | 1073 | 1075 | 1077 | 1079 | 1081 | 1083 | 1085 | 1087 |
| 70 | 1105 | 1107 | 1109 | 1111 | 1113 | 1115 | 1117 | 1119 |
| 71 | 1137 | 1139 | 1141 | 1143 | 1145 | 1147 | 1149 | 1151 |
| 72 | 1168 | 1170 | 1172 | 1174 | 1176 | 1178 | 1180 | 1182 |
| 73 | 1200 | 1202 | 1204 | 1206 | 1208 | 1210 | 1212 | 1214 |
| 74 | 1232 | 1234 | 1236 | 1238 | 1240 | 1242 | 1244 | 1246 |
| 75 | 1264 | 1266 | 1268 | 1270 | 1272 | 1274 | 1276 | 1278 |
| 76 | 1169 | 1171 | 1173 | 1175 | 1177 | 1179 | 1181 | 1183 |
| 77 | 1201 | 1203 | 1205 | 1207 | 1209 | 1211 | 1213 | 1215 |
| 78 | 1233 | 1235 | 1237 | 1239 | 1241 | 1243 | 1245 | 1247 |
| 79 | 1265 | 1267 | 1269 | 1271 | 1273 | 1275 | 1277 | 1279 |

8.3.2 Data Bus Operations

8.3.2.1 Row Addressing

The DIN (input data), DCLKIN (input data clock), and DVALID (data valid) signals enable the DLPC410 to capture one row of customer input data and send that data to the DMD. For the DMD to know specifically to which row the data will be applied, the ROW_MD(1:0) (row mode), the ROW_AD(10:0) (row address), and the NS_FLIP (North/South Flip) signal inputs must be presented to the DLPC410 inputs during each row cycle. [Table 11](#) shows the number of rows for each DMD supported by the DLPC410.

Table 11. DMD Row and Columns

| TYPE | COLUMNS | ROWS | CLOCKS PER ROW | NO. OF DATA LINES |
|----------------------------|----------------------------|------|----------------|-------------------|
| DLP650LNIR DMD | 1280 | 800 | 40 | 16 |
| DLP7000 and DLP7000UV DMDs | 1024 | 768 | 16 | 32 |
| DLP9500 and DLP9500UV DMDs | 1920 (2048) ⁽¹⁾ | 1080 | 16 | 64 |

(1) The DLP9500 and DLP9500UV DMDs have 2048 memory cells per row. There are 64 bits at the beginning of each row and 64 bits at the end of each row which do not have corresponding DMD micromirrors. These 128 memory cells must be loaded with data but the data content can be arbitrary and will not affect the 1920 physical micromirrors within that row.

DMD data is loaded into the DMD SRAM pixels one row of data at a time. The DLP9500 and DLP9500UV require pattern data input to all four input data buses (A,B,C,D) while the DLP650LNIR, DLP7000 and DLP7000UV require pattern data to be input to two input data buses (A,B). The DLP650LNIR uses only the odd data bus pins of input buses A and B. The DMD input data buses are provided by the following DLPC410 outputs:

- DDC_DCLKOUT - high speed 2xLVDS data clock out to DMD
- SCTRL - high speed control bus to DMD
- DDC_DOUT[X:Y] - 2xLVDS data bus where X and Y depend on the DMD.

These signals are all output from the DLPC410 and are listed in [Pin Configuration and Functions](#). Data and control from the DLPC410 are clocked into the DMD on both the rising and falling edges of the DDR data clocks: DDC_DCLKOUT_[A, B] for the 2 input bus DMDs and DDC_DCLKOUT_[A, B, C, D] for the 4 input bus DMDs. Data loading does not cause mirror state changes - mirrors transition to the next state only when a Mirror Clocking Pulse (Reset) operation is performed.

The row load length in clocks can be determined by the following equation: number row clocks = number of pixels per row / (total data buses bit width × 2 edges per clock). The "2 edges per clock" in the denominator is a direct result of the Dual Data Rate (DDR) nature of the DMD input data bus. This equation yields the results shown in [Table 11](#)

The DMD incorporates single row write operations using a row address counter that has different modes of operation. These modes are dependent on the state of the ROW_MD, ROW_AD, and NS_FLIP input signals. As shown in [Table 12](#), ROW_MD(1:0) determines the row mode for a given Row Cycle, and, when ROW_MD = "10", then ROW_AD(10:0) selects the customer supplied single row address. ROW_MD and ROW_AD must be asserted and deasserted synchronously with DVALID and must be valid synchronous to the beginning of the data as shown in [Figure 9](#). If only one specific mode will be utilized in a customer system application, it is certainly acceptable to leave these values at their same desired input levels for as long as desired.

Row address orientation depends on the North/South Flip Flag (NS_FLIP) input to the DLPC410. This input controls if the DMD starting row address starts at the top of the DMD (Row 0) and increments downward, or from the bottom of the DMD (last row) and decrements upward.

The row address counter does not automatically wrap-around when using the increment row address pointer instructions. For example, after the final row is addressed, the row address pointer must be set to row 0.

Table 12. Row Modes and Row Addresses

| ROW_MD(1:0) | ROW_AD(10:0) ⁽¹⁾ | NS_FLIP ⁽²⁾ | ACTION |
|-------------|-----------------------------|------------------------|---|
| "00" | "xxxxxxxxxx" | "x" | Row No-Op (No data write) |
| "01" | "xxxxxxxxxx" | 0 | Increment internal row address by '1' - write concurrent data into that row |
| "01" | "xxxxxxxxxx" | 1 | Decrement internal row address by '1' - write concurrent data into that row |
| "10" | ROW_AD(10:0) | "x" | Set Random row address as specified on ROW_AD(10:0) inputs - write concurrent data into that row. |
| "11" | "xxxxxxxxxx" | 0 | Set First row address (DMD Row 0) and write concurrent data into that row |
| "11" | "xxxxxxxxxx" | 1 | Set Last row address (DMD last row) - write concurrent data into that row (Last row = 767 for DP7000, 799 for DLP650LNIR, 1079 for DLP9500) |

(1) "xxxxxxxxxx" and "x" are don't care situations.

(2) It is recommended NS_FLIP remain constant throughout the loading of the DMD and not change on a row cycle basis.

8.3.2.2 Single Row Write Operation

Once initialization is complete (INIT_ACTIVE = 0) the user is free to send data and control information to the DLPC410. When the user asserts the DVALID signal for the LVDS input buses, the DLPC410 samples the customer supplied binary input pattern data (DIN) as well as the Row Mode, Row Address, Block Mode, Block Address, and other control information. The DLPC410 then sends pattern data synchronously to the DMD along with row address and control information. The row cycle period is defined by the Clocks per Row in [Table 11](#) and is synchronous with DVALID as shown in [Figure 9](#). If DVALID is removed midway in a Row Cycle, the DLPC410 continues loading data regardless of data validity until the internal row cycle counter reaches the terminal count of Clocks/Row for that DMD.

[Figure 9](#) is an example of a single Row Cycle for the DLP7000 DMD. A total of 32 bits of input data are presented to the DLPC410 on each clock edge (16 bits on Bus A + 16 bits on Bus B) . An entire line must be written for data to be latched into DMD memory and it requires 16 DDR clock cycles to write a single row of 1024 bits.

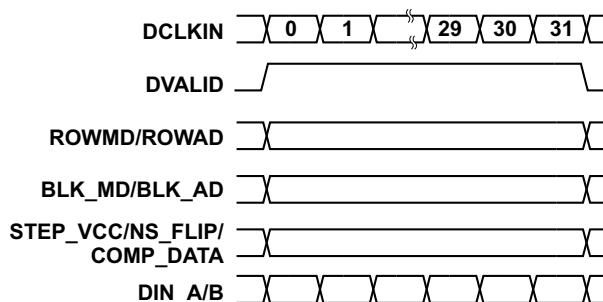


Figure 9. Single Row Write Operation (DLP7000 DMD)

8.3.2.3 No-Op Row Cycle Description

A Row No-Op is a row cycle in which setting ROW_MD = "00" commands the DLPC410 that within the current row cycle, no **Row Write** operation is to be performed. A Block No-Op is a row cycle in which BLK_MD = "00" commands the DLPC410 that within the current row cycle no **Block** Operation is to be performed. Row No-Ops can be inserted when only block operations are desired, Block No-ops can be inserted when only Row Write operations are desired, or both Row No-Ops and Block No-Ops can be performed at the same time when neither type of operation is desired (as shown in Figure 10). No-Ops are frequently inserted in the stream of data and commands when delays are desired to complete on-going operations to avoid violating delay requirements.

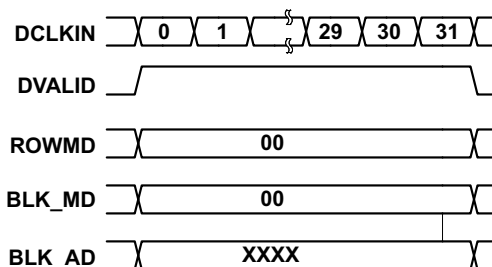


Figure 10. No-Op Row Cycle (DLP7000 example)

8.3.3 DMD Block Operations

Previous sections have described in detail how to send binary pattern data through the DLPC410 Controller to the connected DMD. Although the data loading process involves loading the specified data into the SRAM cells in the DMD array, this loading of data does not change the physical state of the DMD Micromirrors. The state of the mirrors can only be changed (or left the same if the data under the mirrors is unchanged) when a Mirror Clocking Pulse (Reset) is applied to the DMD MBRST pins from the DLPA200.

A sequence of Mirror Clocking Pulses (Resets) begins by asserting a row cycle with BLK_MD and BLK_AD as described in Table 14. Shortly after the row cycle, RST_ACTIVE output to the customer transitions to logic '1' for approximately 4.5 μs indicating a Mirror Clocking Pulse operation is in progress. During this time, no additional Mirror Clocking Pulses may be initiated until RST_ACTIVE returns to logic '0'.

RST_ACTIVE does not return to logic '0' unless:

- data load row cycles are issued to other DMD blocks as in Figure 14 or,

- No-Op row cycles are provided to the DLPC410 to enable MCP or Block Clear operations to continue

This is accomplished by asserting DVALID while holding ROWMD = "00" and BLKMD = "00" for the pre-requisite number of CLKS per ROW (Table 11) clock cycles, as in Figure 10. If no other blocks need to be loaded then continuous No-Op row cycles are applied as in Figure 10.

8.3.3.1 Mirror Clocking Pulse (MCP)

A Mirror Clocking Pulse is an analog voltage waveform provided to the DMD from the DLPA200 DMD Micromirror Driver. This waveform times the electrostatic forces which cause each micromirror to transition to its next state. This next state is determined by the data in the SRAM cell beneath each pixel. If the data has changed, the micromirror will rotate its position 24 degrees to the opposite state. If the data is unchanged, the mirror will remain in the same state. The DLPC410 instructs the DLPA200 to apply Mirror Clocking Pulses to the DLPA200 based on instructions from the user.

NOTE

A Mirror Clocking Pulse (MCP) is often referred to as a "Reset" operation.

8.3.3.2 Reset Active (RST_ACTIVE)

RST_ACTIVE is an output from the DLPC410 to indicate to the user that a user requested Reset (MCP) has been accepted by the DLPC410. Shortly after the user requests a Reset (MCP) by asserting the appropriate Block Control signals defined in [DMD Block Control Signals](#), RST_ACTIVE output to the user will transition to logic '1' for approximately 4.5 μ s indicating a Mirror Clocking Pulse operation is in progress. While RST_ACTIVE is logic '1', no additional Mirror Clocking Pulse requests may be initiated by the user until RST_ACTIVE returns to logic '0'. RST_ACTIVE is synchronized to a version of DCLKIN. As such, circuits in the application FPGA should consider this signal asynchronous and use standard synchronization techniques to assure reliable registering of this signal.

NOTE

After a Mirror Clocking Pulse or Clear command is given, RST_ACTIVE may not be asserted until up to 60ns after the command. During this time, no other command should be given.

8.3.3.3 DMD Block Control Signals

The DMD micromirrors and their corresponding SRAM pixels are organized into horizontal rows where data is loaded one row at a time. DMD Blocks are defined as a group of sequential rows of mirrors. Each mirror block is measured in groups of [ROWS per BLK] as described in [Table 11](#). DMD blocks are typically numbered from 0 to 15 with 0 being the block at the top of the DMD (row 0) and 15 being the block at the bottom of the DMD.

Table 13. DMD Block Characteristics

| DMD TYPE | COLUMNS | ROWS | BLOCKS | ROWS PER BLOCK |
|----------------------------|---------|------|--------|----------------|
| DLP650LNIR DMD | 1280 | 800 | 16 | 50 |
| DLP7000 and DLP7000UV DMDs | 1024 | 768 | 16 | 48 |
| DLP9500 and DLP9500UV DMDs | 1920 | 1080 | 15 | 72 |

8.3.3.3.1 Block Mode - BLK_MD1:0)

The Block Mode signals define the type of block operation the user would like to take place. The allowed operations which can be requested are defined in [Table 14](#). These signals work alongside the RST2BLK and the Block Address signals to provide the gamut of Block Operations that enable DMD mirrors to update to their next used desired state. These signals should be setup synchronously with the start of a row cycle.

8.3.3.3.2 Block Address - BLK_AD(3:0)

The Block Address signals help to specify which block or group of blocks will be acted upon in a user issued Block Operation. They work with the RST2BLK and Block Mode signals to indicate which block or group of blocks will see a Reset (MCP). These signals should be setup synchronously with the start of a row cycle.

8.3.3.3.3 Reset 2 Blocks - $\overline{\text{RST2BLK}}$

The Reset 2 Blocks ($\overline{\text{RST2BLK}}$) signal helps to signify a multiple block operation is requested by the user, where, depending on the state of $\overline{\text{RST2BLK}}$, either two blocks or 4 blocks will be Reset together. The specific blocks to be Reset will then be determined by the Block Mode and Block Address. This signal should be setup synchronously with the start of a row cycle.

NOTE

$\overline{\text{RST2BLK}}$ needs to be kept low during initialization for proper setup of the system. Dynamic changes to $\overline{\text{RST2BLK}}$ during normal operation are not recommended.

8.3.3.4 DMD Block Operations

Once a portion or all of the DMD is loaded with new data, the user typically requests a Block Operation to be performed. This operation causes the DLPC410 to initiate one of the many block related activities to a block or group of blocks to the DMD. Available Block operations are:

- **Block No-Op** - user requests via $\text{BLK_MD}(1:0) = "00"$ that no block operations are to take place in this row cycle. This is typically the case for row cycles used for data loading purposes only without any block operations.
- **Block Clear Request** - user requests a single block to be cleared causing all SRAM cells within that block to be reset to logic '0'.
- **Single Block Reset Request** - user requests a single DMD block be provided a Reset (MCP) signal to cause the micromirrors within that block to update to their new values.
- **Dual Block Reset Request** - user requests two sequential DMD blocks be provided Reset (MCP) signals to cause the micromirrors within those blocks to update to their new values.
- **Quad Block Reset Request** - user requests four sequential DMD blocks be provided Reset (MCP) signals to cause the micromirrors within those blocks to update to their new values.
- **Global Reset Request** - user requests all DMD blocks be provided Reset (MCP) signals to cause all DMD micromirrors to update to their new values.
- **DMD Park (Float) Request** - user requests all DMD micromirrors be provided special Parking Reset (MCP) signals causing the micromirrors within those blocks to relax to their unbiased state. This request is intended to place the micromirrors in the Parked state prior to power removal (shutdown).

Mirror blocks are addressed using the Block Address ($\text{BLK_AD}[3:0]$) signals for application of either a Mirror Clocking Pulse (Reset) or a Memory Clear operation by asserting the block control signals of [Table 14](#) at the start of each row data load. $\overline{\text{RST2BLK}}$, Block Mode ($\text{BLK_MD}[1:0]$), and $\text{BLK_AD}[3:0]$ define the requested operation as shown in [Table 14](#) and designate which mirror block or mirror blocks are issued a Mirror Clocking Pulse or are Cleared. The number of DMD blocks and BLOCKS/ROW is unique to each DMD - refer to the individual DMD data sheets for DMD block definition.

Table 14. Block Control Signals and Operations

| RST2BLK | BLK_MD(1:0) | BLK_AD(3:0) | OPERATION | OPERATION TYPE |
|---------|-------------|-------------|--------------------|---------------------------------------|
| x | 00 | xxxx | None | Block No-OP |
| x | 01 | 0000 | Clear block 00 | Block Clear Request ⁽¹⁾⁽²⁾ |
| x | 01 | 0001 | Clear block 01 | |
| x | 01 | 0010 | Clear block 02 | |
| x | 01 | 0011 | Clear block 03 | |
| x | 01 | 0100 | Clear block 04 | |
| x | 01 | 0101 | Clear block 05 | |
| x | 01 | 0110 | Clear block 06 | |
| x | 01 | 0111 | Clear block 07 | |
| x | 01 | 1000 | Clear block 08 | |
| x | 01 | 1001 | Clear block 09 | |
| x | 01 | 1010 | Clear block 10 | |
| x | 01 | 1011 | Clear block 11 | |
| x | 01 | 1100 | Clear block 12 | |
| x | 01 | 1101 | Clear block 13 | |
| x | 01 | 1110 | Clear block 14 | |
| x | 01 | 1111 | Clear block 15 | |
| x | 10 | 0000 | Reset block 00 | Single Block Reset Request |
| x | 10 | 0001 | Reset block 01 | |
| x | 10 | 0010 | Reset block 02 | |
| x | 10 | 0011 | Reset block 03 | |
| x | 10 | 0100 | Reset block 04 | |
| x | 10 | 0101 | Reset block 05 | |
| x | 10 | 0110 | Reset block 06 | |
| x | 10 | 0111 | Reset block 07 | |
| x | 10 | 1000 | Reset block 08 | |
| x | 10 | 1001 | Reset block 09 | |
| x | 10 | 1010 | Reset block 10 | |
| x | 10 | 1011 | Reset block 11 | |
| x | 10 | 1100 | Reset block 12 | |
| x | 10 | 1101 | Reset block 13 | |
| x | 10 | 1110 | Reset block 14 | |
| x | 10 | 1111 | Reset block 15 | |
| 0 | 11 | 0000 | Reset blocks 00-01 | Dual Block Reset Request |
| 0 | 11 | 0001 | Reset blocks 02-03 | |
| 0 | 11 | 0010 | Reset blocks 04-05 | |
| 0 | 11 | 0011 | Reset blocks 06-07 | |
| 0 | 11 | 0100 | Reset blocks 08-09 | |
| 0 | 11 | 0101 | Reset blocks 10-11 | |
| 0 | 11 | 0110 | Reset blocks 12-13 | |
| 0 | 11 | 0111 | Reset blocks 14-15 | |
| 1 | 11 | 000x | Reset blocks 00-03 | Quad Block Reset Request |
| 1 | 11 | 001x | Reset blocks 04-07 | |
| 1 | 11 | 010x | Reset blocks 08-11 | |
| 1 | 11 | 011x | Reset blocks 12-15 | |
| x | 11 | 10xx | Reset blocks 00-15 | Global Reset Request |
| x | 11 | 11xx | Float blocks 00-15 | DMD Park Request |

- (1) Each Block Clear operation for DLP650LNIR and DLP7000(UV) DMDs will clear all SRAM cells of one DMD block (reset to '0') within one row cycle duration.
- (2) Each Block Clear operation for DLP9500(UV) DMDs must be followed by two No-Op row cycles. To clear one DMD Block, one Block Clear Request row cycle followed by two consecutive No Op row cycles are required. In total, 15 Block Clear Request row cycles and 30 No-Ops are required to clear the entire 15 block DMD array.

Block operations cause the DMD micromirrors to transition to their next state. Some notes and restrictions regarding block operations are:

- A Block No-Op row cycle causes no new block operations to occur. Block No-Op row cycles can be used to provide extended time for a previous operation.
- The Block Clear operation resets all SRAM pixels in the designated block to logic zero during the current row cycle.
- It is not necessary to Clear a block if it will be reloaded with new data (just like a normal memory cell).
- It is not possible to Clear a block while writing to a different block.
- It is possible to issue a Mirror Clocking Pulse to a block while data loading a different block.
- The DLP9500 and DLP9500UV DMDs have 15 blocks (block 0 – block 14). Block operations on block 15 have no function for this DMD.
- $\overline{\text{RST2BLK}}$ should be set to one value and not adjusted during normal system operation. A change in $\overline{\text{RST2BLK}}$ is not immediately effective and will require more than one row load cycle to complete.

8.3.3.4.1 Global Reset (MCP) Consideration

A Global Reset ($\text{BLK_MD} = 11$ and $\text{BLK_AD} = 10\text{XX}$) is an operation which Resets (MCP) all DMD blocks at the same time. The Global Reset duration is the same as the Single, Dual, and Quad Block Reset (MCP). In addition to requiring a No-Op row cycle to initiate the Global Reset, row cycles (either No-Op row cycles or data loading row cycles) are required to continually be provided to complete the Global Reset operation. If continual provision of row cycles is not provided, the customer interface monitoring RST_ACTIVE may never see RST_ACTIVE transition back low to indicate the Reset is complete. Customers should always provide valid row cycles, either No-Ops or data loading row cycles. To know when the reset operation is complete, customers can either monitor RST_ACTIVE high-to-low transition, or use a counter to know when at least a 4.5 μs period has expired from the start of the Global Reset. From that point on, the customer also needs to count the mirror settling time of the DMD to expire prior to loading the next data into the DMD.

NOTE

Reset (MCP) operations to a specific block or consecutive blocks of the DMD are also referred to "Block Resets" or just "Reset" operations. This is because they are physically "resetting" the micromirrors of the block to their next physical positions based on the underlying data.

NOTE

(DLP9500 and DLP9500UV DMDs Only) To clear one Mirror Clocking Pulse (Reset) Group in the DMD Block, one Clear command followed by two consecutive No Operation commands (No-Ops) are required. Therefore, 15 total Block Clear commands and 30 total No-Ops commands are required to clear the entire DMD array.

8.3.4 Other Data Control Inputs

It is recommended that the Complement and Flip flags be set to one value and not adjusted during normal system operation. These controls are asserted through a different mechanism than the input data bus and row controls, hence their effect is asynchronous and cannot be expected to take effect immediately upon assertion.

8.3.4.1 Complement Data

By setting the COMP_DATA flag high, the user is able to command the DMD to internally complement its data inputs prior to loading the data into the mirror array. At least 0.6 ms is needed for the signal to be loaded. This signal should not be used to invert data on a row basis. When used with the "Clear" command, the mirrors are still set to zero regardless of the COMP_DATA bit. The COMP_DATA signal should be kept low during initialization to ensure proper setup of the system.

8.3.4.2 North/South Flip

NS_FLIP allows the user to specify the loading direction of rows in the DMD when used with $\text{ROWMD} = "01"$. This control has no effect if $\text{ROWMD} = "10"$.

Row Addressing and Table 12 describe the effect of N/S flip. If NS_FLIP is set, this does not reverse the direction of Mirror Clocking Pulse groups (blocks). For example, the normal case is to Mirror Clocking Pulse blocks 0 – 15 in order. When NS_FLIP is set, the order of block Mirror Clocking Pulses must be reversed to 15 – 0.

The NS_FLIP signal should be kept low during initialization to ensure proper setup of the system.

8.3.5 Miscellaneous Control Inputs

8.3.5.1 \overline{ARST}

\overline{ARST} is an active low, asynchronous reset. This reset can be sourced from a voltage supervisor or from the customer interface. Be aware that the chipset will not operate correctly if all DLPC410 power supplies are not in range at the time this reset is released.

8.3.5.2 CLKIN_R

The reference clock, CLKIN_R, supplied from an oscillator must be 50 MHz. This is required for precise timing used to perform the DMD Mirror Clocking Pulse (Reset). This clock should be valid prior to releasing \overline{ARST} .

8.3.5.3 DMD_A_RESET

DMD_A_RESET is an active low reset to the DMD. This signal is deasserted as appropriate at the end of system initialization.

8.3.5.4 Watchdog Timer Enable ($\overline{WDT_ENABLE}$)

The DLPC410 contains a watchdog timer that initiates a global DMD Mirror Clocking Pulse in the event that the DMD has not received any Mirror Clocking Pulse by the user within the last 10 seconds. This auto-generated Mirror Clocking Pulse function is to provide Mirror Clocking Pulses to the DMD mirrors to prevent long term landed mirrors in the event the input data and source control has been inadvertently disrupted. This capability can be user disabled by setting WDT_ENABLE to logic '1'. Note that the global DMD Mirror Clocking Pulse generated by the watch dog timer is asynchronous to any/all activity on the DMD input data bus - therefore there is no guarantee as to the validity of the data displayed on the DMD once this pulse occurs, at least until new data is subsequently loaded and displayed.

8.3.6 Miscellaneous Status Outputs

8.3.6.1 INIT_ACTIVE

The INIT_ACTIVE signal ins an output which indicates that the DMD, Digital Micromirror Driver, and the Digital Controller are in an initialization state after power is applied. During this initialization period, the DLPC410 is calibrating the data interface, initializing the DMD, and DLPA200(s). When this signal goes low, the system has completed initialization. See the section on System initialization

8.3.6.2 DMD_Type(3:0)

The DLPC410 only supports the DMDs indicated in Table 15. At power-up, the DLPC410 checks the DMD signature. If the DLPC410 finds the DMD is not supported, it will not allow the user to display data on the DMD and indicated that the DMD is unsupported.

DMD_TYPE(3:0) is an output from the DLPC410 to the user FPGA which will indicate to the user which DMD is connected to the DLPC410, or in another case, the DMD is not supported or a DMD is not properly connected.

Table 15. DMD Characteristics

| DMD_TYPE(3:0) | DMD Reported |
|---------------|----------------------------|
| 0000 | DLP9500 and DLP9500UV DMDs |
| 0001 | DLP7000 and DLP7000UV DMDs |
| 0111 | DLP650LNIR DMD |
| 1111 | Unsupported DMD / No DMD |

8.3.6.3 DDC_VERSION(2:0)

These three pins identify the version of the DLPC410 determined by the contents of DLPR410. If a problem is encountered which encourages you to contact a Texas Instruments representative, please provide the version number along with the detailed information of the problem. See the DLPR410 datasheet ([DLPS027](#)) for the version number reported on these pins.

8.3.6.4 LED0

The LED0 signal is typically connected to an LED to show that the DLPC410 is operating normally. The signal is 1 Hz with 50% duty cycle, otherwise known as the heartbeat.

8.3.6.5 LED1

The LED1 signal is typically connected to an LED indicator to show the status of system initialization and the status of the clock circuits. The LED1 signal is asserted only when system initialization is complete and clock circuits are initialized. Logically, these signals are ANDed together to show an indication of the health of the system. If the Phase Locked Loop (PLL) connected to the data clock and the DMD clock are functioning correctly after system initialization, the LED will be illuminated.

8.3.6.6 DLPA200 Control Signals

Coordinating the operation of the DLPA200 with the DMD is one of the primary functions of the DLPC410. During system initialization, the DLPC410 releases the reset pin (DAD_INIT) and communicates with the DLPA200 via a serial bus to configure the device. Once this is complete, the high voltage output pins are enabled to prepare for command execution. As the DLPC410 is commanded to load data and perform Mirror Clocking Pulses, the DAD_ADDR address, DAD_MODE mode, DAD_SEL select and DAD_STROBE strobe signals are asserted as appropriate to cause the Mirror Clocking Pulses. The operation of these signals are managed by the DLPC410 and, besides board layout and good design practices, should be of little concern to the end user.

8.3.6.7 ECM2M_TP_ (31:0)

These are reserved signals for test signal output. Do not drive these signals.

8.4 Device Functional Modes

The DLPC410 has one basic function which is to receive customer data at the inputs of the DLPC410 and deliver that data and any appropriate DMD control information to the DMD for displaying of binary patterns at very high speeds. The [Feature Description](#) section describes how binary pattern data is loaded into the DMD and ultimately where that data is displayed on the DMD. The following subsections describe the different display modes of operation of the DMD as enabled by the DLPC410.

8.4.1 DLPC410 Initialization and Training

8.4.1.1 Initialization

The INIT_ACTIVE signal indicates that the DMD, Digital Micromirror Driver, and the Digital Controller are in an initialization state after power is applied. During this initialization period, the DLPC410 is calibrating the data interface, initializing the DMD, and DLPA200(s). When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command row cycles must not be presented to the DLPC410 during the initialization. INIT_ACTIVE should be considered an asynchronous feedback signal to the user. Standard synchronization techniques should be applied. After initialization is complete, a delay of at least 64 DCLKIN clocks (on all input data buses being used) should be observed before the first DVALID is asserted on those data buses to ensure a clean start up process.

NOTE

Note: NS_FLIP, COMP_DATA, and RST2BLK signals should be kept low ('0') during initialization to ensure proper system setup.

8.4.1.2 Input Data Interface (DIN) Training

The DLPC410 detects the phase differences between the $\frac{1}{2}$ speed clock (used in the customer device driving the LVDS data) and the internally generated $\frac{1}{2}$ speed data clocks and automatically corrects their alignment. This is done by the customer FPGA supplying a simple repeating pattern on all of the data inputs while the INIT_ACTIVE output of the DLPC410 is high/active. The details of the training pattern are described below.

This is a simple block diagram of the training pattern insertion logic.

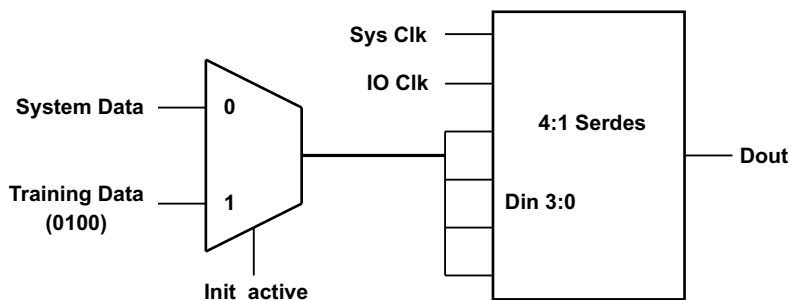


Figure 11. Block Diagram of Training Pattern Logic

The expected training pattern is 0100. In [Figure 12](#) the data input to the 4:1 SERDES cells is captured on the rising edge of the $\frac{1}{2}$ speed system clock. The output latency shown is based on the documentation for the Xilinx SERDES cells. Individual implementation may vary depending on the type of cells, technology, and design technique used.

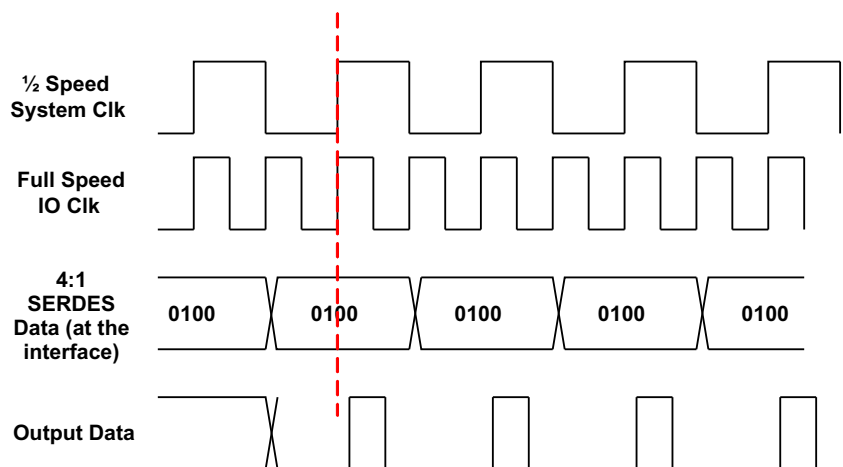


Figure 12. Training Pattern Alignment

NOTE

In Xilinx FPGAs (due to the construction of the ISERDES and OSERDES cells) a pattern of 0010 needs to be applied to the output/transmitting SERDES cells data pins (D1 = 0, D2 = 0, D3 = 1, D4 = 0) in order to receive a result of 0100 (Q1 = 0, Q2 = 1, Q3 = 0, Q4 = 0) at the input/receiving SERDES cell.

The patterns should be applied on all of the input data and DVALID pins. In this respect, the interface is treated as a 17 bit interface with DVALID being the 17th data bit. The receiving logic in the DLPC410 will shift the data until the correct pattern is seen at the inputs. The SERDES cells align the incoming data with the ½ speed system clock (derived from the full speed data clock). This allows DLPC410 to correctly align the DVALID signal and the incoming data and will contribute to a more robust interface. It is important that the training pattern is applied to the DVALID and data inputs of the DLPC410 before reset to the device is deasserted, as training commences immediately on the deassertion of reset. The INIT_ACTIVE signal is asserted while the device is held in reset in order to help facilitate this behavior.

8.4.2 DLPC410 Operational Modes

The following modes of operation are frequently used operational modes enabling customers to update DMD data and to control how, where, and how long their binary patterns are displayed on the DMD. Customers frequently pick the mode which provides the best performance and simplicity for their specific system. Combinations of these modes can also be used.

8.4.2.1 Single Block Mode

A single block of DMD memory cells can be updated by providing successive row cycles with valid data (DVALID) to the DLPC410 until the desired amount of data is presented. Since different DMDs have different row and block sizes (and therefore different number of clocks per row or per block), the amount of time it takes to load a block of DMD data will be different for each DMD. Leveraging [Table 11](#) and [Table 13](#), we can calculate the single block load time for each DMD by the following equation: Block Load Time = Clock Period × number CLKS per ROW × number ROWS per BLK. The results are shown in [Table 16](#) for DLPC410 supported DMDs.

Table 16. DMD Block Load Time (400 MHz DMD Clock)

| DMD | DMD BLOCK LOAD TIME |
|---------------------|---------------------|
| DLP650LNIR | 5.00 μsec |
| DLP7000 / DLP7000UV | 1.92 μsec |
| DLP9500 / DLP9500UV | 2.88 μsec |

Once the block is loaded with data, a Block Reset (MCP) for that block must be initiated. This can be performed by providing a row cycle with BLKMD = "10" and with BLK_AD(3:0) equal to the block just loaded. Upon initiation of the Block Reset, RST_ACTIVE will transition high for approximately 4.5 μs indicating a Reset operation is taking place and that no additional Reset Requests will be accepted during that time. In the case of wanting to reload the same block with new data, one must wait for the 12.5 μs (RST_ACTIVE (4.5 μs) + the micromirror settling time (8 μs)) before the reload of the same block can start. Waiting this time allows for the DMD micromirrors in that block to settle to a stable state prior to reloading the memory cells underneath with new data. [Figure 13](#) shows a single block load, Mirror Clocking Pulse and reload sequence with the 8 μs periods indicating micromirror settling times.

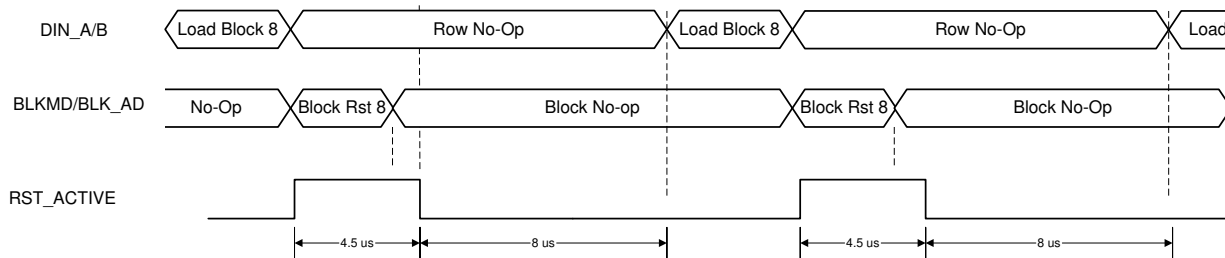


Figure 13. Block Load, Reset, and Same Block Reload

Although [Figure 13](#) shows that one must wait for the mirror settling time of the current block (Block=8 in this case) to complete before reloading data into the same block (8), it is possible to load data to a different block while waiting for Block 8 to settle. However, it must be a block which is not currently being Reset nor which has micromirrors which are still settling. This method is used in the Phased Mode of operation described in [Single Block Phased Mode](#).

NOTE

The RST_ACTIVE and micromirror settling times indicated in this example are typical for many DMDs. See each individual DMD data sheet for more information on the micromirror switching and settling times.

NOTE

Customers do not have to load the entire block at one time unless specifically directed. The DLPC410 supports individual row loads and partial block loads. Customers can use ROW_AD(10:0) to load one (or more) specific Row Addresses within any block. These loading modes are defined in [Table 12](#). Care must be taken to ensure all RST_ACTIVE time plus DMD mirror settling times are taken into account prior to re-loading any rows in the same block once a Reset has been requested.

8.4.2.2 Single Block Phased Mode

Single Block Phased Mode is best described as "phasing" the data load operation with the Block Reset operation. The major advantages of Phased Modes (Single, Dual, and Quad) in general are the idea of not having to wait for the micromirror settling time duration to complete prior to the next block reset, and for not having to wait for the Reset Request to complete prior to loading more data. In the example of [Figure 14](#), Block 15 is loaded with data while the Reset operation is taking place for Block 14 (Rst 14). The Reset Request (BLKMD and BLK_AD) for Block 14 needs to be one row cycle in duration minimum but can be extended to additional row cycles. Subsequent row cycles containing a valid Reset Request will be ignored until RST_ACTIVE goes low. Therefore, BLKMD and BLK_AD should transition from a Reset Request to a Block No-Op while RST_ACTIVE is still asserted as once RST_ACTIVE de-asserts there is the likelihood of an undesired Reset Request to be generated on the same block.

In [Figure 14](#), Block 0 is issued a Block Reset concurrently with data being loaded into the next block (1). The Row Cycles of the Block 1 data loading capture the Reset Request for Block 0, and provide continued Row Cycles for the duration of both the Block Load and the Block Reset. Note that the loading of block 1 does not need to wait for the mirror settling time of Block 0. This is repeated until the last block is Reset (which might also contain loading the next Block 0 data). Since the DLP650LNIR block load time is already longer than the RST_ACTIVE time, full utilization of its bandwidth is readily achieved in a single block phased mode.

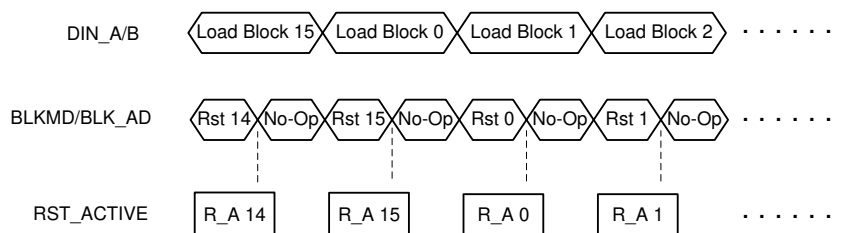


Figure 14. Single Block Phased Mode with Longer Block Load Times

Depending on the DMD type, the RST_ACTIVE duration of 4.5us may be longer than a single block load time. For example, the sequence shown in Figure 15 shows that when the Block Load time is shorter than RST_ACTIVE, one should include Row No-Ops to create a delay until the current RST_ACTIVE transitions low. Once RST_ACTIVE transitions low, the first row cycle of the next block data load can occur while also providing the Reset Request for the previously loaded block. At least one row cycle minimum must be completed to initiate the Reset Request and the next Reset Request must wait until the data is loaded and RST_ACTIVE transitions low.

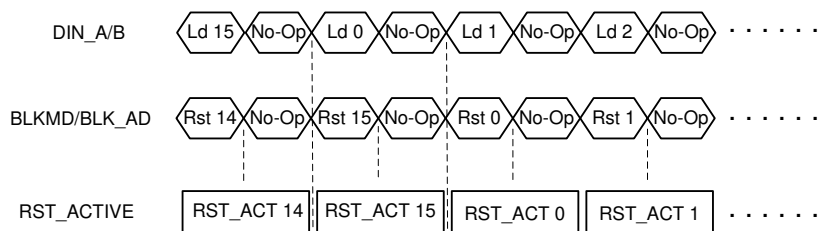


Figure 15. Single Block Phased Mode with Short Block Load Times

Figure 16 is nearly the same as Figure 15 except that the data loading of each block is timed such that it completes loading the block just about the same time the RST_ACTIVE signal goes low. Row No-Op cycles are used to provide the Reset Requests instead of data load row cycles. The benefit of this would be the delayed loading of data could provide more time for the customer application data processing upstream. In both cases, the next block Reset Request cannot be initiated until the previous Reset Request has completed.

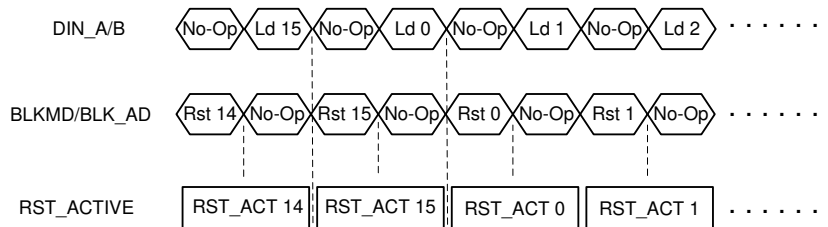


Figure 16. 2nd Single Block Phased Mode with Short Block Load Times

8.4.2.3 Dual Block Mode

Dual Block Mode can help to avoid the required delays (via No-Ops) encountered in a Single Phased Mode where the load time is less than the Reset duration. In the case of the DLP9500 DMD with a block load time of 2.88 μs, loading two blocks (2 × 2.88 = 5.76 μs) takes more time than the Reset duration (4.5 μs) so once the data is loaded, a Dual Block Reset Request can be issued immediately (instead of waiting for RST_ACTIVE) to the two blocks by setting RST2BLK to “0” and BLK_MD to “11” and the appropriate address in BLK_AD. This method is indicated in Figure 17.

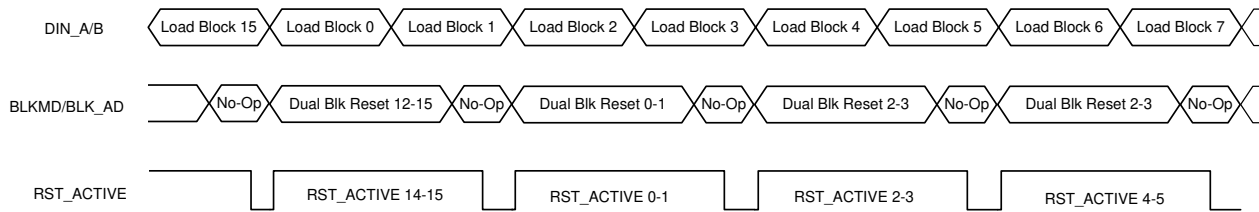


Figure 17. Dual Block Mode

8.4.2.4 Quad Block Mode

Quad Block mode is very similar to Dual Block mode but in Quad Block Mode, 4 Blocks are loaded with data and then Reset. In the case of the DLP7000 DMD with a block load time of 1.92 μ s, the loading of two blocks would still be less than the 4.5 μ s required for the Reset to complete so No-Ops would be required. To avoid inserting No-Ops in this case, loading four blocks ($4 \times 1.92 = 7.68 \mu$ s) is longer than the RST_ACTIVE duration (4.5 μ s) so once loaded, the 4 blocks can immediately be issued a Reset Request by ensuring RST2BLK = "1", BLK_MD = "11", and setting the appropriate BLK_AD address in the first row cycle of the next data block load.

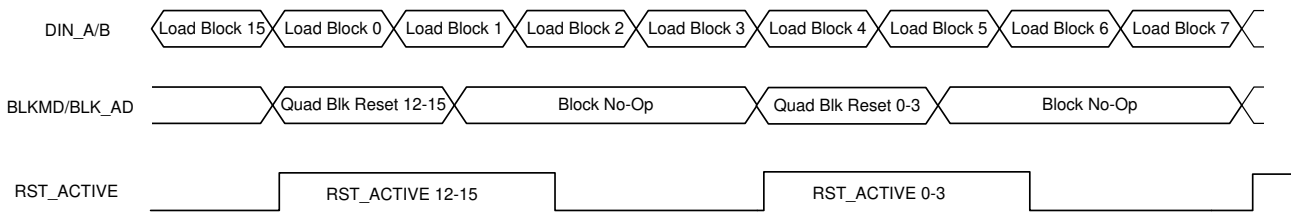


Figure 18. Quad Block Mode

Quad Block mode tends to offer customers the fastest full-DMD pattern rates combined with the largest solid state illuminations windows. Pattern rates for Single Block Phased and Dual Block Phased modes can sometimes be as fast as Quad Block rates, but the illumination windows can be smaller or even negative, thereby requiring delays between patterns to widen the illumination windows for solid state illuminators. These added delays will decrease the resulting pattern rates.

8.4.2.5 Global Mode

One of the simplest and most frequently utilized modes, the Global Mode involves loading the entire DMD with new pattern data and then issuing a Global Reset to update all DMD mirrors at the same time. Loading the entire DMD with data involves loading every row of every block. The time it takes to load the DMD is the block load time \times the number of blocks for that specific DMD. Table 17 shows the fastest DMD load times for DLPC410 supported DMDs.

Table 17. DMD Load Times (Entire DMD)

| DMD | DMD LOAD TIME (400 MHz Clock) |
|---------------------|-------------------------------|
| DLP650LNIR | 80.0 μ sec |
| DLP7000 / DLP7000UV | 30.7 μ sec |
| DLP9500 / DLP9500UV | 43.2 μ sec |

The Global Mode case is shown in [Figure 19](#). Following the loading of all rows in the device, a Row No-Op row cycle with a Global Reset Request must be issued to initiate the Reset Pulse and No-Ops should continue until ready to load the DMD again. If the global Reset Pulse is asserted prior to loading all rows of the device, rows which were not updated will show old data. Global mode is similar to [Single Block Mode](#) in that the mirror settling time must be taken into account prior to reloading the DMD data after a Reset Request is provided. This additional delay makes the Global Mode of operation inherently slower. However, if speed is not as important in a customer application, Global mode is great for its simplicity of DMD loading and Resetting.

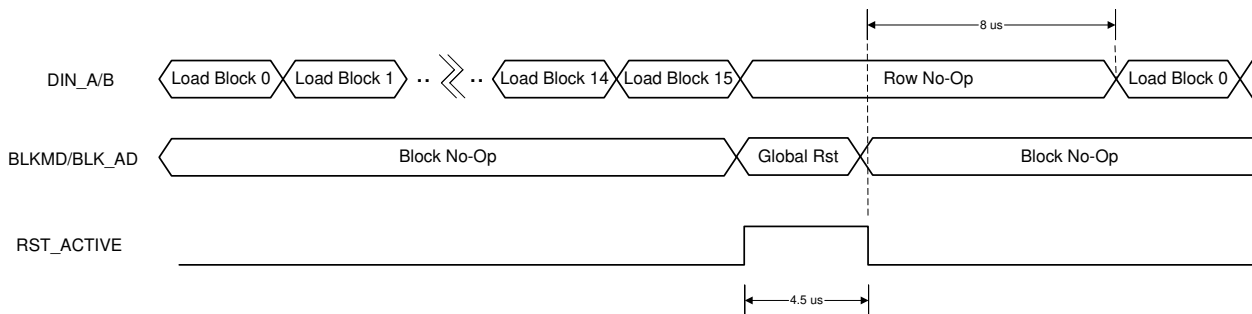


Figure 19. Full Device Load with Global Reset

8.4.2.6 DMD Park Mode

Park Mode places the DMD in a state where the micromirrors are not biased to either the plus or the minus side, but are instead floating in an unbiased and uncontrolled state. Hence, this is also referred to as Mirror Float mode. Parking (floating) the DMD mirrors should be performed when powering down the DMD to avoid leaving a static image on the DMD during down time or storage. The mirror can be Parked in one of two ways:

1. **PWR_FLOAT** input pin (recommended method) : asserting this input to the DLPC410 will cause the DLPC410 to automatically Park the mirrors in preparation for power removal. This operation is independent of any activity on the input data bus or Block operations. It is often best to drive this pin from both a power supervisor circuit which provides immediate DMD parking upon detecting input power removal, and from a programmable/controllable output from the customer application FPGA or processor.
2. **DMD Park (Float Blocks 0-15)** operation per [Table 14](#): A mirror float sequence begins with a row cycle with assertion of the proper **BLK_MD** and **BLK_AD** as described in [Table 14](#). Following the row cycle, the DMD releases the tension under each mirror so that all mirrors relax to a relatively flat position. The float operation takes approximately 3 μs to complete, during which time **RST_ACTIVE** is asserted.

NOTE

Park the DMD only when DC power is going to be removed from the DMD. Recovery from a **PWR_FLOAT** input pin assertion requires either a DLPC410 logic reset or a complete power cycle.

8.4.2.7 DMD Idle Mode

When not powering down the DMD yet it is desired to place the system in an idle (non-functioning) state, regardless of end application, all DMDs benefit from continuously operating the DMD near 50% landed on/off duty cycle. This requires customers to understand how they can provide the DMD a sequence of patterns which approximate a 50/50 duty cycle without interfering with normal operation of their system. See section 3 (Duty Cycle Considerations) in application note [DLPA052 - System Design Considerations Using TI DLP® Technology down to 400 nm](#). Also see

- [DLPA060 - System Design Considerations Using TI DLP® Technology in UVA](#), and
 - [DLPA104 - DLP® High-Power NIR Thermal Design Guide](#)
- for additional information.

8.4.3 LOAD4 Functionality (enabled with DLPR410A)

The DLPR410A PROM enables a new LOAD4 feature for the DLPC410 and attached DMD. The LOAD4 capability enables the DMD to load 4 rows for every row of data provided by the DLPC410, thereby reducing the number of rows to be transferred to 1/4 of the total of DMD rows, and the pattern load time to 1/4 the total of row cycles, all at the expense of vertical resolution (1/4). Faster global binary pattern rates at the expense of vertical addressable resolution may make sense for certain applications like shutter/chopper solutions and vertical structured light patterns. LOAD4 reduces data load time only and does not reduce the “Mirror Clocking Pulse” and “Settling Time” durations.

8.4.3.1 Enabling LOAD4

LOAD4 is enabled by setting the DLPC410 input signal " $\overline{\text{LOAD4}}$ " to a logic '0'. When not using LOAD4, this input should be driven or pulled up to logic '1'.

NOTE

The $\overline{\text{LOAD4}}$ pin on the DLPC410 was previously defined as "DDC_SPARE_0" pin. DLPC410 reference schematics may still show this signal as DDC_SPARE_0 even though the DLPR410A enables the LOAD4 capability using this pin. LOAD4 capability is available starting with the DLPR410A and is not available with the DLPR410.

8.4.3.2 Loading Data with LOAD4

LOAD4 enables the attached DMD to load four rows of the same data for every one row of provided pattern data. “Automatic Increment” mode and “Row Address” mode can be used as before, however the largest addressable row will be the Vertical Resolution (VRes) of the attached DMD divided by four. For example, using LOAD4 the XGA DMD will have $1024/4 = 256$ addressable rows (0 . . . 255). The addressable vertical resolution is reduced by four, although the physical mirror resolution remains unchanged.

“Automatic Increment” address mode will automatically increment the Row Address input by one (or decrement by one for N/S flip). The Row Address input will be re-mapped as shown in the next section.

8.4.3.3 Row Mapping with LOAD4

The DMD row addresses are re-mapped per [Table 18](#).

Table 18. LOAD4 Row Address Mapping

| Row Address Input | Physical Rows loaded on DMD |
|-------------------|--------------------------------|
| 0 | 0, 1, 2, 3 |
| 1 | 4, 5, 6, 7 |
| 2 | 8, 9, 10, 11 |
| 3 | 12, 13, 14, 15 |
| ... | ... |
| N | 4N, 4N+1, 4N+2, 4N+3 |
| ... | ... |
| (VRes/4) -1 | VRes-4, VRes-3, VRes-2, VRes-1 |

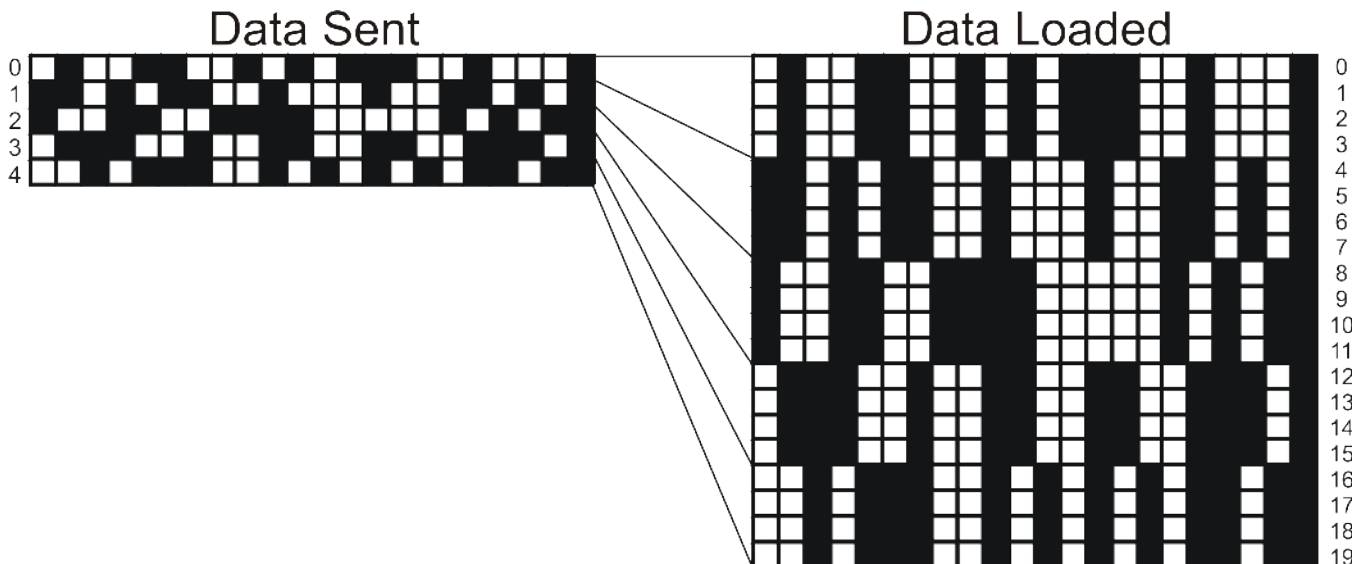


Figure 20. LOAD4 Row Address Mapping

8.4.3.4 Using Block Clear with LOAD4

While LOAD4 is enabled, Block Clear operations will be ignored. To use LOAD4 followed by Block Clear operations, simply de-assert LOAD4 at the beginning of the Reset request(s) preceding the Block Clear request(s). Re-assert LOAD4 at the beginning of the Reset request(s) preceding the next desired LOAD4 operation. This will ensure that the DLPC410 Controller has sufficient time to disable or enable LOAD4 before data is loaded or Block Clear(s) are requested.

8.4.3.5 Timing Requirements for LOAD4

LOAD4 functionality is primarily intended to be used with Global Resets. However, It is possible to use a subset of the DMD array including Block Resets. The driving software/hardware MUST ensure that the average “Reset” (MCP) rate does not exceed an average rate of 50,000 MCPs/sec as this is the specification limit of the [DLPA200 Micromirror Driver device](#). The driving software/hardware MUST also ensure that the “Mirror Settling Time” is not violated for any Block.

Average rate means averaged over 2-3 Load/Clear cycles. For example if a pattern is loaded and displayed with a Mirror Clocking Pulse followed by a Block Clear and a Mirror Clocking Pulse the “on” display time is very short. However, If the next pattern is loaded and displayed immediately, the average MCP rate may be exceeded, depending on the DMD and the number of Blocks in use. Therefore idle time must be added in the Load or Block Clear cycle to ensure an average MCP rate of 50,000 MCPs/sec or lower. Typically the smallest pattern display time is desired so that the time is added during the Load cycle rather than the Block Clear cycle so that the “off” time is extended, not the pattern display time.

8.4.3.6 Global Binary Pattern Rate increases using LOAD4

Table 19 shows the improvements in binary pattern rates for the DLPC410 supported DMDs when using LOAD4 enhanced functionality of the DLPR410A PROM. When using solid state illuminators (which can be switched on and off quickly), the illumination window is the period of time between when a solid state illuminator can be turned on after the micromirrors have settled to when the micromirrors start to transition to their next state (after the load and a Reset). This illumination window is typically equal to the DMD load time. When the DMD load time is long (without LOAD4) there is a longer allowed illumination window for the application. As one moves to using LOAD4 but yet keeps the illumination window unchanged, the illumination window becomes a higher percentage of pattern period, and more the limiter of the maximum binary pattern rate.

Table 19. DMD Block Load Time at 400MHz DMD Clock

| DMD | Global Frame Rate (without LOAD4) | Global Frame Rate (with LOAD4 mode) |
|------------|--------------------------------------|--|
| DLP650LNIR | 11k binary patterns/sec | 30k binary patterns/sec |
| DLP7000 | 23k binary patterns/sec | 48k binary patterns/sec |
| DLP9500 | 18k binary patterns/sec | 42k binary patterns/sec |

8.4.3.7 Special LOAD4 considerations

Take precautions when using LOAD4 mode with the DLP650LNIR DMD, or similar DMDs where the number of rows per reset block is not evenly divisible by 4. In the case of the DLP650LNIR, the number of rows per block for this DMD is 50 rows which is not evenly divisible by 4. Therefore, loading the last two rows of an even number block ($n = 0, 2, 4, \dots, 14$) concurrently loads the first two rows in the subsequent odd number block ($n+1$). Conversely, to address and load an odd block using LOAD4, the last two rows of the preceding even number block will be loaded first, else the first two rows of the odd block will not be loaded with new data.

8.5 Programming

The DLPC410 has no software interfaces and is therefore not programmable from a software perspective. All operational modes involve externally applied hardware signals.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV devices require they be coupled with the DLPC410 controller to provide a reliable solution for many different applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC410. Applications of interest include industrial, medical, and intelligent display.

9.1.1 Device Description

The DLPC410 Controller based chipsets offer developers a convenient way to design a wide variety of industrial, medical, and advanced display applications by delivering maximum flexibility in formatting and sequencing customer binary pattern data for display as projected light patterns from DMDs of varying resolutions.

These chipsets include the following components:

DLPC410 DMD Digital Controller

- Captures 2xLVDS input pattern data plus control from the user.
- Provides data and additional control to the DMD for high speed binary pattern display.
- Commands the DLPA200 to generate Resets Pulses (MCP) with highly specific timing.
- Supports random DMD row addressing, clear operations, and LOAD4 capability.

DLPR410 Configuration PROM

- Contains DLPC410 Controller power up configuration information.

DLPA200 DMD Micromirror Driver

- Creates Reset Pulses (MCP) to the DMD to initiate mirror transitions to the next state.

DMD: Digital Micromirror Device, a 2-dimensional array of aluminum micromirrors

- DMD micromirrors tilt +12 degrees and -12 degrees to steer light in one of two directions.
- DLP650LNIR DMD: 0.65-inch array diagonal, 1280 x 800 micromirror array, WXGA resolution.
- DLP7000(UV) DMDs: 0.7-inch array diagonal, 1024 x 768 micromirror array, XGA resolution.
- DLP9500(UV) DMDs: 0.95-inch array diagonal, 1920 x 1080 micromirror array, 1080p resolution.

Reliable function and operation of the DLP650LNIR, DLP7000, DLP7000UV, DLP9500, and DLP9500UV DMDs require the DMDs to be used in conjunction with the components listed in [Table 1](#). This document describes the proper integration and use of the chipset components.

The DLPC410 chipset can be combined with a user programmable Application FPGA (not included) to create high performance systems.

9.2 Typical Application

A typical embedded system application using the DLPC410 controller is shown in [Figure 21](#). The DLPC410, the DMD, and their associated DLP components do not specifically determine the application in which the components are used - customer applications and use cases may vary widely, from Digital Image Lithography to 3D Printing to 3D Scanners using Structured Light. The DMD is capable of being used with multiple illumination source types, from Lasers and LEDs to wide band wavelength mercury halide lamps. The DLPC410 supported DMDs cover applications utilizing ultraviolet (UV), visible, and/or near-infrared (NIR) wavelengths. The duration of each binary pattern displayed on the DMD is totally under control of the Applications Processor. The displayed patterns could be strictly binary patterns or could be bit weight exposures of varying durations representing

Typical Application (continued)

encoded PWM-based gray scales. The timing of the micromirrors and the illumination sources are controlled at the discretion of a Customer Applications Processor and in many solid state cases, provide best performance when source illuminators are synchronous to the commanded DMD micromirror transitions. The speed, diversity, programmability, and flexibility of the DLPC410 building blocks provide an electro-optical cornerstone for customers to build upon to create applications limited only by customer ingenuity.

In **Figure 21**, the MBRST 2 signals and the C, D LVDS Data buses are shown with dashed lines to indicate that some DMDs do not require these signals to be used. TI's Reference Design and Evaluation Modules leverage a DLPC410 Controller Board which supports all 5 of the DLPC410 supported DMDs. The performance differences for each application are determined by which DMD Board is plugged into the Controller Board. This provides a single DLPC410 design platform which can then be used for multiple customer SKUs within an application platform for product segmentation purposes.

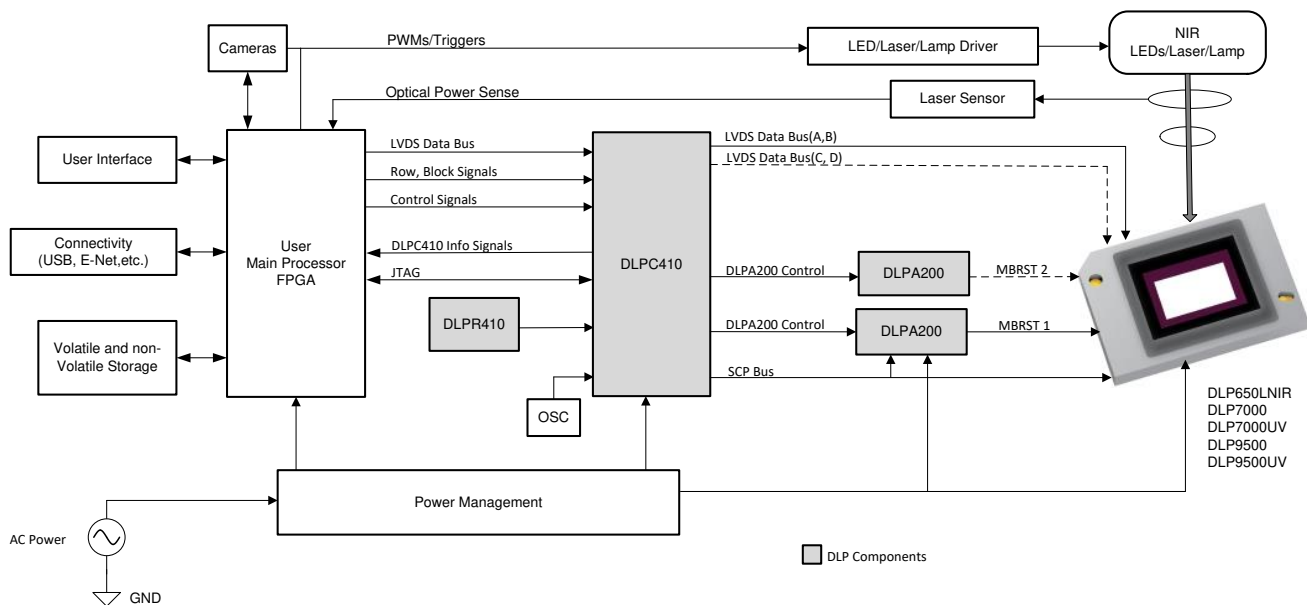


Figure 21. DLPC410 Application Example Block Diagram

9.2.1 Design Requirements

All applications using the DLP650LNIR, DLP7000(UV) or DLP9500(UV) DMDs require the DLPC410 Controller, DLPR410 PROM, and one or two DLPA200 Micromirror Drivers for proper operation. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry for the DLPC410 are required:

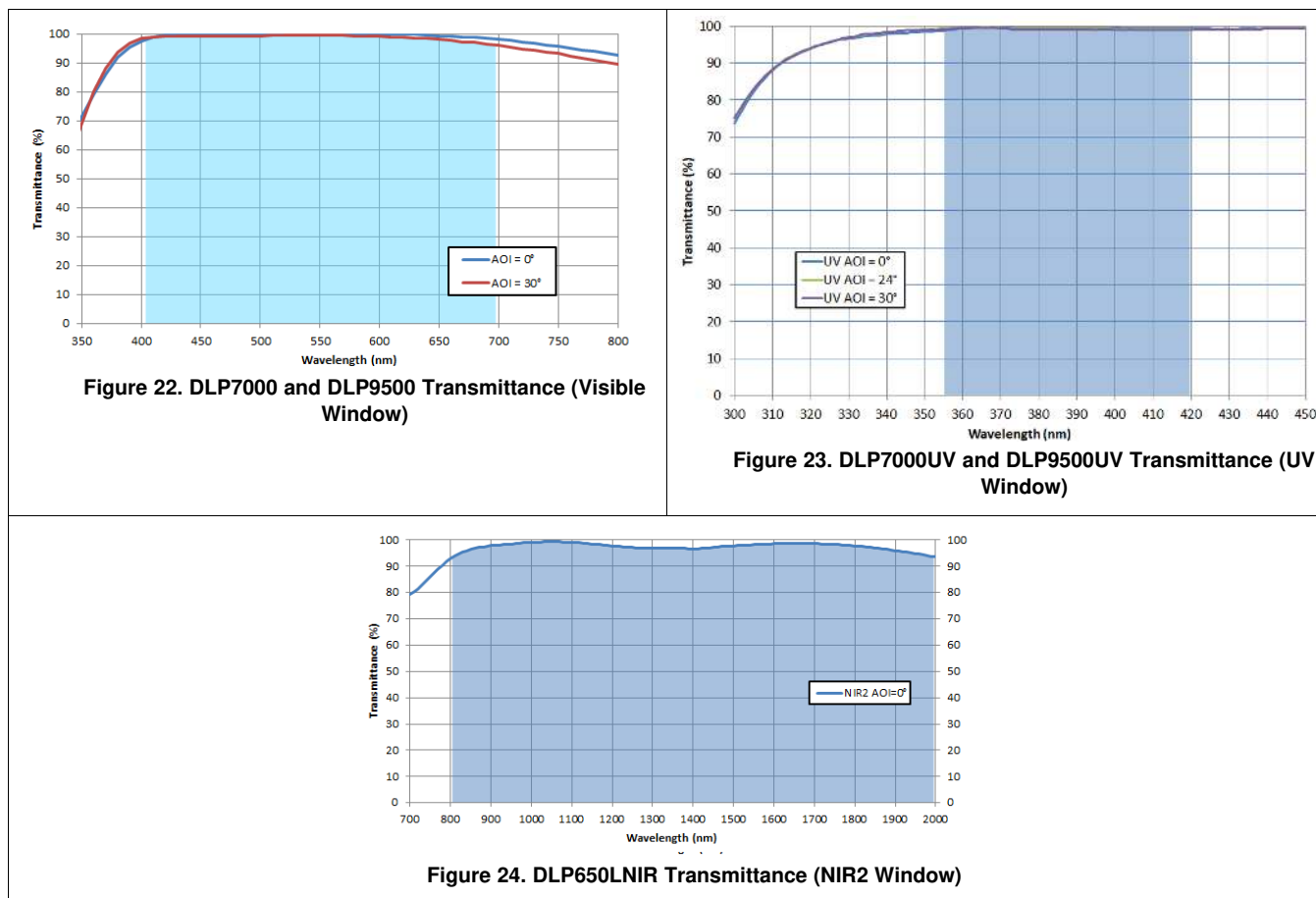
- DLPC410 Application System Interfaces to the customer electronics and software:
 - Input LVDS Data Buses A, B, C, D
 - Row Address to specify DMD row to load
 - Block address and Block Mode to specify which DMD block(s) to "Reset" (MCP)
 - RST_ACTIVE feedback to indicated a "Reset" is in progress
 - Miscellaneous control inputs
 - Miscellaneous feedback signals
 - Power Supply inputs
- DLPC410 to other DLP Component Interfaces
 - Output LVDS Data Buses A, B, C, D to DMD
 - Output control signals (SCP bus) to DMD
 - Output commands to DLPA200 for MCP generation

Typical Application (continued)

9.2.2 Detailed Design Procedure

The DLP7000 and DLP9500 DMD are designed to be operated by the DLPC410 controller and are well suited for visible light applications requiring fast, spatially programmable light patterns using the micromirror array. In addition the DLP7000UV and DLP9500UV are well suited for direct imaging lithography, 3D printing applications, and other applications requiring ultraviolet light (UVA). The DLP650LNIR DMD is optimal for high power Near-Infrared light (NIR) applications like 3D additive manufacturing (SLS), marking and coding, and FPD repair and ablation. Refer to the [Functional Block Diagrams](#) to investigate the connections between the DLP650LNIR, DLP7000 / DLP7000UV or DLP9500 / DLP9500UV DMD, the DLPC410 digital controller, the DLPR410 Configuration PROM, and the DLPA200 DMD micromirror drivers. Layout guidelines should be followed for reliability.

9.2.3 Application Curves



9.3 Initialization Setup

9.3.1 Debugging Guidelines

Prior to checking the DLPC410 output signals, make sure the reference clock to the DLPC410 is running at 50 MHz. Check that DONE_DDC (pin K10) signal is asserted and ECP2_Finished is de-asserted indicating the DLPR410 PROM has correctly programmed the DLPC410 Controller and the DLPC410 is running.

9.3.2 Initialization

Initialization will automatically start after $\overline{\text{ARST}}$ (pin AC13) is released (transition to '1'). The initialization process includes the following components:

Initialization Setup (continued)

1. Input Data Bus Calibration
2. DLPA200 Initialization Step 1
3. DMD Initialization
4. DLPA200 Initialization Step 2
5. Command Sequence

9.3.2.1 Input Data Bus Calibration

Calibration of the DLPC410 2xLVDS input data buses is performed on each of the data (DDC_DIN) and DVALID signal pairs of all input buses using the training pattern as specified in [Input Data Interface \(DIN\) Training](#). When this calibration is successful, the System Initialization process will move on to initializing the DLPA200 devices.

NOTE

The training pattern going into the SERDES on the transmit side is different than the pattern on the receive SERDES. On the receive side the value should be "0100". However, this could translate to "0010" on the transmit side. Please see [Input Data Interface \(DIN\) Training](#) for more information. An improper training pattern could cause the part to not perform the commands correctly.

9.3.2.2 DLPA200 Initialization Step 1

The DLPC410 will partially initialize both DLPA200 devices (1 and 2) such that all voltages to the DMD are at their proper initial state. The DLPC410 outputs $\overline{\text{DAD_A_SCPEN}}$ (pin AE3) and $\overline{\text{DAD_B_SCPEN}}$ (pin AB19) will assert indicating that the DLPC410 is ready to communicate with the DLPA200 devices. Signaling should be seen on SCPCLK (pin AB15), SCPDO (pin AA15 - SCP data output from the DLPC410) and SCPDI (pin AA15 - SCP data input to the DLPC410). During layout, ensure that the direction of the SCP data input and output signals are connected correctly.

9.3.2.3 DMD Initialization

During DMD initialization, the DLPC410 output $\overline{\text{DMD_A_SCPEN}}$ (pin AB14) signal will assert indicating that the DLPC410 is ready to communicate to the DMD. Signaling can be seen on SCPCLK (pin AB15), SCPDO (pin AA15 - SCP output from the DLPC410) and SCPDI (pin AA15 - SCP input to the DLPC410) lines. During layout, ensure that the direction of the SCP input and output signals are connected correctly.

9.3.2.3.1 DMD Device ID Check

If the DLPC410 has successfully initialized the DMD, the four DMD_TYPE(3:0) output pins (AA17, AC16, AB17, and AD15) of the DLPC410 will provide the DMD type as identified from the DMD during its initialization process. The possible DMD_TYPE values are shown in [Table 15](#). DMD_TYPE(3:0) will return "1111" if the DMD is not recognized, not attached, or if the DLPC910 is unable to communicate with the DMD.

NOTE

Only the DMDs listed in [Table 1](#) and [Table 15](#) are supported by the DLPC410. The DLPC410 will not function for unsupported DMDs or when a DMD is not installed.

9.3.2.4 DLPA200 Initialization Step 2

Now that the DMD ID has been assessed by the DLPC410, the Controller will finish the DLPA200 initialization to set the DLPA200 voltages to their final operating settings for the specific connected DMD. The DLPC410 outputs $\overline{\text{DAD_A_SCPEN}}$ (pin AE3) and $\overline{\text{DAD_B_SCPEN}}$ (pin AB19) will assert indicating that the DLPC410 is ready to communicate with the DLPA200 devices. Signaling should be seen on SCPCLK (pin AB15), SCPDO (pin AA15 - SCP data output from the DLPC410) and SCPDI (pin AA15 - SCP data input to the DLPC410). During layout, ensure that the direction of the SCP data input and output signals are connected correctly.

Initialization Setup (continued)

When DLPA200 initialization is complete, check V_{BIAS} , V_{RESET} , and V_{OFFSET} voltage values on both DLPA200 devices and compare against the DLPA200 data sheet specification and the DMD data sheet specification for the DMD connected to the DLPC410.

9.3.2.5 Command Sequence Initialization

The last portion of the initialization process involves a series of commands sent from the DLPC410 to the DMD. During this step, check the output pins (OUT[15:0]) of the DLPA200(s). One should expect to see several Mirror Clocking Pulse waveforms indicating the DLPA200s are initialized correctly.

This will complete the initialization process. When the initialization process starts, the INIT_ACTIVE output signal (pin AA18) will assert (go high) indicating that the initialization sequence is in process. At the end of the initialization sequence, if the initialization is successful, the INIT_ACTIVE output signal (pin AA18) will deassert (go low) indicating that the initialization process is complete.

NOTE

Initialization complete indicates that the initialization sequence of the DLPC410 has completed, but does not ensure that each step was completed correctly, only that it finished. For example the initialization of a DLPA200 may complete, but if the voltages set are incorrect further investigation is needed to uncover the reason.

9.3.3 Image Display Issues

There are three steps to displaying an image on the DMD, each of which can cause an image to fail to display correctly or in some case not at all. These steps are:

1. Present Data to DLPC410 – Pattern data generated by the user's device.
2. Load Data to the DMD – The DLPC410 loads data into the attached DMD CMOS memory array.
3. Issue Reset (MCP) – A Reset pulse (MCP) is issued to block(s) to change the state of the micromirrors based on the data loaded in step two. See [Mirror Clocking Pulse \(MCP\)](#).

9.3.3.1 Present Data to DLPC410

If there is a problem with the image displayed, one of the first places to check is the data being presented to the DLPC410. This data is generated by customer application hardware/software and is then presented to the inputs of the DLPC410. If the data is formatted incorrectly or the control information is incorrect, the DLPC410 may not properly receive the data. Please see [Row Addressing](#) for a description of how to send data to the DLPC410.

9.3.3.2 Load Data to DMD

After data and commands are sent to the DLPC410, the DLPC410 processes the information and passes it to the DMD. If there is no image displayed, first check the data output and SCTRL lines of the DLPC410 to see if there is data coming out. Data output (DDC_DOUT...) and DDC_SCTRL pins can be found in the [Pin Configuration and Functions](#).

PWR_FLOAT (pin AC17) will prevent the data from coming out of the DLPC410 if asserted. Check to make sure that it is at logic level 0.

A *Float blocks 00-15* command will also prevent data from the DLPC410. Please see the last entry of [Table 14](#).

9.3.3.3 Mirror Clocking Pulse

For a new image to appear on the DMD, Mirror Clocking Pulses must be received for the DMD block or blocks that have received new data. Check DAD_A_STROBE (pin AF3) and DAD_B_STROBE (pin AB20) [if applicable] for pulses to verify that requests for mirror clocking pulses are being sent to the DLPA200(s). Also check the DLPA200(s) output is enabled by checking that $\overline{DAD_OE}$ (pin AF5) is low.

10 Power Supply Recommendations

10.1 Power Down Operation

For correct operation of the DMD, the following power down procedure must be executed. Prior to power removal, assert PWR_FLOAT and allow approximately 300 μ s for the procedure to complete. This procedure will assure the mirrors are in a flat state, similar to the float operation. Following this procedure, the power can be safely removed.

To restart after assertion of PWR_FLOAT the DLPC410 must be reset ($\overline{\text{ARST}}$ low then high) or power must be cycled.

11 Layout

11.1 Layout Guidelines

The DLPC410 is part of a chipset that controls a DLP650LNIR, DLP7000 / DLP7000UV or DLP9500 / DLP9500UV DMD in conjunction with the DLPA200 driver(s). These guidelines are targeted at designing a PCB board with these components.

11.1.1 Impedance Requirements

Signals should be routed to have a matched impedance of 50 $\Omega \pm 10\%$ except for LVDS differential pairs (DMD_DAT_Xnn, DMD_DCKL_Xn, and DMD_SCTRL_Xn), which should be matched to 100 $\Omega \pm 10\%$ across each pair.

11.1.2 PCB Signal Routing

When designing a PCB board for the DLP650LNIR, DLPC7000 / DLP7000UV or DLP9500 / DLP9500UV controlled by the DLPC410 in conjunction with the DLPA200(s), the following are recommended:

Signal trace corners should be no sharper than 45°. Adjacent signal layers should have the predominate traces routed orthogonal to each other. TI recommends that critical signals be hand routed in the following order: DDR2 Memory, DMD (LVDS signals), then DLPA200 signals.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

High speed signal traces should not cross over slots in adjacent power and/or ground planes.

Table 20. Important Signal Trace Constraints

| SIGNAL | CONSTRAINTS |
|---|--|
| LVDS (DMD_DAT_xnn, DMD_DCKL_xn, and DMD_SCTRL_xn) | P-to-N data, clock, and SCTRL: <10 mils (0.25 mm); Pair-to-pair <10 mils (0.25 mm); Bundle-to-bundle <2000 mils (50 mm, for example DMD_DAT_Ann to DMD_DAT_Bnn) Trace width: 4 mil (0.1 mm) Trace spacing: In ball field – 4 mil (0.11 mm); PCB etch – 14 mil (0.36 mm) Maximum recommended trace length <6 inches (150 mm) |

Table 21. Power Trace Widths and Spacing

| SIGNAL NAME | MINIMUM TRACE WIDTH | MINIMUM TRACE SPACING | LAYOUT REQUIREMENTS |
|--------------|-------------------------------|-----------------------|---|
| GND | Maximize | 5 mil (0.13 mm) | Maximize trace width to connecting pin as a minimum |
| P2P5V, P1P0V | 50 mil (1.3 mm) | 10 mil (0.25 mm) | Create mini planes and connect to devices as necessary with multiple vias |
| P2P5V, P1P0V | 30 mil (0.76 mm) - stub width | 10 mil (0.25 mm) | Stub width to connecting IC pins; maximize width when possible |

11.1.3 Fiducials

Fiducials for automatic component insertion should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

11.1.4 PCB Layout Guidelines

A target impedance of 50 Ω for single ended signals and 100 Ω between LVDS signals (P/N) is specified for all signal layers.

11.1.4.1 DMD Interface

The digital interface from the DLPC410 to the DMD are LVDS signals that run at clock rates up to 400 MHz. DDR Data is clocked into the DMD on both the rising and falling edge of the clock, so the data rate is 800 MHz. The LVDS signals should have 100- Ω differential impedance. The differential signals should be matched but kept as short as possible. Parallel termination at the LVDS receiver is in the DMD; therefore, on board termination is not necessary.

11.1.4.1.1 Trace Length Matching

The require precise length matching. LVDS data bus differential pairs should have an impedance of 100 Ω (with 5% tolerance). It is important that the propagation delays are matched. The maximum differential pair uncoupled length is 150 mils with a relative propagation delay of ± 25 mil between the p and n. Matching all signals exactly will maximize the channel margin. The signal path through all boards, flex cables and internal DMD routing must be considered in this calculation.

11.1.4.2 DLPC410 DMD Decoupling

General decoupling capacitors for the DMD should be distributed around the PCB and placed to minimize the distance from IC voltage and ground pads. Each decoupling capacitor (0.1 μ F recommended) should have vias directly to the ground and power planes. Via sharing between components (discreet or integrated) is discouraged. The power and ground pads of the DMD should be tied to the voltage and ground planes with their own vias.

11.1.4.2.1 Decoupling Capacitors

Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. It is recommended that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

11.1.4.3 VCC and VCC2

The VCC pins of the DMD should be connected directly to the DMD VCC plane. Decoupling for the VCC should be distributed around the DMD and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor should have vias directly connected to the ground and power planes. The VCC and GND pads of the DMD should be tied to the VCC and ground planes with their own vias.

The VCC2 voltage can be routed to the DMD as a trace. Decoupling capacitors should be placed to minimize the distance from the VCC2 and ground pads of the DMD. Using wide etch from the decoupling capacitors to the DMD connection will reduce inductance and improve decoupling performance.

11.1.4.4 DMD Layout

See the respective sections in this data sheet for package dimensions, timing and pin out information.

11.1.4.5 DLPA200

The DLPA200 generates the micromirror clocking pulses for the DMD. The DMD-drive outputs from the DLPA200 should be routed with minimum trace width of 11 mil and a minimum spacing of 15 mil. The VCC and VCC2 traces from the output capacitors to the DLPA200 should also be routed with a minimum trace width and spacing of 11 mil and 15 mil, respectively. See the DLPA200 customer data sheet for mechanical package and layout information.

11.2 Layout Example

For LVDS (and other differential signal) pairs and groups, it is important to match trace lengths. In the area of the dashed lines, [Figure 25](#) shows correct matching of signal pair lengths with serpentine sections to maintain the correct impedance.

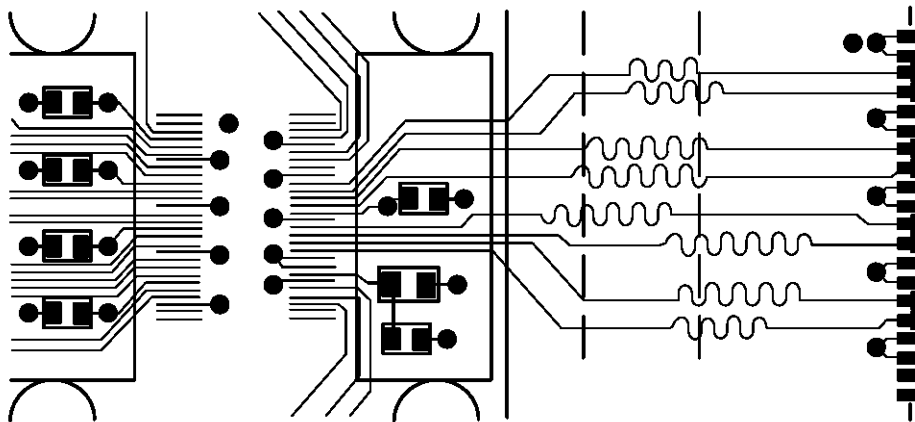


Figure 25. Mitering LVDS Traces to Match Lengths

11.3 DLPC410 Chipset Connections

The following tables list the signal connections between components of the Chipset when used with the DLP650LNIR DMD, the DLP7000 / DLP700UV DMD, and with the DLP9500 / DLP9500UV DMD. These tables do not include power, ground, pull-up, pull-down, termination, or any other connection requirements. Please see the Pin Functions table in the respective data sheet of each chipset component for connection requirements.

Table 22. DLPC410 Chipset Connections with the DLP650LNIR

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 (MICROMIRROR DRIVER) | | DLP650LNIR (DMD) | |
|----------------------------|------|-----------------------|-----|------------------------------|-----|--------------------|------|
| PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DONE_DDC | K10 | \overline{CE} | B4 | | | | |
| INTB_DDC | J11 | OE/\overline{RESET} | A3 | | | | |
| PROGB_DDC | J18 | \overline{CF} | D1 | | | | |
| PROM_CCK_DDC | J10 | CLKOUT | C2 | | | | |
| PROM_D0_DDC | K11 | D0 | H6 | | | | |
| TCK_JTAG | U11 | TCK | H3 | | | | |
| TDO_XCF16DDC | V11 | TDO | E6 | | | | |
| TMS_JTAG | V12 | TMS | E2 | | | | |
| DAD_A_ADDR0 | E1 | | | ADDR0 | 19 | | |
| DAD_A_ADDR1 | E2 | | | ADDR1 | 18 | | |
| DAD_A_ADDR2 | E3 | | | ADDR2 | 17 | | |
| DAD_A_ADDR3 | F3 | | | ADDR3 | 16 | | |
| DAD_A_MODE0 | C1 | | | MODE0 | 3 | | |
| DAD_A_MODE1 | D1 | | | MODE1 | 2 | | |
| DAD_A_SEL0 | AB12 | | | SEL0 | 5 | | |
| DAD_A_SEL1 | AC12 | | | SEL1 | 4 | | |
| DAD_A_STROBE | AF3 | | | STROBE | 15 | | |
| DAD_INIT | AF4 | | | \overline{RESET} | 59 | | |
| $\overline{DAD_OE}$ | AF5 | | | \overline{OE} | 6 | | |
| $\overline{DAD_A_SCPEN}$ | AE3 | | | \overline{SCPEN} | 58 | | |
| SCPCLK | AB15 | | | SCPCLK | 56 | SCPCLK | E3 |
| SCPDI | AA15 | | | SCPDO | 57 | SCPDO | B2 |
| SCPDO | AA14 | | | SCPDI | 42 | SCPDI | F4 |
| $\overline{DMD_A_SCPEN}$ | AB14 | | | | | \overline{SCPEN} | D4 |
| DMD_A_RESET | AD14 | | | | | \overline{PWRDN} | C3 |
| DDC_DCLKOUT_A_DPN | N1 | | | | | DCLK_AN | B22 |
| DDC_DCLKOUT_A_DPP | M1 | | | | | DCLK_AP | B24 |
| DDC_DCLKOUT_B_DPN | Y5 | | | | | DCLK_BN | AB22 |
| DDC_DCLKOUT_B_DPP | Y6 | | | | | DCLK_BP | AB24 |
| DDC_DOUT_A1_DPN | AD1 | | | | | D_AN(1) | A13 |
| DDC_DOUT_A1_DPP | AE1 | | | | | D_AP(1) | A11 |
| DDC_DOUT_A3_DPN | AB1 | | | | | D_AN(3) | C17 |
| DDC_DOUT_A3_DPP | AB2 | | | | | D_AP(3) | C15 |
| DDC_DOUT_A5_DPN | W1 | | | | | D_AN(5) | A17 |
| DDC_DOUT_A5_DPP | Y1 | | | | | D_AP(5) | A19 |
| DDC_DOUT_A7_DPN | U1 | | | | | D_AN(7) | D22 |
| DDC_DOUT_A7_DPP | U2 | | | | | D_AP(7) | D20 |
| DDC_DOUT_A9_DPN | N2 | | | | | D_AN(9) | D28 |
| DDC_DOUT_A9_DPP | M2 | | | | | D_AP(9) | B28 |

DLPC410 Chipset Connections (continued)
Table 22. DLPC410 Chipset Connections with the DLP650LNIR (continued)

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 (MICROMIRROR DRIVER) | | DLP650LNIR (DMD) | |
|----------------------|-----|----------------|-----|------------------------------|-----|------------------|------|
| PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DDC_DOUT_A11_DPN | K2 | | | | | D_AN(11) | F26 |
| DDC_DOUT_A11_DPP | K3 | | | | | D_AP(11) | D26 |
| DDC_DOUT_A13_DPN | H2 | | | | | D_AN(13) | H28 |
| DDC_DOUT_A13_DPP | J1 | | | | | D_AP(13) | H30 |
| DDC_DOUT_A15_DPN | G2 | | | | | D_AN(15) | K26 |
| DDC_DOUT_A15_DPP | F2 | | | | | D_AP(15) | K28 |
| DDC_DOUT_B1_DPN | AD3 | | | | | D_BN(1) | AC13 |
| DDC_DOUT_B1_DPP | AD4 | | | | | D_BP(1) | AC11 |
| DDC_DOUT_B3_DPN | AC3 | | | | | D_BN(3) | AA17 |
| DDC_DOUT_B3_DPP | AC4 | | | | | D_BP(3) | AA15 |
| DDC_DOUT_B5_DPN | AB7 | | | | | D_BN(5) | AC17 |
| DDC_DOUT_B5_DPP | AC6 | | | | | D_BP(5) | AC19 |
| DDC_DOUT_B7_DPN | AA7 | | | | | D_BN(7) | Y22 |
| DDC_DOUT_B7_DPP | Y7 | | | | | D_BP(7) | Y20 |
| DDC_DOUT_B9_DPN | W4 | | | | | D_BN(9) | Y28 |
| DDC_DOUT_B9_DPP | V4 | | | | | D_BP(9) | AB28 |
| DDC_DOUT_B11_DPN | V7 | | | | | D_BN(11) | V26 |
| DDC_DOUT_B11_DPP | V6 | | | | | D_BP(11) | Y26 |
| DDC_DOUT_B13_DPN | T4 | | | | | D_BN(13) | R29 |
| DDC_DOUT_B13_DPP | T5 | | | | | D_BP(13) | T28 |
| DDC_DOUT_B15_DPN | U7 | | | | | D_BN(15) | N27 |
| DDC_DOUT_B15_DPP | T7 | | | | | D_BP(15) | P26 |
| DDC_SCTRL_AN | R1 | | | | | SCTRL_AN | C21 |
| DDC_SCTRL_AP | P1 | | | | | SCTRL_AP | C23 |
| DDC_SCTRL_BN | AA3 | | | | | SCTRL_BN | AA21 |
| DDC_SCTRL_BP | AB4 | | | | | SCTRL_BP | AA23 |

Table 23. DLPC410 Chipset Connections with the DLP7000

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 (MICROMIRROR DRIVER) | | DLP7000 / UV (DMD) | |
|----------------------|-----|-----------------------|-----|------------------------------|-----|--------------------|-----|
| PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DONE_DDC | K10 | \overline{CE} | B4 | | | | |
| INTB_DDC | J11 | $\overline{OE/RESET}$ | A3 | | | | |
| PROGB_DDC | J18 | \overline{CF} | D1 | | | | |
| PROM_CCK_DDC | J10 | CLKOUT | C2 | | | | |
| PROM_D0_DDC | K11 | D0 | H6 | | | | |
| TCK_JTAG | U11 | TCK | H3 | | | | |
| TDO_XCF16DDC | V11 | TDO | E6 | | | | |
| TMS_JTAG | V12 | TMS | E2 | | | | |
| DAD_A_ADDR0 | E1 | | | ADDR0 | 19 | | |
| DAD_A_ADDR1 | E2 | | | ADDR1 | 18 | | |
| DAD_A_ADDR2 | E3 | | | ADDR2 | 17 | | |

Table 23. DLPC410 Chipset Connections with the DLP7000 (continued)

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 (MICROMIRROR DRIVER) | | DLP7000 / UV (DMD) | |
|-----------------------------------|------|----------------|-----|------------------------------|-----|---------------------------|------|
| PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DAD_A_ADDR3 | F3 | | | ADDR3 | 16 | | |
| DAD_A_MODE0 | C1 | | | MODE0 | 3 | | |
| DAD_A_MODE1 | D1 | | | MODE1 | 2 | | |
| DAD_A_SEL0 | AB12 | | | SEL0 | 5 | | |
| DAD_A_SEL1 | AC12 | | | SEL1 | 4 | | |
| DAD_A_STROBE | AF3 | | | STROBE | 15 | | |
| DAD_INIT | AF4 | | | $\overline{\text{RESET}}$ | 59 | | |
| $\overline{\text{DAD_OE}}$ | AF5 | | | $\overline{\text{OE}}$ | 6 | | |
| $\overline{\text{DAD_A_SCPEN}}$ | AE3 | | | $\overline{\text{SCPEN}}$ | 58 | | |
| SCPCLK | AB15 | | | SCPCLK | 56 | SCPCLK | E3 |
| SCPDI | AA15 | | | SCPDO | 57 | SCPDO | B2 |
| SCPDO | AA14 | | | SCPDI | 42 | SCPDI | F4 |
| $\overline{\text{DMD_A_SCPEN}}$ | AB14 | | | | | $\overline{\text{SCPEN}}$ | D4 |
| DMD_A_RESET | AD14 | | | | | $\overline{\text{PWRDN}}$ | C3 |
| DDC_DCLKOUT_A_DPN | N1 | | | | | DCLK_AN | B22 |
| DDC_DCLKOUT_A_DPP | M1 | | | | | DCLK_AP | B24 |
| DDC_DCLKOUT_B_DPN | Y5 | | | | | DCLK_BN | AB22 |
| DDC_DCLKOUT_B_DPP | Y6 | | | | | DCLK_BP | AB24 |
| DDC_DOUT_A0_DPN | AE2 | | | | | D_AN(0) | B10 |
| DDC_DOUT_A0_DPP | AF2 | | | | | D_AP(0) | B12 |
| DDC_DOUT_A1_DPN | AD1 | | | | | D_AN(1) | A13 |
| DDC_DOUT_A1_DPP | AE1 | | | | | D_AP(1) | A11 |
| DDC_DOUT_A2_DPN | AC1 | | | | | D_AN(2) | D16 |
| DDC_DOUT_A2_DPP | AC2 | | | | | D_AP(2) | D14 |
| DDC_DOUT_A3_DPN | AB1 | | | | | D_AN(3) | C17 |
| DDC_DOUT_A3_DPP | AB2 | | | | | D_AP(3) | C15 |
| DDC_DOUT_A4_DPN | Y2 | | | | | D_AN(4) | B18 |
| DDC_DOUT_A4_DPP | AA2 | | | | | D_AP(4) | B16 |
| DDC_DOUT_A5_DPN | W1 | | | | | D_AN(5) | A17 |
| DDC_DOUT_A5_DPP | Y1 | | | | | D_AP(5) | A19 |
| DDC_DOUT_A6_DPN | V1 | | | | | D_AN(6) | A25 |
| DDC_DOUT_A6_DPP | V2 | | | | | D_AP(6) | A23 |
| DDC_DOUT_A7_DPN | U1 | | | | | D_AN(7) | D22 |
| DDC_DOUT_A7_DPP | U2 | | | | | D_AP(7) | D20 |
| DDC_DOUT_A8_DPN | R2 | | | | | D_AN(8) | C29 |
| DDC_DOUT_A8_DPP | T2 | | | | | D_AP(8) | A29 |
| DDC_DOUT_A9_DPN | N2 | | | | | D_AN(9) | D28 |
| DDC_DOUT_A9_DPP | M2 | | | | | D_AP(9) | B28 |
| DDC_DOUT_A10_DPN | K1 | | | | | D_AN(10) | E27 |
| DDC_DOUT_A10_DPP | L2 | | | | | D_AP(10) | C27 |
| DDC_DOUT_A11_DPN | K2 | | | | | D_AN(11) | F26 |
| DDC_DOUT_A11_DPP | K3 | | | | | D_AP(11) | D26 |
| DDC_DOUT_A12_DPN | J3 | | | | | D_AN(12) | G29 |
| DDC_DOUT_A12_DPP | H3 | | | | | D_AP(12) | F30 |
| DDC_DOUT_A13_DPN | H2 | | | | | D_AN(13) | H28 |

Table 23. DLPC410 Chipset Connections with the DLP7000 (continued)

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 (MICROMIRROR DRIVER) | | DLP7000 / UV (DMD) | |
|----------------------|-----|----------------|-----|------------------------------|-----|--------------------|------|
| PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DDC_DOUT_A13_DPP | J1 | | | | | D_AP(13) | H30 |
| DDC_DOUT_A14_DPN | H1 | | | | | D_AN(14) | J27 |
| DDC_DOUT_A14_DPP | G1 | | | | | D_AP(14) | J29 |
| DDC_DOUT_A15_DPN | G2 | | | | | D_AN(15) | K26 |
| DDC_DOUT_A15_DPP | F2 | | | | | D_AP(15) | K28 |
| DDC_DOUT_B0_DPN | AE5 | | | | | D_BN(0) | AB10 |
| DDC_DOUT_B0_DPP | AE6 | | | | | D_BP(0) | AB12 |
| DDC_DOUT_B1_DPN | AD3 | | | | | D_BN(1) | AC13 |
| DDC_DOUT_B1_DPP | AD4 | | | | | D_BP(1) | AC11 |
| DDC_DOUT_B2_DPN | AD5 | | | | | D_BN(2) | Y16 |
| DDC_DOUT_B2_DPP | AD6 | | | | | D_BP(2) | Y14 |
| DDC_DOUT_B3_DPN | AC3 | | | | | D_BN(3) | AA17 |
| DDC_DOUT_B3_DPP | AC4 | | | | | D_BP(3) | AA15 |
| DDC_DOUT_B4_DPN | AB5 | | | | | D_BN(4) | AB18 |
| DDC_DOUT_B4_DPP | AB6 | | | | | D_BP(4) | AB16 |
| DDC_DOUT_B5_DPN | AB7 | | | | | D_BN(5) | AC17 |
| DDC_DOUT_B5_DPP | AC6 | | | | | D_BP(5) | AC19 |
| DDC_DOUT_B6_DPN | AA5 | | | | | D_BN(6) | AC25 |
| DDC_DOUT_B6_DPP | AA4 | | | | | D_BP(6) | AC23 |
| DDC_DOUT_B7_DPN | AA7 | | | | | D_BN(7) | Y22 |
| DDC_DOUT_B7_DPP | Y7 | | | | | D_BP(7) | Y20 |
| DDC_DOUT_B8_DPN | Y3 | | | | | D_BN(8) | AA29 |
| DDC_DOUT_B8_DPP | W3 | | | | | D_BP(8) | AC29 |
| DDC_DOUT_B9_DPN | W4 | | | | | D_BN(9) | Y28 |
| DDC_DOUT_B9_DPP | V4 | | | | | D_BP(9) | AB28 |
| DDC_DOUT_B10_DPN | W6 | | | | | D_BN(10) | W27 |
| DDC_DOUT_B10_DPP | W5 | | | | | D_BP(10) | AA27 |
| DDC_DOUT_B11_DPN | V7 | | | | | D_BN(11) | V26 |
| DDC_DOUT_B11_DPP | V6 | | | | | D_BP(11) | Y26 |
| DDC_DOUT_B12_DPN | U4 | | | | | D_BN(12) | T30 |
| DDC_DOUT_B12_DPP | V3 | | | | | D_BP(12) | U29 |
| DDC_DOUT_B13_DPN | T4 | | | | | D_BN(13) | R29 |
| DDC_DOUT_B13_DPP | T5 | | | | | D_BP(13) | T28 |
| DDC_DOUT_B14_DPN | U6 | | | | | D_BN(14) | R27 |
| DDC_DOUT_B14_DPP | U5 | | | | | D_BP(14) | P28 |
| DDC_DOUT_B15_DPN | U7 | | | | | D_BN(15) | N27 |
| DDC_DOUT_B15_DPP | T7 | | | | | D_BP(15) | P26 |
| DDC_SCTRL_AN | R1 | | | | | SCTRL_AN | C21 |
| DDC_SCTRL_AP | P1 | | | | | SCTRL_AP | C23 |
| DDC_SCTRL_BN | AA3 | | | | | SCTRL_BN | AA21 |
| DDC_SCTRL_BP | AB4 | | | | | SCTRL_BP | AA23 |

Table 24. DLPC410 Chipset Connections with the DLP9500

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 Number 1 (MICROMIRROR DRIVER) | | DLPA200 Number 2 (MICROMIRROR DRIVER) | | DLP9500 or UV (DMD) | |
|----------------------------|------|-----------------------|-----|--|-----|--|-----|------------------------|------|
| PIN | | PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DONE_DDC | K10 | \overline{CE} | B4 | | | | | | |
| INTB_DDC | J11 | OE/\overline{RESET} | A3 | | | | | | |
| PROGB_DDC | J18 | \overline{CF} | D1 | | | | | | |
| PROM_CCK_DDC | J10 | CLKOUT | C2 | | | | | | |
| PROM_D0_DDC | K11 | D0 | H6 | | | | | | |
| TCK_JTAG | U11 | TCK | H3 | | | | | | |
| TDO_XCF16DDC | V11 | TDO | E6 | | | | | | |
| TMS_JTAG | V12 | TMS | E2 | | | | | | |
| DAD_A_ADDR0 | E1 | | | ADDR0 | 19 | | | | |
| DAD_A_ADDR1 | E2 | | | ADDR1 | 18 | | | | |
| DAD_A_ADDR2 | E3 | | | ADDR2 | 17 | | | | |
| DAD_A_ADDR3 | F3 | | | ADDR3 | 16 | | | | |
| DAD_A_MODE0 | C1 | | | MODE0 | 3 | | | | |
| DAD_A_MODE1 | D1 | | | MODE1 | 2 | | | | |
| DAD_A_SEL0 | AB12 | | | SEL0 | 5 | | | | |
| DAD_A_SEL1 | AC12 | | | SEL1 | 4 | | | | |
| DAD_A_STROBE | AF3 | | | STROBE | 15 | | | | |
| DAD_B_ADDR0 | E26 | | | | | ADDR0 | 19 | | |
| DAD_B_ADDR1 | E25 | | | | | ADDR1 | 18 | | |
| DAD_B_ADDR2 | F25 | | | | | ADDR2 | 17 | | |
| DAD_B_ADDR3 | F24 | | | | | ADDR3 | 16 | | |
| DAD_B_MODE0 | D26 | | | | | MODE0 | 3 | | |
| DAD_B_MODE1 | D25 | | | | | MODE1 | 2 | | |
| DAD_B_SEL0 | R22 | | | | | SEL0 | 5 | | |
| DAD_B_SEL1 | R23 | | | | | SEL1 | 4 | | |
| DAD_B_STROBE | AB20 | | | | | STROBE | 15 | | |
| DAD_INIT | AF4 | | | \overline{RESET} | 59 | \overline{RESET} | 59 | | |
| $\overline{DAD_OE}$ | AF5 | | | \overline{OE} | 6 | \overline{OE} | 6 | | |
| $\overline{DAD_A_SCPEN}$ | AE3 | | | \overline{SCPEN} | 58 | | | | |
| $\overline{DAD_B_SCPEN}$ | AB19 | | | | | \overline{SCPEN} | 58 | | |
| SCPCLK | AB15 | | | SCPCLK | 56 | SCPCLK | 56 | SCPCLK | AE1 |
| SCPDI | AA15 | | | SCPDO | 57 | SCPDO | 57 | SCPDO | AC3 |
| SCPDO | AA14 | | | SCPDI | 42 | SCPDI | 42 | SCPDI | AD2 |
| $\overline{DMD_A_SCPEN}$ | AB14 | | | | | | | \overline{SCPEN} | AD4 |
| DMD_A_RESET | AD14 | | | | | | | \overline{PWRDN} | B4 |
| DDC_DCLKOUT_A_DPN | N1 | | | | | | | DCLK_AN | D10 |
| DDC_DCLKOUT_A_DPP | M1 | | | | | | | DCLK_AP | D8 |
| DDC_DCLKOUT_B_DPN | Y5 | | | | | | | DCLK_BN | AJ11 |
| DDC_DCLKOUT_B_DPP | Y6 | | | | | | | DCLK_BP | AJ9 |
| DDC_DCLKOUT_C_DPN | AA22 | | | | | | | DCLK_CN | C23 |
| DDC_DCLKOUT_C_DPP | AB22 | | | | | | | DCLK_CP | C21 |
| DDC_DCLKOUT_D_DPN | M26 | | | | | | | DCLK_DN | AJ23 |
| DDC_DCLKOUT_D_DPP | M25 | | | | | | | DCLK_DP | AJ21 |
| DDC_DOUT_A0_DPN | AE2 | | | | | | | D_AN(0) | F2 |

Table 24. DLPC410 Chipset Connections with the DLP9500 (continued)

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 Number 1 (MICROMIRROR DRIVER) | | DLPA200 Number 2 (MICROMIRROR DRIVER) | | DLP9500 or UV (DMD) | |
|----------------------|-----|----------------|-----|--|-----|--|-----|------------------------|------|
| PIN | | PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DDC_DOUT_A0_DPP | AF2 | | | | | | | D_AP(0) | F4 |
| DDC_DOUT_A1_DPN | AD1 | | | | | | | D_AN(1) | H8 |
| DDC_DOUT_A1_DPP | AE1 | | | | | | | D_AP(1) | H10 |
| DDC_DOUT_A2_DPN | AC1 | | | | | | | D_AN(2) | E5 |
| DDC_DOUT_A2_DPP | AC2 | | | | | | | D_AP(2) | E3 |
| DDC_DOUT_A3_DPN | AB1 | | | | | | | D_AN(3) | G9 |
| DDC_DOUT_A3_DPP | AB2 | | | | | | | D_AP(3) | G11 |
| DDC_DOUT_A4_DPN | Y2 | | | | | | | D_AN(4) | D2 |
| DDC_DOUT_A4_DPP | AA2 | | | | | | | D_AP(4) | D4 |
| DDC_DOUT_A5_DPN | W1 | | | | | | | D_AN(5) | G3 |
| DDC_DOUT_A5_DPP | Y1 | | | | | | | D_AP(5) | G5 |
| DDC_DOUT_A6_DPN | V1 | | | | | | | D_AN(6) | E11 |
| DDC_DOUT_A6_DPP | V2 | | | | | | | D_AP(6) | E9 |
| DDC_DOUT_A7_DPN | U1 | | | | | | | D_AN(7) | F8 |
| DDC_DOUT_A7_DPP | U2 | | | | | | | D_AP(7) | F10 |
| DDC_DOUT_A8_DPN | R2 | | | | | | | D_AN(8) | C9 |
| DDC_DOUT_A8_DPP | T2 | | | | | | | D_AP(8) | C11 |
| DDC_DOUT_A9_DPN | N2 | | | | | | | D_AN(9) | H2 |
| DDC_DOUT_A9_DPP | M2 | | | | | | | D_AP(9) | H4 |
| DDC_DOUT_A10_DPN | K1 | | | | | | | D_AN(10) | B10 |
| DDC_DOUT_A10_DPP | L2 | | | | | | | D_AP(10) | B8 |
| DDC_DOUT_A11_DPN | K2 | | | | | | | D_AN(11) | G15 |
| DDC_DOUT_A11_DPP | K3 | | | | | | | D_AP(11) | H14 |
| DDC_DOUT_A12_DPN | J3 | | | | | | | D_AN(12) | D14 |
| DDC_DOUT_A12_DPP | H3 | | | | | | | D_AP(12) | D16 |
| DDC_DOUT_A13_DPN | H2 | | | | | | | D_AN(13) | F14 |
| DDC_DOUT_A13_DPP | J1 | | | | | | | D_AP(13) | F16 |
| DDC_DOUT_A14_DPN | H1 | | | | | | | D_AN(14) | C17 |
| DDC_DOUT_A14_DPP | G1 | | | | | | | D_AP(14) | C15 |
| DDC_DOUT_A15_DPN | G2 | | | | | | | D_AN(15) | H16 |
| DDC_DOUT_A15_DPP | F2 | | | | | | | D_AP(15) | G17 |
| DDC_DOUT_B0_DPN | AE5 | | | | | | | D_BN(0) | AH2 |
| DDC_DOUT_B0_DPP | AE6 | | | | | | | D_BP(0) | AH4 |
| DDC_DOUT_B1_DPN | AD3 | | | | | | | D_BN(1) | AD8 |
| DDC_DOUT_B1_DPP | AD4 | | | | | | | D_BP(1) | AD10 |
| DDC_DOUT_B2_DPN | AD5 | | | | | | | D_BN(2) | AJ5 |
| DDC_DOUT_B2_DPP | AD6 | | | | | | | D_BP(2) | AJ3 |
| DDC_DOUT_B3_DPN | AC3 | | | | | | | D_BN(3) | AE3 |
| DDC_DOUT_B3_DPP | AC4 | | | | | | | D_BP(3) | AE5 |
| DDC_DOUT_B4_DPN | AB5 | | | | | | | D_BN(4) | AG9 |
| DDC_DOUT_B4_DPP | AB6 | | | | | | | D_BP(4) | AG11 |
| DDC_DOUT_B5_DPN | AB7 | | | | | | | D_BN(5) | AE11 |
| DDC_DOUT_B5_DPP | AC6 | | | | | | | D_BP(5) | AE9 |
| DDC_DOUT_B6_DPN | AA5 | | | | | | | D_BN(6) | AH10 |

Table 24. DLPC410 Chipset Connections with the DLP9500 (continued)

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 Number 1 (MICROMIRROR DRIVER) | | DLPA200 Number 2 (MICROMIRROR DRIVER) | | DLP9500 or UV (DMD) | |
|----------------------|------|----------------|-----|--|-----|--|-----|------------------------|------|
| PIN | | PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DDC_DOUT_B6_DPP | AA4 | | | | | | | D_BP(6) | AH8 |
| DDC_DOUT_B7_DPN | AA7 | | | | | | | D_BN(7) | AF10 |
| DDC_DOUT_B7_DPP | Y7 | | | | | | | D_BP(7) | AF8 |
| DDC_DOUT_B8_DPN | Y3 | | | | | | | D_BN(8) | AK8 |
| DDC_DOUT_B8_DPP | W3 | | | | | | | D_BP(8) | AK10 |
| DDC_DOUT_B9_DPN | W4 | | | | | | | D_BN(9) | AG5 |
| DDC_DOUT_B9_DPP | V4 | | | | | | | D_BP(9) | AG3 |
| DDC_DOUT_B10_DPN | W6 | | | | | | | D_BN(10) | AL11 |
| DDC_DOUT_B10_DPP | W5 | | | | | | | D_BP(10) | AL9 |
| DDC_DOUT_B11_DPN | V7 | | | | | | | D_BN(11) | AE15 |
| DDC_DOUT_B11_DPP | V6 | | | | | | | D_BP(11) | AD14 |
| DDC_DOUT_B12_DPN | U4 | | | | | | | D_BN(12) | AH14 |
| DDC_DOUT_B12_DPP | V3 | | | | | | | D_BP(12) | AH16 |
| DDC_DOUT_B13_DPN | T4 | | | | | | | D_BN(13) | AF14 |
| DDC_DOUT_B13_DPP | T5 | | | | | | | D_BP(13) | AF16 |
| DDC_DOUT_B14_DPN | U6 | | | | | | | D_BN(14) | AJ17 |
| DDC_DOUT_B14_DPP | U5 | | | | | | | D_BP(14) | AJ15 |
| DDC_DOUT_B15_DPN | U7 | | | | | | | D_BN(15) | AD16 |
| DDC_DOUT_B15_DPP | T7 | | | | | | | D_BP(15) | AE17 |
| DDC_DOUT_C0_DPN | T22 | | | | | | | D_CN(0) | B14 |
| DDC_DOUT_C0_DPP | T23 | | | | | | | D_CP(0) | B16 |
| DDC_DOUT_C1_DPN | R20 | | | | | | | D_CN(1) | E15 |
| DDC_DOUT_C1_DPP | R21 | | | | | | | D_CP(1) | E17 |
| DDC_DOUT_C2_DPN | T19 | | | | | | | D_CN(2) | A17 |
| DDC_DOUT_C2_DPP | T20 | | | | | | | D_CP(2) | A15 |
| DDC_DOUT_C3_DPN | U21 | | | | | | | D_CN(3) | G21 |
| DDC_DOUT_C3_DPP | U22 | | | | | | | D_CP(3) | H20 |
| DDC_DOUT_C4_DPN | U20 | | | | | | | D_CN(4) | B20 |
| DDC_DOUT_C4_DPP | U19 | | | | | | | D_CP(4) | B22 |
| DDC_DOUT_C5_DPN | V23 | | | | | | | D_CN(5) | F20 |
| DDC_DOUT_C5_DPP | V24 | | | | | | | D_CP(5) | F22 |
| DDC_DOUT_C6_DPN | V22 | | | | | | | D_CN(6) | D22 |
| DDC_DOUT_C6_DPP | V21 | | | | | | | D_CP(6) | D20 |
| DDC_DOUT_C7_DPN | W19 | | | | | | | D_CN(7) | G23 |
| DDC_DOUT_C7_DPP | V19 | | | | | | | D_CP(7) | H22 |
| DDC_DOUT_C8_DPN | W23 | | | | | | | D_CN(8) | B26 |
| DDC_DOUT_C8_DPP | W24 | | | | | | | D_CP(8) | B28 |
| DDC_DOUT_C9_DPN | Y22 | | | | | | | D_CN(9) | F28 |
| DDC_DOUT_C9_DPP | Y23 | | | | | | | D_CP(9) | F26 |
| DDC_DOUT_C10_DPN | Y20 | | | | | | | D_CN(10) | C29 |
| DDC_DOUT_C10_DPP | Y21 | | | | | | | D_CP(10) | C27 |
| DDC_DOUT_C11_DPN | AA24 | | | | | | | D_CN(11) | G27 |
| DDC_DOUT_C11_DPP | AA23 | | | | | | | D_CP(11) | G29 |
| DDC_DOUT_C12_DPN | AA19 | | | | | | | D_CN(12) | D26 |

Table 24. DLPC410 Chipset Connections with the DLP9500 (continued)

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 Number 1 (MICROMIRROR DRIVER) | | DLPA200 Number 2 (MICROMIRROR DRIVER) | | DLP9500 or UV (DMD) | |
|----------------------|------|----------------|-----|--|-----|--|-----|------------------------|------|
| PIN | | PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DDC_DOUT_C12_DPP | AA20 | | | | | | | D_CP(12) | D28 |
| DDC_DOUT_C13_DPN | AC24 | | | | | | | D_CN(13) | H28 |
| DDC_DOUT_C13_DPP | AB24 | | | | | | | D_CP(13) | H26 |
| DDC_DOUT_C14_DPN | AC19 | | | | | | | D_CN(14) | E29 |
| DDC_DOUT_C14_DPP | AD19 | | | | | | | D_CP(14) | E27 |
| DDC_DOUT_C15_DPN | AC22 | | | | | | | D_CN(15) | J29 |
| DDC_DOUT_C15_DPP | AC23 | | | | | | | D_CP(15) | J27 |
| DDC_DOUT_D0_DPN | AB26 | | | | | | | D_DN(0) | AK14 |
| DDC_DOUT_D0_DPP | AC26 | | | | | | | D_DP(0) | AK16 |
| DDC_DOUT_D1_DPN | AA25 | | | | | | | D_DN(1) | AG15 |
| DDC_DOUT_D1_DPP | AB25 | | | | | | | D_DP(1) | AG17 |
| DDC_DOUT_D2_DPN | Y26 | | | | | | | D_DN(2) | AL17 |
| DDC_DOUT_D2_DPP | Y25 | | | | | | | D_DP(2) | AL15 |
| DDC_DOUT_D3_DPN | W26 | | | | | | | D_DN(3) | AE21 |
| DDC_DOUT_D3_DPP | W25 | | | | | | | D_DP(3) | AD20 |
| DDC_DOUT_D4_DPN | U26 | | | | | | | D_DN(4) | AK20 |
| DDC_DOUT_D4_DPP | V26 | | | | | | | D_DP(4) | AK22 |
| DDC_DOUT_D5_DPN | U25 | | | | | | | D_DN(5) | AF20 |
| DDC_DOUT_D5_DPP | U24 | | | | | | | D_DP(5) | AF22 |
| DDC_DOUT_D6_DPN | T25 | | | | | | | D_DN(6) | AH22 |
| DDC_DOUT_D6_DPP | T24 | | | | | | | D_DP(6) | AH20 |
| DDC_DOUT_D7_DPN | R26 | | | | | | | D_DN(7) | AE23 |
| DDC_DOUT_D7_DPP | R25 | | | | | | | D_DP(7) | AD22 |
| DDC_DOUT_D8_DPN | P24 | | | | | | | D_DN(8) | AK26 |
| DDC_DOUT_D8_DPP | P25 | | | | | | | D_DP(8) | AK28 |
| DDC_DOUT_D9_DPN | N24 | | | | | | | D_DN(9) | AF28 |
| DDC_DOUT_D9_DPP | M24 | | | | | | | D_DP(9) | AF26 |
| DDC_DOUT_D10_DPN | L25 | | | | | | | D_DN(10) | AJ29 |
| DDC_DOUT_D10_DPP | L24 | | | | | | | D_DP(10) | AJ27 |
| DDC_DOUT_D11_DPN | K26 | | | | | | | D_DN(11) | AE27 |
| DDC_DOUT_D11_DPP | K25 | | | | | | | D_DP(11) | AE29 |
| DDC_DOUT_D12_DPN | J26 | | | | | | | D_DN(12) | AH26 |
| DDC_DOUT_D12_DPP | J25 | | | | | | | D_DP(12) | AH28 |
| DDC_DOUT_D13_DPN | J24 | | | | | | | D_DN(13) | AD28 |
| DDC_DOUT_D13_DPP | H24 | | | | | | | D_DP(13) | AD26 |
| DDC_DOUT_D14_DPN | H26 | | | | | | | D_DN(14) | AG29 |
| DDC_DOUT_D14_DPP | G26 | | | | | | | D_DP(14) | AG27 |
| DDC_DOUT_D15_DPN | G25 | | | | | | | D_DN(15) | AC29 |
| DDC_DOUT_D15_DPP | G24 | | | | | | | D_DP(15) | AC27 |
| DDC_SCTRL_AN | R1 | | | | | | | SCTRL_AN | J3 |
| DDC_SCTRL_AP | P1 | | | | | | | SCTRL_AP | J5 |
| DDC_SCTRL_BN | AA3 | | | | | | | SCTRL_BN | AF4 |
| DDC_SCTRL_BP | AB4 | | | | | | | SCTRL_BP | AF2 |
| DDC_SCTRL_CN | W20 | | | | | | | SCTRL_CN | E23 |

Table 24. DLPC410 Chipset Connections with the DLP9500 (continued)

| DLPC410 (CONTROLLER) | | DLPR410 (PROM) | | DLPA200 Number 1 (MICROMIRROR DRIVER) | | DLPA200 Number 2 (MICROMIRROR DRIVER) | | DLP9500 or UV (DMD) | |
|----------------------|-----|----------------|-----|--|-----|--|-----|------------------------|------|
| PIN | | PIN | | PIN | | PIN | | PIN | |
| NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. | NAME | NO. |
| DDC_SCTRL_CP | W21 | | | | | | | SCTRL_CP | E21 |
| DDC_SCTRL_DN | N26 | | | | | | | SCTRL_DN | AG23 |
| DDC_SCTRL_DP | P26 | | | | | | | SCTRL_DP | AG21 |

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Marking

Figure 26 is representative of the Xilinx XC5VLX30 FPGA configured for the DLPC410 device.

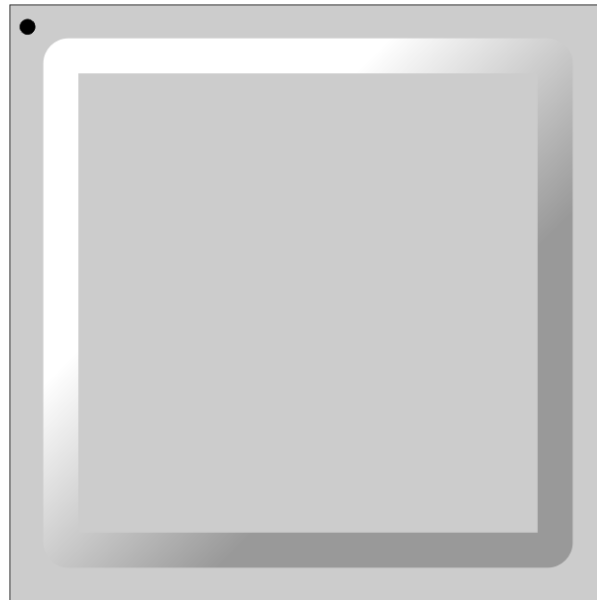


Figure 26. Diagram of the Xilinx XC5VLX30 FPGA

Figure 27 provides a legend for reading the Xilinx device marking for this DLP device.

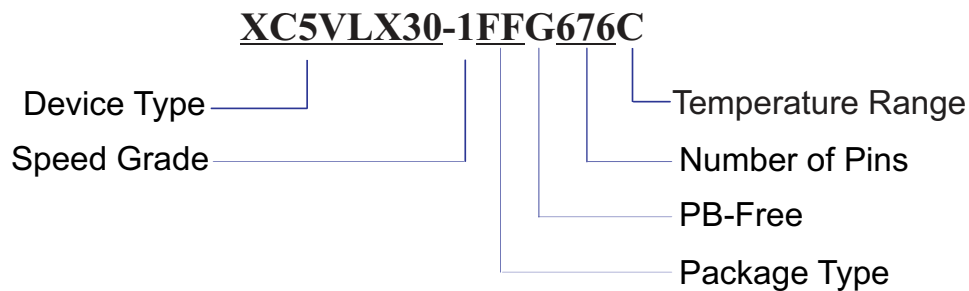


Figure 27. Legend

12.1.2 Device Nomenclature

Figure 28 provides a legend of reading the complete device name for any DLP device.

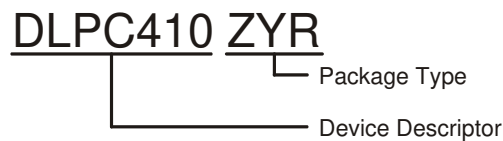


Figure 28. Device Nomenclature

12.2 Documentation Support

12.2.1 Related Documentation

Table 25. Related Documentation

| DOCUMENT | TI LITERATURE NUMBER |
|---|-------------------------|
| DLP650LNIR 0.65 NIR WXGA S450 DMD data sheet | DLPS136 |
| DLP7000 DLP 0.7 XGA 2x LVDS Type A DMD data sheet | DLPS026 |
| DLP7000UV DLP 0.7 UV XGA 2x LVDS Type A DMD data sheet | DLPS061 |
| DLP9500 DLP 0.95 1080p 2x LVDS Type A DMD data sheet | DLPS025 |
| DLP9500UV DLP 0.95 UV 1080p 2x LVDS Type A DMD data sheet | DLPS033 |
| DLPA200 DMD Micromirror Driver data sheet | DLPS015 |
| DLPR410 Configuration PROM data sheet | DLPS027 |

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

E2E is a trademark of Texas Instruments.

DLP is a registered trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| DLPC410ZYR | ACTIVE | | | 676 | 1 | TBD | Call TI | Call TI | 0 to 85 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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