# **Silicon Controlled Rectifiers**Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies.

#### **Features**

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 V
- These are Pb-Free Devices

## **MAXIMUM RATINGS** $^{\dagger}$ (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (T <sub>J</sub> = -40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open) 2N6394 2N6395 2N6397 2N6399	V <sub>DRM</sub> , V <sub>RRM</sub>	50 100 400 800	>
On-State RMS Current (180° Conduction Angles; T <sub>C</sub> = 90°C)	I <sub>T(RMS)</sub>	12	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, T <sub>J</sub> = 90°C)	I <sub>TSM</sub>	100	A
Circuit Fusing (t = 8.3 ms)	I <sup>2</sup> t	40	A <sup>2</sup> s
Forward Peak Gate Power (Pulse Width $\leq$ 1.0 $\mu$ s, T <sub>C</sub> = 90°C)	P <sub>GM</sub>	20	W
Forward Average Gate Power (t = 8.3 ms, T <sub>C</sub> = 90°C)	P <sub>G(AV)</sub>	0.5	W
Forward Peak Gate Current (Pulse Width $\leq$ 1.0 $\mu$ s, T <sub>C</sub> = 90°C)	I <sub>GM</sub>	2.0	Α
Operating Junction Temperature Range	TJ	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to +150	°C

#### **MAXIMUM RATINGS** $\dagger$ (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	2.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	$T_L$	260	°C

†Indicates JEDEC Registered Data

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

1



#### ON Semiconductor®

http://onsemi.com

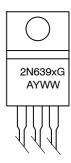
# SCRs 12 AMPERES RMS 50 thru 800 VOLTS



#### MARKING DIAGRAM







2N639x = Device Code x = 4, 5, 7, or 9 G = Pb-Free Package A = Assembly Location

Y = Year WW = Work Week

PIN ASSIGNMENT		
1	Cathode	
2	Anode	
3	Gate	
4	Anode	

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

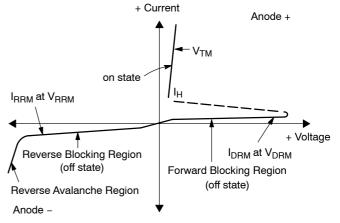
### **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted.)

I <sub>DRM</sub> , I <sub>RRM</sub>				
I <sub>DRM</sub> , I <sub>RRM</sub>				
	_	-	10	μΑ
	-	-	2.0	mA
•			•	
$V_{TM}$	-	1.7	2.2	V
I <sub>GT</sub>	-	5.0	30	mA
V <sub>GT</sub>	-	0.7	1.5	V
$V_{GD}$	0.2	-	-	V
I <sub>H</sub>	-	6.0	50	mA
t <sub>gt</sub>	-	1.0	2.0	μs
tq	_	15	-	μs
	-	35	-	
dv/dt	-	50	-	V/μs
	I <sub>GT</sub> V <sub>GT</sub> V <sub>GD</sub> I <sub>H</sub> t <sub>gt</sub> t <sub>q</sub>	V <sub>TM</sub> -  I <sub>GT</sub> -  V <sub>GD</sub> 0.2  I <sub>H</sub> -  t <sub>q</sub> -  dv/dt -	V <sub>TM</sub> - 1.7  I <sub>GT</sub> - 5.0  V <sub>GT</sub> - 0.7  V <sub>GD</sub> 0.2 -  I <sub>H</sub> - 6.0  t <sub>gt</sub> - 1.0  t <sub>q</sub> - 15  - 35	V <sub>TM</sub> - 1.7 2.2  I <sub>GT</sub> - 5.0 30  V <sub>GT</sub> - 0.7 1.5  V <sub>GD</sub> 0.2  I <sub>H</sub> - 6.0 50  t <sub>gt</sub> - 1.0 2.0  t <sub>q</sub> - 15 - 35 -  dv/dt - 50 -

†Indicates JEDEC Registered Data

#### **Voltage Current Characteristic of SCR**

Symbol	Parameter
V <sub>DRM</sub>	Peak Repetitive Off State Forward Voltage
I <sub>DRM</sub>	Peak Forward Blocking Current
V <sub>RRM</sub>	Peak Repetitive Off State Reverse Voltage
I <sub>RRM</sub>	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
I <sub>H</sub>	Holding Current



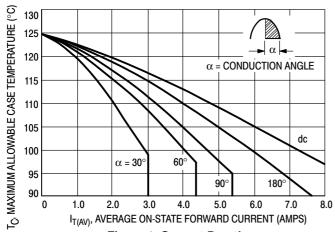


Figure 1. Current Derating

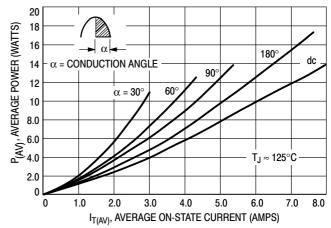


Figure 2. Maximum On-State Power Dissipation

<sup>2.</sup> Pulse Test: Pulse Width  $\leq$  300  $\mu sec,$  Duty Cycle  $\leq$  2%.

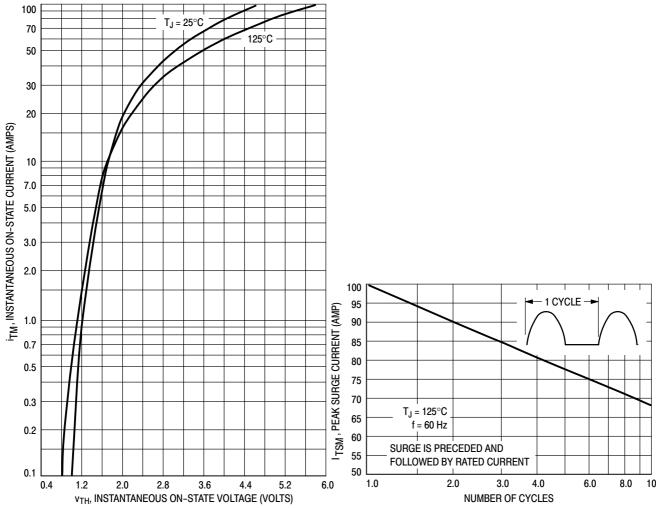


Figure 3. On-State Characteristics

Figure 4. Maximum Non-Repetitive Surge Current

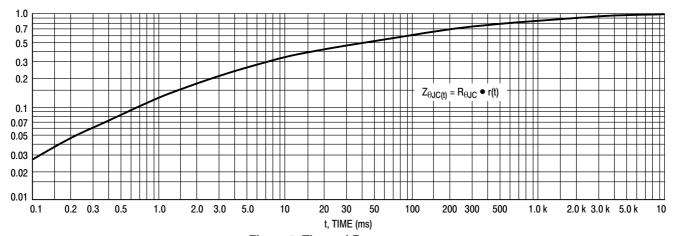
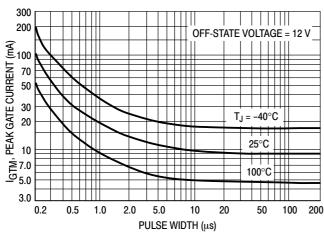


Figure 5. Thermal Response

#### **TYPICAL CHARACTERISTICS**



3.0 OFF-STATE VOLTAGE = 12 V

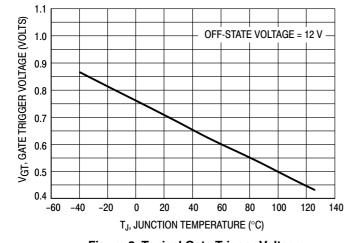
1.0 OFF-STATE VOLTAGE = 12 V

0.5 OFF-STATE VOLTAGE = 12 V

1.0 OF

Figure 6. Typical Gate Trigger Current versus Pulse Width

Figure 7. Typical Gate Trigger Current versus Temperature



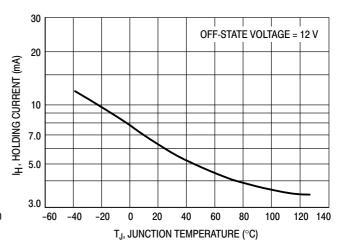


Figure 8. Typical Gate Trigger Voltage versus Temperature

Figure 9. Typical Holding Current versus Temperature

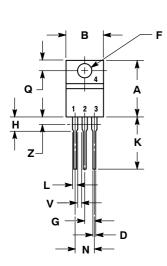
#### **ORDERING INFORMATION**

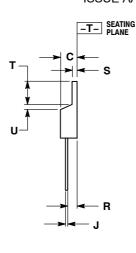
Device	Package	Shipping**
2N6394G		500 Units / Bulk
2N6394TG		50 Units / Rail
2N6395G		500 Units / Bulk
2N6397G	TO-220AB (Pb-Free)	500 Units / Bulk
2N6397TG	, , ,	50 Units / Rail
2N6399G		500 Units / Bulk
2N6399TG	]	50 Units / Rail

<sup>\*\*</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

#### TO-220AB CASE 221A-07 **ISSUE AA**





#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M 1982
- 2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL **BODY AND LEAD IRREGULARITIES ARE** ALLOWED

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

#### STYLE 3:

- PIN 1. CATHODE
  - 2. ANODE 3. GATE
  - ANODE

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