

# TPS563209 Step-Down Converter Evaluation Module User's Guide



## ABSTRACT

This user's guide contains information for the TPS563209 as well as support documentation for the TPS563209EVM-652 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS563209EVM-652.

## Table of Contents

<b>1 Introduction</b> .....	3
<b>2 Performance Specification Summary</b> .....	4
<b>3 Modifications</b> .....	5
3.1 Output Voltage Setpoint.....	5
<b>4 Test Setup and Results</b> .....	6
4.1 Input/Output Connections.....	6
4.2 Start-Up Procedure.....	6
4.3 Efficiency.....	7
4.4 Load Regulation.....	8
4.5 Line Regulation.....	9
4.6 Load Transient Response.....	9
4.7 Output Voltage Ripple.....	10
4.8 Input Voltage Ripple.....	11
4.9 Start-Up.....	12
4.10 Shut-Down.....	13
<b>5 Board Layout</b> .....	14
5.1 Layout.....	14
<b>6 Schematic, Bill of Materials, and Reference</b> .....	16
6.1 Schematic.....	16
6.2 Bill of Materials.....	17
6.3 Reference.....	18
<b>7 Revision History</b> .....	18

## List of Figures

Figure 4-1. TPS563209EVM-652 Efficiency.....	7
Figure 4-2. TPS563209EVM-652 Light Load Efficiency.....	7
Figure 4-3. TPS563209EVM-652 Load Regulation, 5-V Input.....	8
Figure 4-4. TPS563209EVM-652 Load Regulation, 12-V Input.....	8
Figure 4-5. TPS563209EVM-652 Line Regulation.....	9
Figure 4-6. TPS563209EVM-652 Load Transient Response, 25% to 75% Load Step.....	9
Figure 4-7. TPS563209EVM-652 Output Voltage Ripple, $I_{OUT} = 3\text{ A}$ .....	10
Figure 4-8. TPS563209EVM-652 Output Voltage Ripple, $I_{OUT} = 0\text{ mA}$ .....	10
Figure 4-9. TPS563209EVM-652 Input Voltage Ripple, $I_{OUT} = 3\text{ A}$ .....	11
Figure 4-10. TPS563209EVM-652 Start-Up Relative to $V_{IN}$ .....	12
Figure 4-11. TPS563209EVM-652 Start-Up Relative to EN.....	12
Figure 4-12. TPS563209EVM-652 Shut-Down Relative to $V_{IN}$ .....	13
Figure 4-13. TPS563209EVM-652 Shut-Down Relative to EN.....	13
Figure 5-1. Top Assembly.....	14
Figure 5-2. Top Layer.....	14
Figure 5-3. Bottom Layer.....	15
Figure 6-1. TPS563209EVM-652 Schematic Diagram.....	16

## List of Tables

Table 1-1. Input Voltage and Output Current Summary.....	3
Table 2-1. TPS563209EVM-652 Performance Specifications Summary.....	4
Table 3-1. Output Voltages.....	5
Table 4-1. Connection and Test Points.....	6
Table 6-1. Bill of Materials.....	17

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## 1 Introduction

The TPS563209 is a single, adaptive on-time, D-CAP2™ mode, synchronous buck converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 650 kHz. Forced CCM operation maintains constant frequency at light load conditions. The high-side and low-side switching MOSFETs are incorporated inside the TPS563209 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS563209 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS563209 dc/dc synchronous converter is designed to provide up to a 3-A output from an input voltage source of 4.5 V to 17 V. The output voltage range is from 0.8 V to 6.5 V. Rated input voltage and output current ranges for the evaluation module are given in [Table 1-1](#).

The TPS563209EVM-652 evaluation module (EVM) is a single, synchronous buck converter providing 1.05 V at 3 A from 4.5-V to 17-V input. This user's guide describes the TPS563209EVM-652 performance.

**Table 1-1. Input Voltage and Output Current Summary**

EVM	Input Voltage Range	Output Current Range
TPS563209EVM-652	$V_{IN} = 4.5 \text{ V to } 17 \text{ V}$	0 A to 3 A

## 2 Performance Specification Summary

A summary of the TPS563209EVM-652 performance specifications is provided in [Table 2-1](#). Specifications are given for an input voltage of  $V_{IN} = 12\text{ V}$  and an output voltage of  $1.05\text{ V}$ , unless otherwise noted. The ambient temperature is  $25^{\circ}\text{C}$  for all measurement, unless otherwise noted.

**Table 2-1. TPS563209EVM-652 Performance Specifications Summary**

Specifications		Test Conditions	Min	Typ	Max	Unit
Input voltage range ( $V_{IN}$ )			4.5	12	17	V
CH1	Output voltage			1.05		V
	Operating frequency	$V_{IN} = 12\text{ V}, I_O = 3\text{ A}$		650		kHz
	Output current range		0		3	A
	Over current limit	$V_{IN} = 12\text{ V}, L_O = 1.5\text{ }\mu\text{H}$				A
	Output ripple voltage	$V_{IN} = 12\text{ V}, I_O = 3\text{ A}$		20		mV <sub>PP</sub>

### 3 Modifications

These evaluation modules are designed to provide access to the features of the TPS563209. Some modifications can be made to this module.

#### 3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.765 V. The value of R1 for a specific output voltage can be calculated using [Equation 1](#).

$$R1 = \frac{R2 \times (V_{OUT} - 0.765 \text{ V})}{0.765 \text{ V}} \quad (1)$$

[Table 3-1](#) lists the R5 values for some common output voltages. Note that the values given in [Table 3-1](#) are standard values and not the exact value calculated using [Table 3-1](#).

**Table 3-1. Output Voltages**

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C5 + C6 + C7 (μF)
			Min	Typ	Max	
1.0	3.09	10.0	1.5	2.2	4.7	20 - 68
1.05	3.74	10.0	1.5	2.2	4.7	20 - 68
1.2	5.76	10.0	1.5	2.2	4.7	20 - 68
1.5	9.53	10.0	1.5	2.2	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	2.2	3.3	4.7	20 - 68
3.3	33.2	10.0	2.2	3.3	4.7	20 - 68
5.0	54.9	10.0	3.3	4.7	4.7	20 - 68
6.5	75.0	10.0	3.3	4.7	4.7	20 - 68

## 4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS563209EVM-652. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

### 4.1 Input/Output Connections

The TPS563209EVM-652 is provided with input/output connectors and test points as shown in [Table 4-1](#). A power supply capable of supplying 3 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 3 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the  $V_{IN}$  input voltages with TP2 providing a convenient ground reference. TP7 is used to monitor the output voltage with TP8 as the ground reference.

**Table 4-1. Connection and Test Points**

Reference Designator	Function
J1	$V_{IN}$ (see <a href="#">Table 1-1</a> for $V_{IN}$ range)
J2	$V_{OUT}$ , 1.05 V at 3-A maximum
JP1	EN control. Shunt EN to GND to disable, shunt EN to $V_{IN}$ to enable.
TP1	$V_{IN}$ positive monitor point
TP2	GND monitor test point
TP3	EN test point
TP4	Switch node test point
TP5	Test point for loop response measurements
TP6	$V_{OUT}$ positive monitor point
TP7	GND monitor test point

### 4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate  $V_{IN}$  voltage to VI (J1-2) and GND (J1-1).
3. Move the jumper at JP1 (Enable control) from pins 1 and 2 (EN and GND), to pins 2 and 3 (EN and  $V_{IN}$ ) enabling the output.

### 4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS563209EVM-652 at an ambient temperature of 25°C.

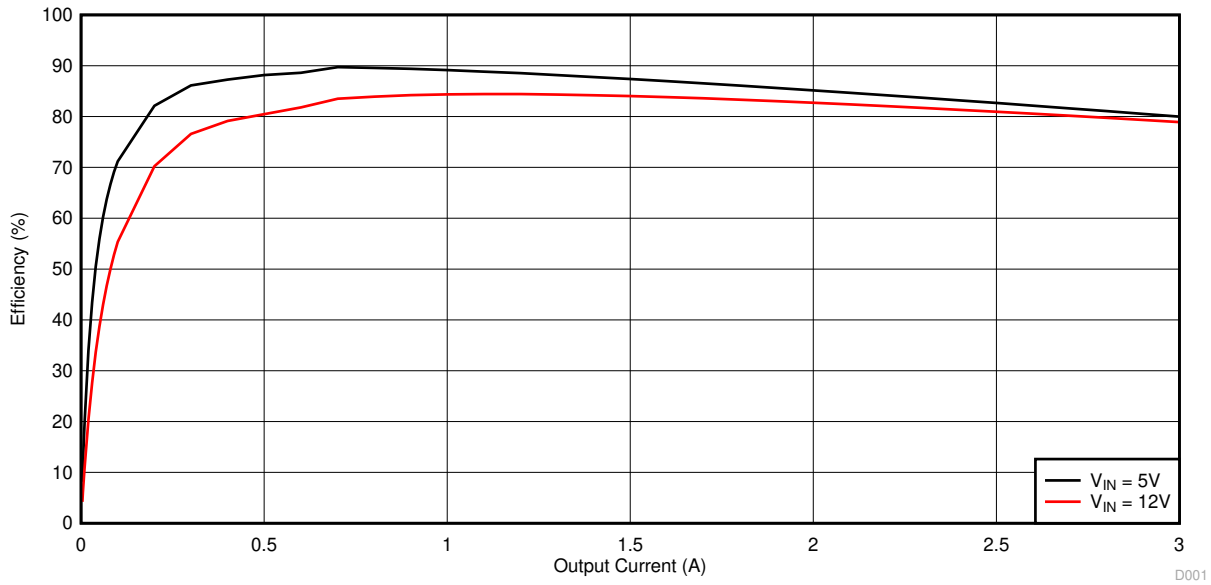


Figure 4-1. TPS563209EVM-652 Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS563209EVM-652 at an ambient temperature of 25°C.

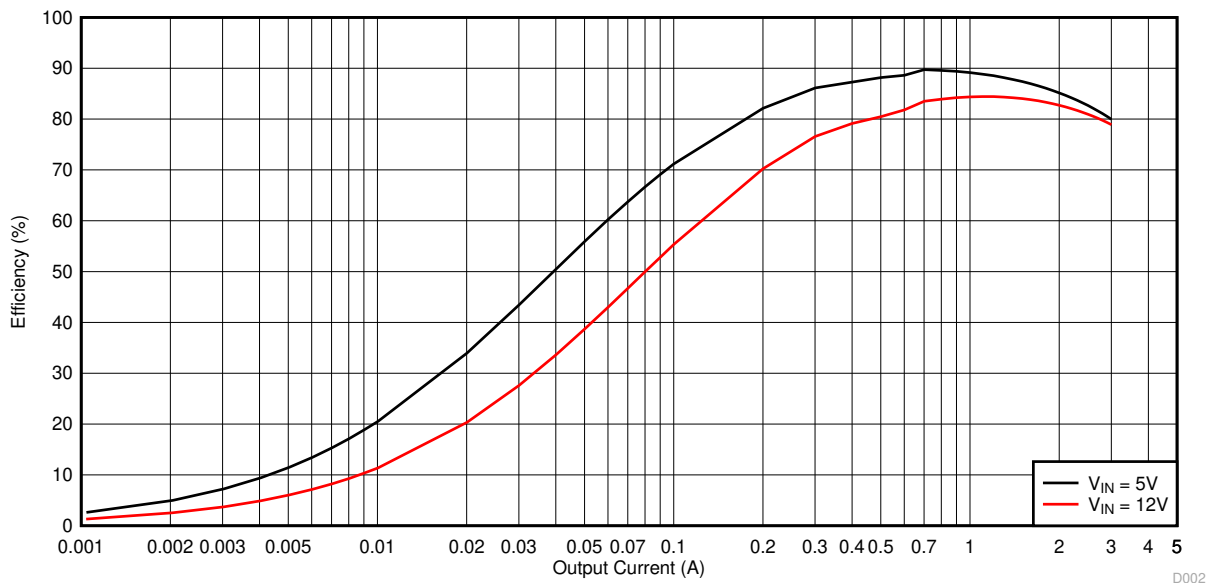
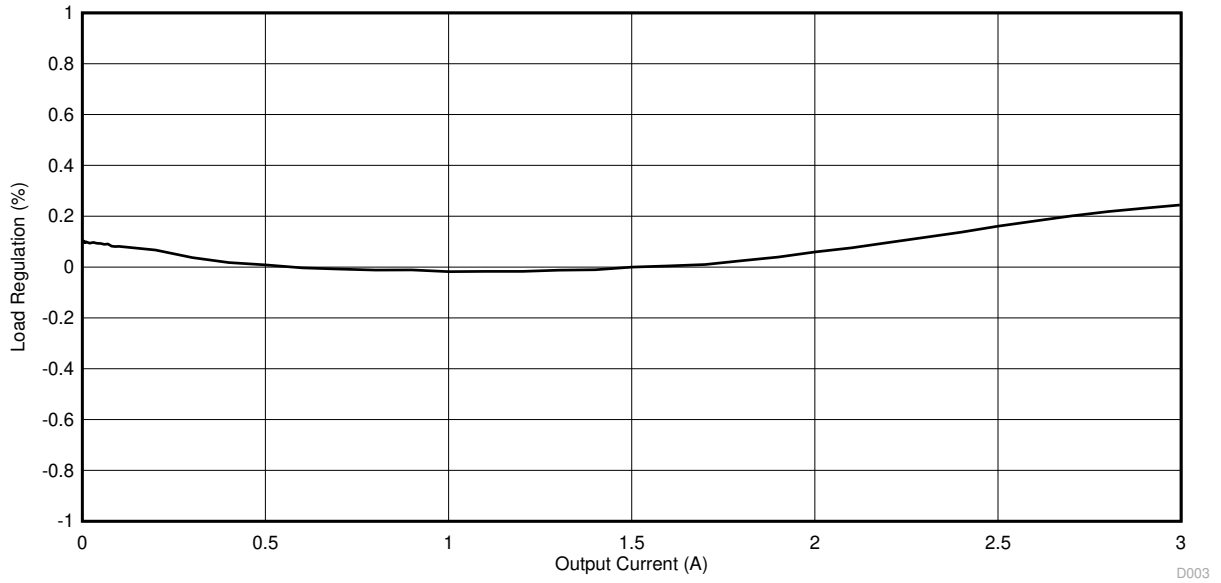


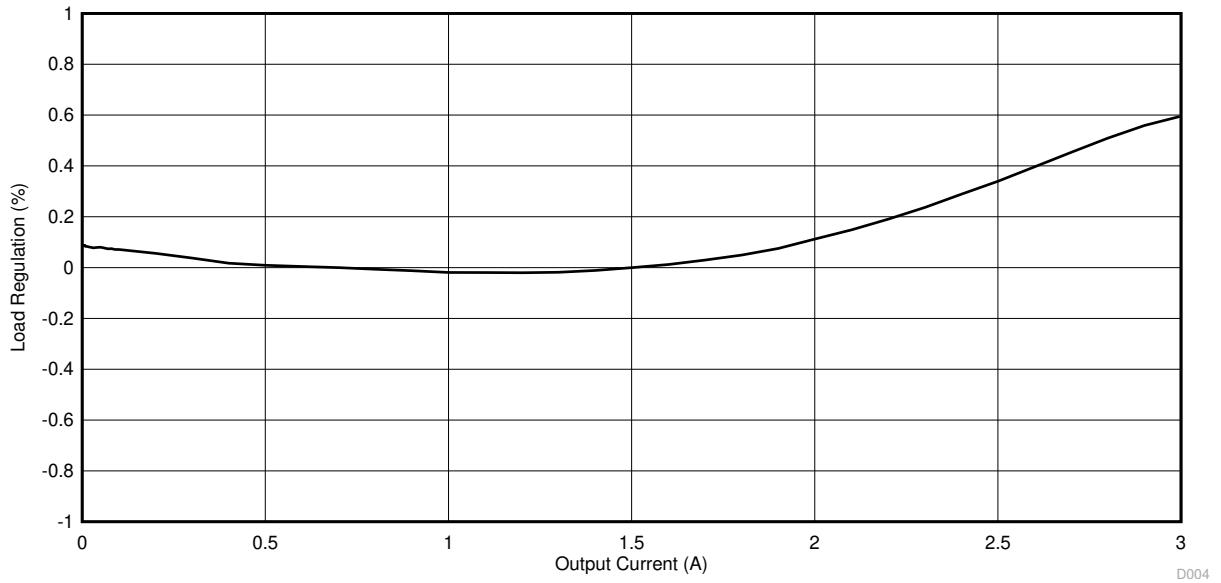
Figure 4-2. TPS563209EVM-652 Light Load Efficiency

## 4.4 Load Regulation

The load regulation for the TPS563209EVM-652 is shown in [Figure 4-3](#) and [Figure 4-4](#).



**Figure 4-3. TPS563209EVM-652 Load Regulation, 5-V Input**



**Figure 4-4. TPS563209EVM-652 Load Regulation, 12-V Input**



### 4.5 Line Regulation

The line regulation for the TPS563209EVM-652 is shown in Figure 4-5.

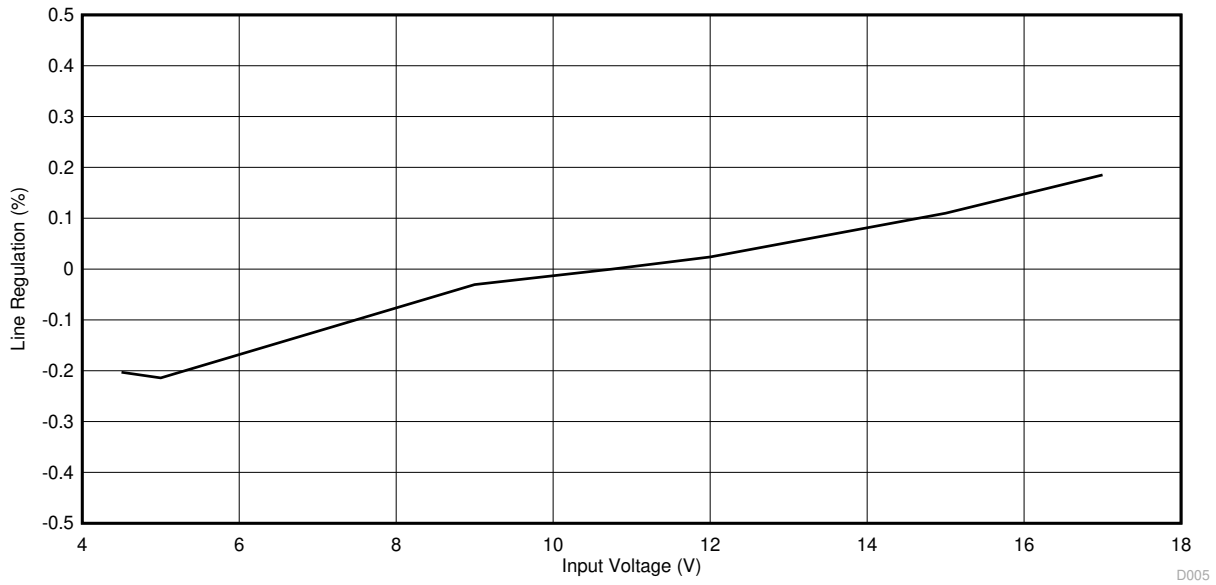


Figure 4-5. TPS563209EVM-652 Line Regulation

### 4.6 Load Transient Response

The TPS563209EVM-652 response to load transient is shown in Figure 4-6. The current steps and slew rates are indicated in the figures. Total peak-to-peak voltage variation is as shown.

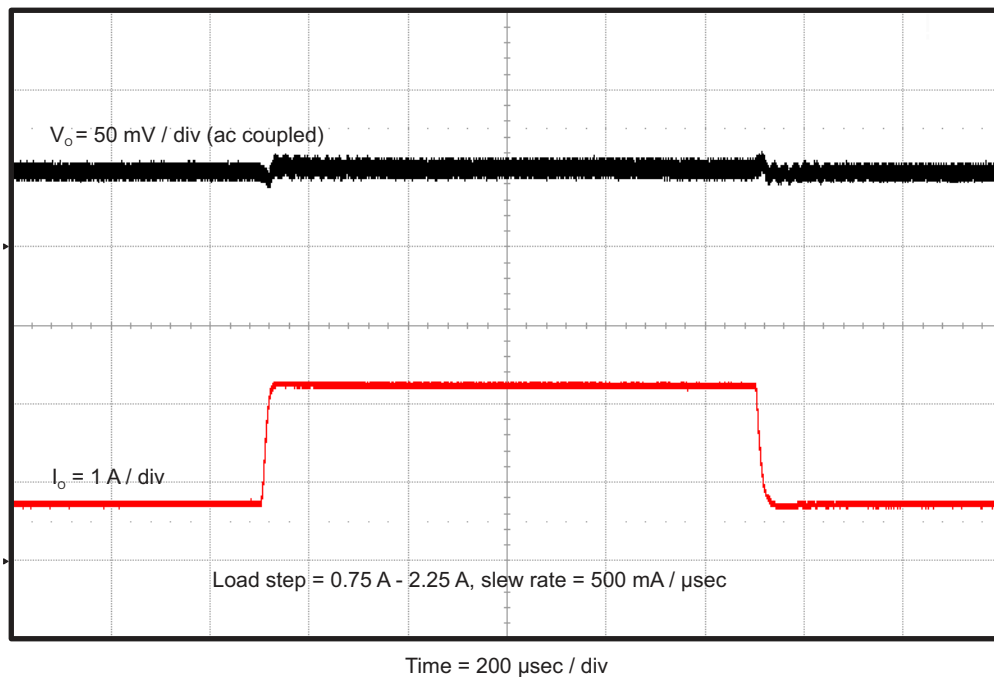
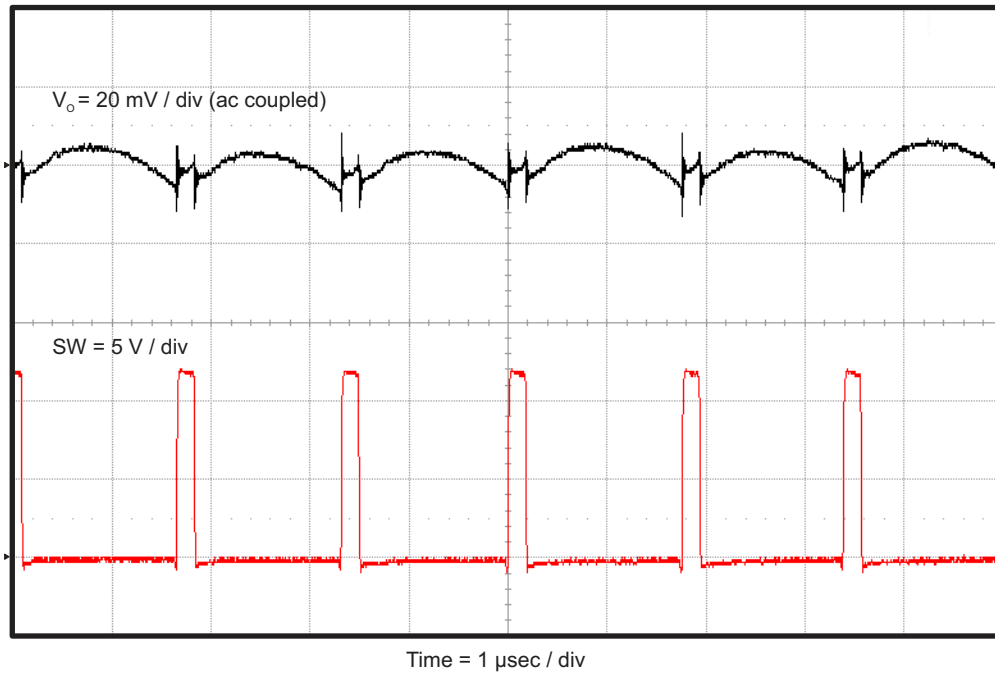


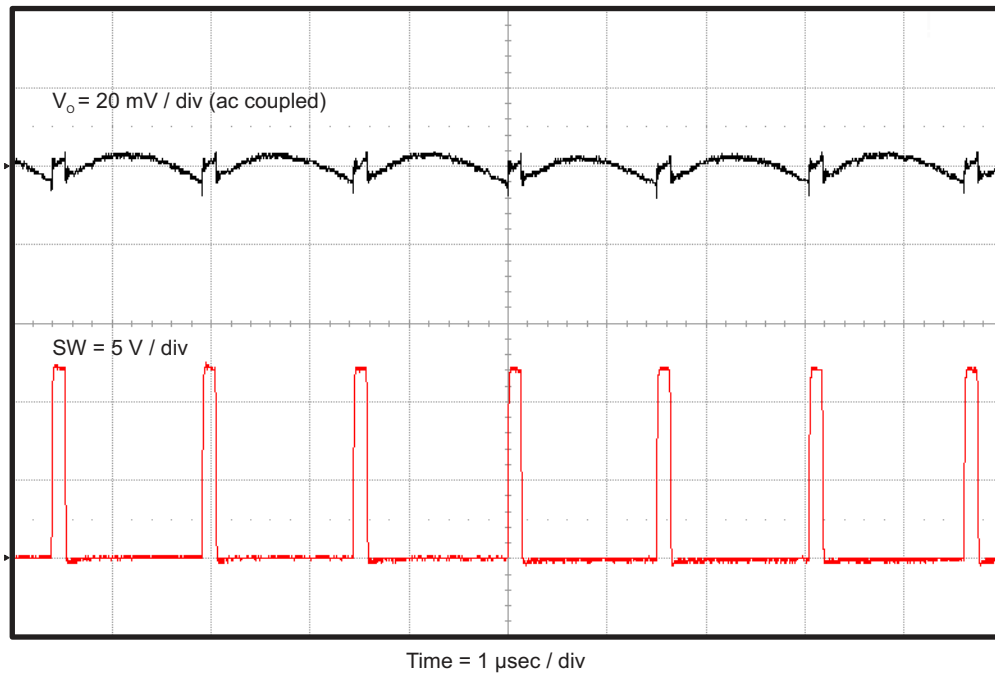
Figure 4-6. TPS563209EVM-652 Load Transient Response, 25% to 75% Load Step

### 4.7 Output Voltage Ripple

The TPS563209EVM-652 output voltage ripple is shown in [Figure 4-7](#), and [Figure 4-8](#). The output currents are as indicated.



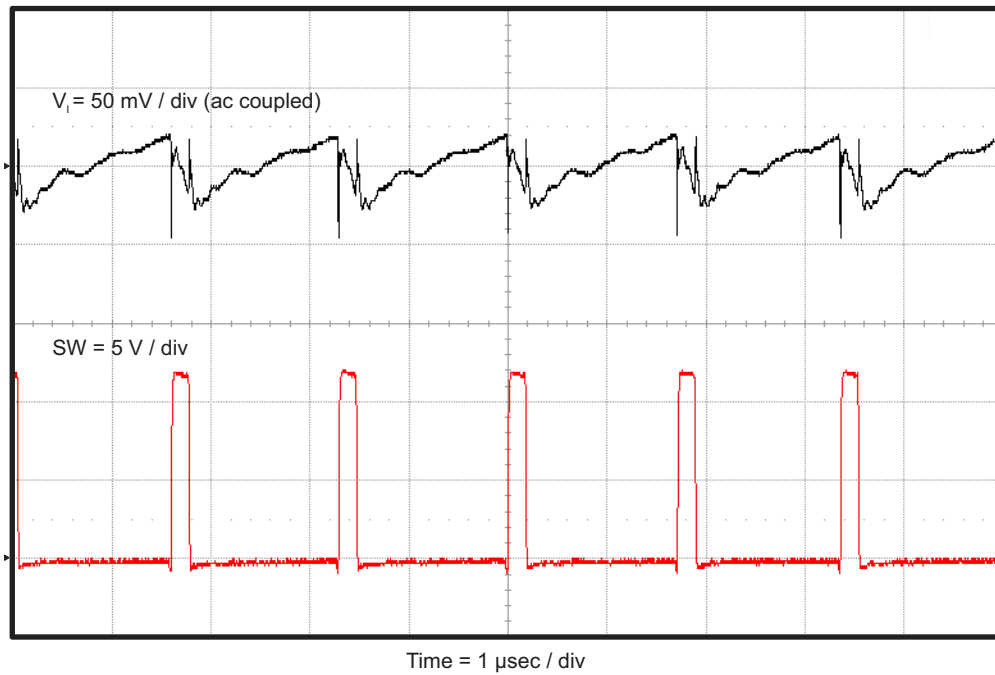
**Figure 4-7. TPS563209EVM-652 Output Voltage Ripple,  $I_{OUT} = 3 \text{ A}$**



**Figure 4-8. TPS563209EVM-652 Output Voltage Ripple,  $I_{OUT} = 0 \text{ mA}$**

## 4.8 Input Voltage Ripple

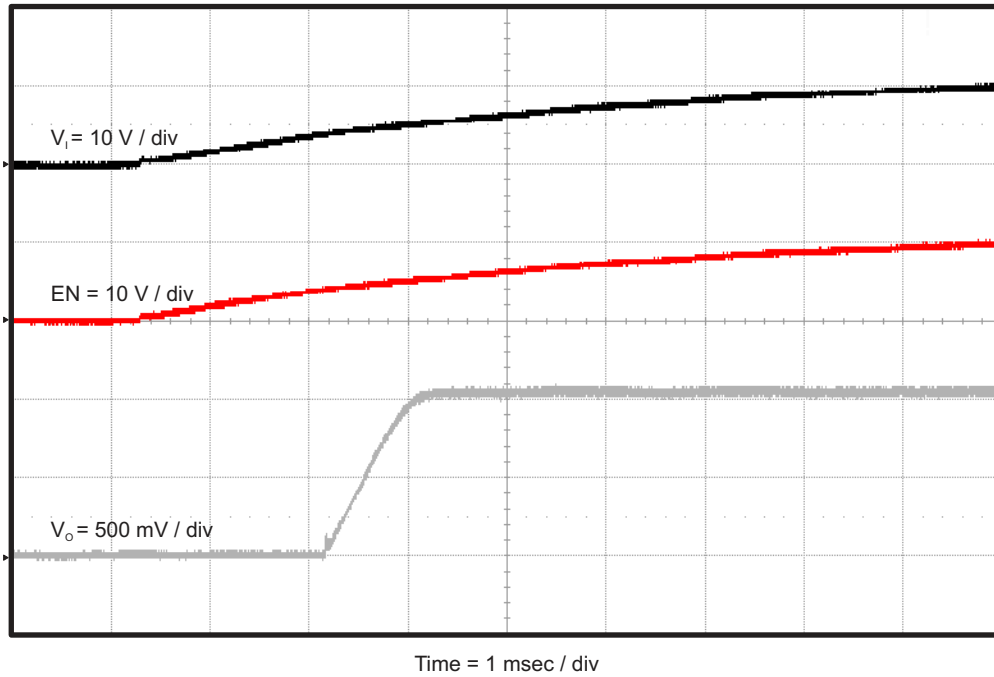
The TPS563209EVM-652 input voltage ripple is shown in [Figure 4-9](#). The output current is as indicated.



**Figure 4-9. TPS563209EVM-652 Input Voltage Ripple,  $I_{OUT} = 3 \text{ A}$**

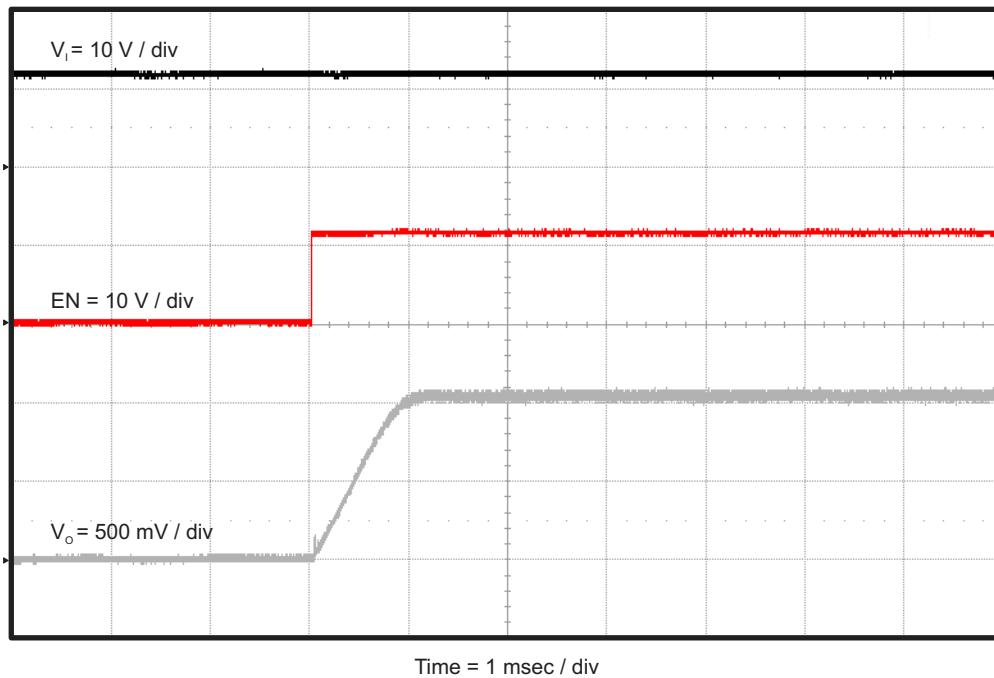
## 4.9 Start-Up

The TPS563209EVM-652 start-up waveform relative to  $V_{IN}$  is shown in [Figure 4-10](#). Load = 1  $\Omega$  resistive.



**Figure 4-10. TPS563209EVM-652 Start-Up Relative to  $V_{IN}$**

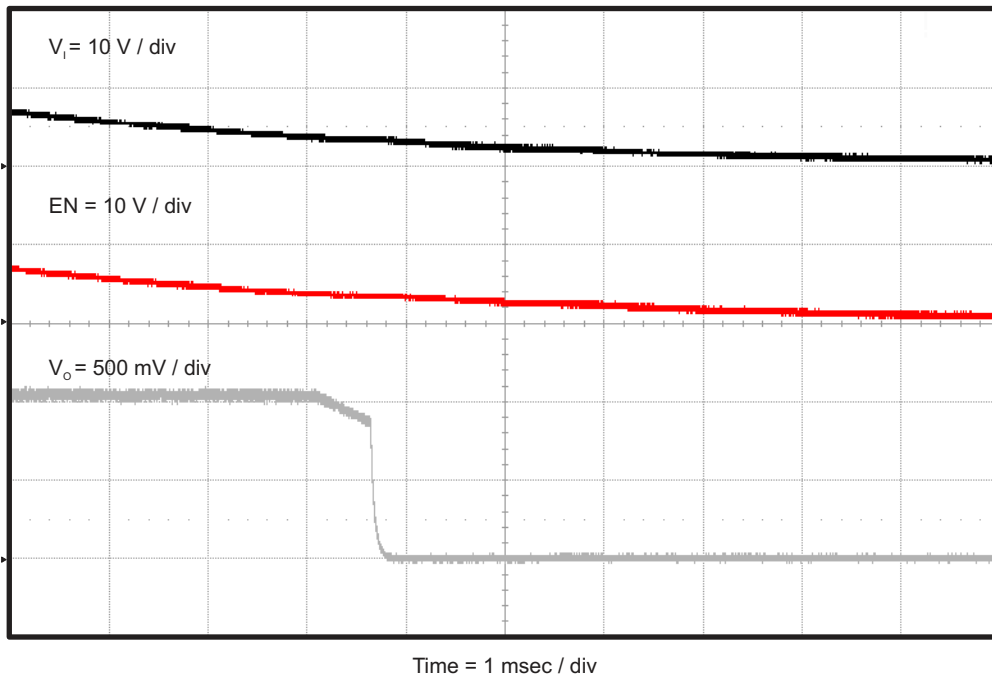
The TPS563209EVM-652 start-up waveform relative to enable (EN) is shown in [Figure 4-11](#). Load = 1  $\Omega$  resistive.



**Figure 4-11. TPS563209EVM-652 Start-Up Relative to EN**

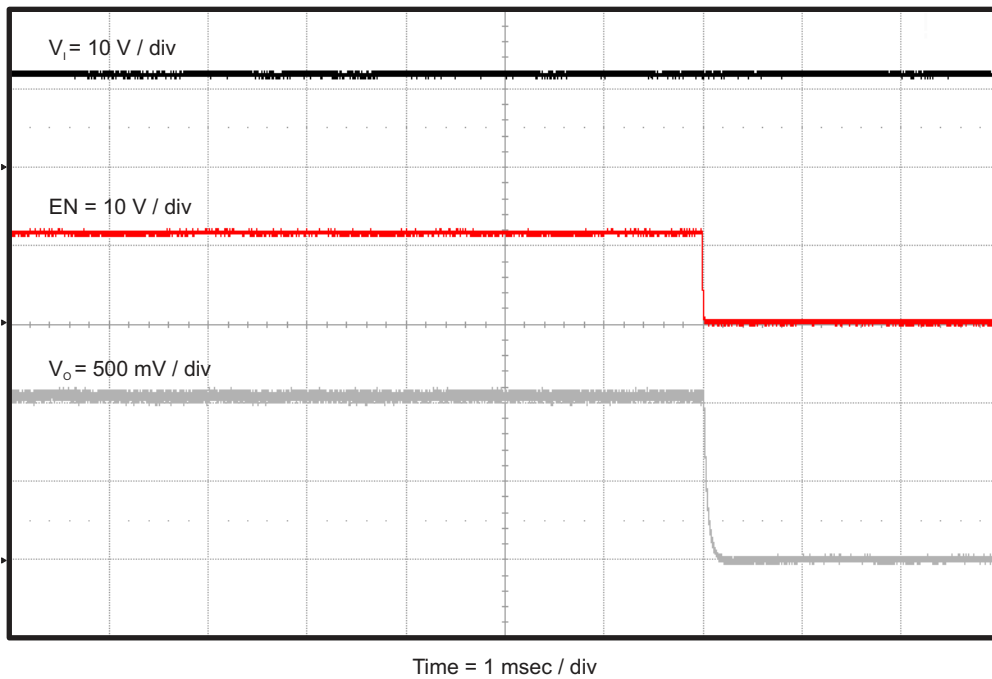
## 4.10 Shut-Down

The TPS563209EVM-652 shut-down waveform relative to  $V_{IN}$  is shown in [Figure 4-12](#). Load = 1  $\Omega$  resistive.



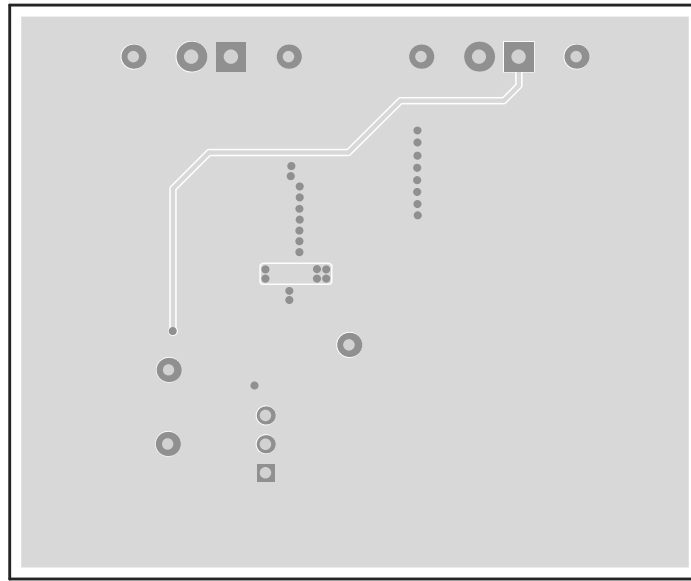
**Figure 4-12. TPS563209EVM-652 Shut-Down Relative to  $V_{IN}$**

The TPS563209EVM-652 shut-down waveform relative to EN is shown in [Figure 4-13](#). Load = 1  $\Omega$  resistive.



**Figure 4-13. TPS563209EVM-652 Shut-Down Relative to EN**





**Figure 5-3. Bottom Layer**

## 6 Schematic, Bill of Materials, and Reference

### 6.1 Schematic

Figure 6-1 is the schematic for the TPS563209EVM-652.

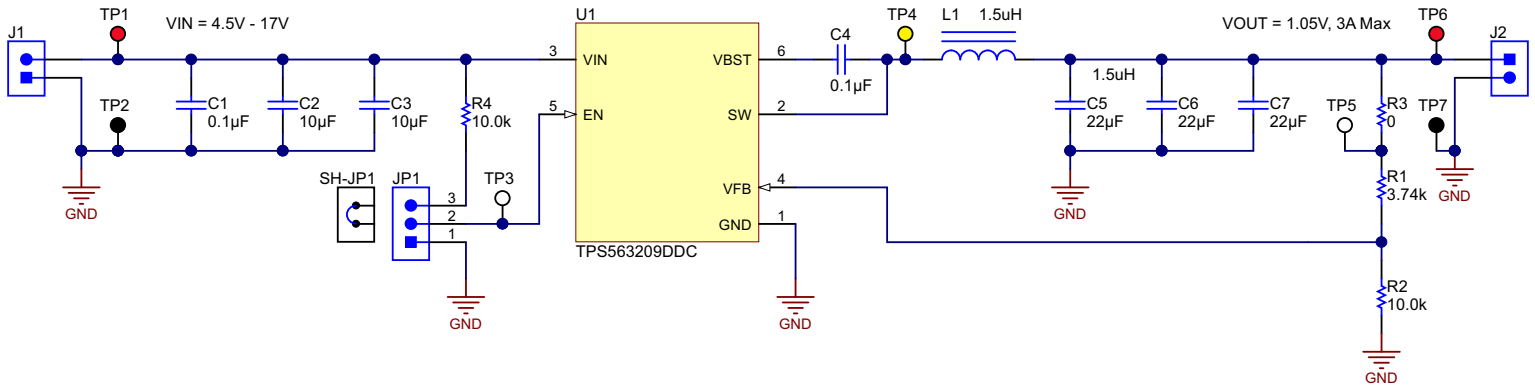


Figure 6-1. TPS563209EVM-652 Schematic Diagram



## 6.2 Bill of Materials

**Table 6-1. Bill of Materials**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		PWR652	Any
C1, C4	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X5R, 0603	0603	GRM188R61E104KA01D	MuRata
C2, C3	2	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1210	1210	GRM32DR61E106KA12L	MuRata
C5, C6, C7	3	22uF	CAP, CERM, 22uF, 10V, +/-10%, X7R, 1206	1206	GRM31CR71A226KE15L	MuRata
J1, J2	2		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
JP1	1		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
L1	1	1.5uH	Inductor, Shielded Drum Core, Superflux, 1.5uH, 11A, 0.0078 ohm, SMD	WE-HC4	744311150	Würth Elektronik eiSos
LBL1	1		Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	PCB Label 1.25"H x 0.250"W	THT-13-457-10	Brady
R1	1	3.74k	RES, 3.74k ohm, 1%, 0.1W, 0603	0603	CRCW06033K74FKEA	Vishay-Dale
R2, R4	2	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R3	1	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	ERJ-3GEY0R00V	Panasonic
SH-JP1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1, TP6	2	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP2, TP7	2	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP3, TP5	2	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP4	1	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
U1	1		TPS563209 4.5V to 17 V Input, 3-A Synchronous Step-Down Voltage Regulator in SOT-23, DDC0006A	DDC0006A	TPS563209DDC	Texas Instruments

### 6.3 Reference

1. *TPS562209 2-A, TPS563209 3-A, 4.5-V to 17-V Input, Synchronous Step-Down Voltage Regulator in 6 pin SOT-23* data sheet ([SLVSCM5](#))

### 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (September 2014) to Revision A (July 2021)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	3
• Updated user's guide title.....	3

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