TEXAS INSTRUMENTS

TPS65120EVM-076/ TPS65124EVM-076

User's Guide

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PMP Portable Power

SLVU112

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the TPS65120EVM−076 and TPS65124EVM−076 evaluation modules (EVM). Included are EVM specifications, test results, schematic diagram, bill of materials (BOM), and recommended test setup.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – EVM Operation
- Chapter 3 – Board Layout
- Chapter 4 – Bill of Materials and Schematic

Related Documentation From Texas Instruments

SLVS531 – TPS6512x data sheet

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Figures

Tables

Chapter 1

Introduction

This chapter contains introductory information about the TPS65120EVM−076 and TPS65124EVM−076 evaluation modules.

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1.1 Background

The TPS65120EVM uses a TPS65120 single inductor, multichannel output IC to provide the three output voltages necessary to power amorphous silicon (a−Si) and low-temperature polysilicon (LTPS) TFT-LCD displays. The TPS65120 has integrated power−up/down sequencing and an auxiliary linear regulator providing an additional 3.3-V rail. The TPS65124EVM uses a TPS65124 IC that provides the same output rails as the TPS65120EVM, except that it has user-programmable power-up/down sequencing and replaces the linear regulator with enable signals for VGH and VGL.

1.2 Performance Specification Summary

Table 1−1. Typical Performance Specification Summary for V_{IN} = 3.6 V and T_A = 25°C

Specification	Output Voltage (V)			Output Current (mA)		
	Min	Typ	Max	Min	Typ	Max
VMAIN	4.95	5.00	5.05			25
VGH	11.64	12.00	12.36			4
VGL	−12.36	−12.00	−11.64			4
LDOOUT (65120)	3.20	3.30	3.40			20

1.3 Modifications

The HPA076 PCB was designed to allow for several user−defined modifications. In addition to being able to accommodate the other members of the TPS6512x family, the board has unpopulated footprints of passive and active elements which provide the following:

- **VLOGIC Rail** – P-channel FET Q1 (e.g., Si1031x) and supporting passives C4, C9, C11, R11, R12, and J6 allow the input voltage to be gated and provide a rail to power peripheral logic circuits . In addition, VLOGIC enables VMAIN, VGH, and VGL after the RC time constant delay formed by R11 and C9 (if R1 is removed).

- **VMAIN Power−Down Sequencing** – The TPS65120/1/2 actively power down VMAIN only after FBL reaches 1.2 V typical. Using N-channel FET Q2 (e.g., Si1032X) and supporting passives R10, R14, and R15 to alter FBL, VMAIN's power-down sequencing trip point can be moved. See the TPS6521x data sheet (SLVS531) for guidance on sizing the passive components.

- **Independent VMAIN Sequencing** – After RUN is pulled high, the TPS6512x devices power up VMAIN. Using dual transistor Q3 (e.g., Si1016X), supporting passives JP4, R16, and R20, and removing R18, a switch can be constructed to switch in VMAIN as the application requires. R18 shorts out Q3.

- **More Current From VMAIN** – An external linear regulator U3 (e.g., TPS79201) powered from BOOT and supporting passives, C14, C15, R17, and R19 can be added to provide more output current for VMAIN. The linear regulator data sheet provides guidance on sizing the supporting passives. Size feedback resistors R17 and R19 so that the regulator output is about 1% below VMAIN. See theTPS6521x data sheet (SLVS531) for guidance on sizing the output capacitor on BOOT relative to C14.

- **A Second Negative Rail, VGL2** – An external linear regulator U2 (e.g., TPS72301) powered from VGL and supporting passives C5, R5, R6, JP3, and J5 can be added to provide a second negative voltage rail. The linear regulator data sheet provides guidance on sizing the supporting passives. The middle pin of JP3 connects to the EN pin on the TPS72301 IC. Tying this pin to VIN enables the IC. Tying this pin to GND disables the IC. J5 is the output terminal for the second negative rail, VGL2. See the TPS6521x data sheet (SLVS531) for guidance on sizing the output capacitor on VGL relative to C5.

- **Lower Output Ripple on VGH and VGL** – C3 and C7 accommodate 10-pF feedforward capacitors that reduce the output ripple on VGH and VGL, respectively.

Chapter 2

EVM Operation

This chapter describes how to properly test the TPS65120 and TPS65124 using the TPS65120EVM and TPS65124EVM.

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2.1 Input/Output Connections

The EVM's input and output connections are described in the following paragraphs.

- **J1-VIN –** This header connects to the positive terminal of the input power supply.
- **J2-GND –** This header connects to the negative terminal of the input power supply.
- **J3-VGH –** This header is the output terminal for the boosted gate voltage, VGH.
- **J4-GND –** This header is a GND terminal.
- **J7-GND –** This header is a GND terminal.
- **J8-VGL –** This header is the output terminal for the inverted gate voltage, VGL.
- **J9-VMAIN –** This header is the output terminal for the main voltage, VMAIN.
- **J10-GND –** This header is a GND terminal.
- **J11-BOOT –** This header is measurement/sense point for the bootstrap voltage, BOOT.
- **JP1-EN –** The middle pin of this jumper connects to the EN pin on the IC. Tying this pin to VIN enables VMAIN on the IC. Tying this pin to GND disables VMAIN on the IC.
- **JP2-RUN –** The middle pin of this jumper connects to the RUN pin on the IC. Tying this pin to VIN begins the power−up procedure of the IC. Tying this pin to GND disables the IC.
- **JP5-LDOIN on TPS65120EVM or VGL on TPS65123EVM** For the TPS65120EVM, the middle pin of this jumper is a measurement/sense point for the input to the auxiliary LDO and pin 3 is GND. LDOIN is connected to BOOT through 0−Ω resistor R7. Pin 1 is floating.

  For the TPS65124EVM, the middle pin of this jumper connects to VGL pin on the IC. Tying this pin to ON enables VGL; tying it to OFF disables VGL.
- **JP6−LDOOUT on TPS65120EVM or VGH on TPS65124EVM** For the TPS65120EVM, the middle pin of this jumper is the output for the auxiliary linear regulator, and pin 3 is GND. Pin 1 is floating.

  For the TPS65124EVM, the middle pin of this jumper connects to VGH pin on the IC. Tying this pin to ON enables VGH. Tying this pin to OFF disables VGH.

  The headers and jumpers that were omitted in the previous discussion are not populated on the EVM and are discussed in section 1.3.

2.2 Test Setup

Although the absolute maximum voltage for V_{IN} is 6 V, the TPS6512x family is designed to operate with input voltages of 5.5 V or less. For best results with the EVM as packaged, connect a power supply with a 3.3-V output voltage and current limit set to at least 500 mA.

To enable the TPS65120EVM, first short pins 1−2 of jumper JP2 (tie RUN to ON); then short pins 1−2 of jumper JP1 (tie EN to ON).

To enable the TPS65124EVM, first short pins 1−2 of jumper JP2 (tie RUN to ON); then short pins 1−2 of jumper JP1 (tie EN to ON) then short pins 1−2 of jumper JP5 and JP6 in any order to enable VGL and VGH, respectively. Connect output loads on each rail not to exceed the maximum current ratings in Table 1−1.

2.3 Test Results

Figure 2−1. Main Output Efficiency vs Load Current

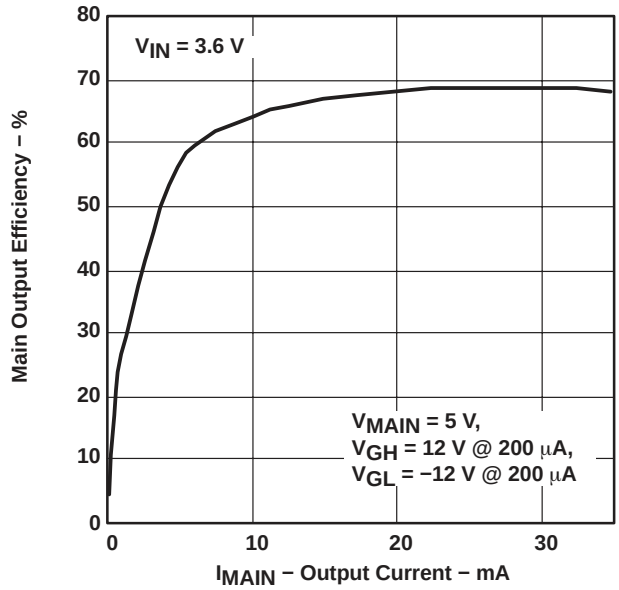


Figure 2−2. Main Output Ripple Voltage

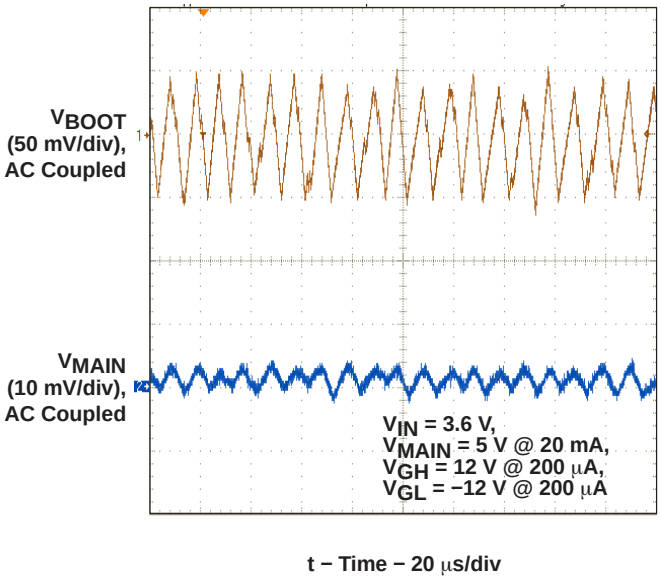
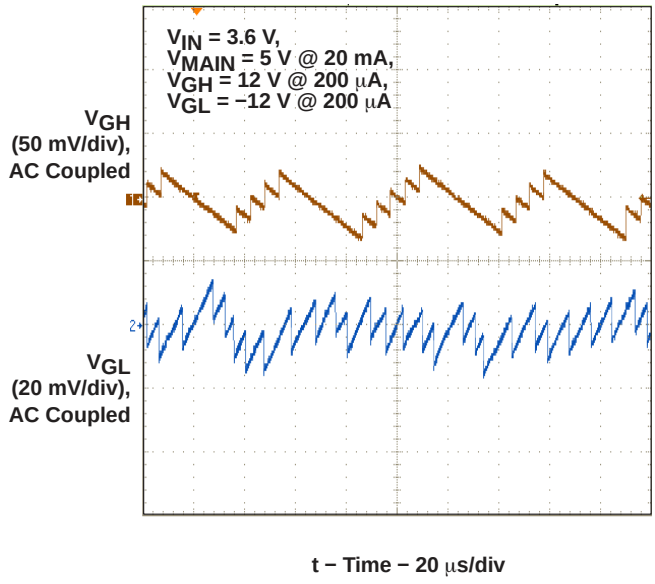


Figure 2−3. VGH and VGL Output Ripple



Chapter 3

Board Layout

The chapter describes the HPA076 PCB board layout and illustrations.

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3.1 Board Layout

Board layout is critical for all switch mode power supplies. Figure 3−1, Figure 3−2, and Figure 3−3 show the board layout for the HPA076 PCB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry and special attention has been given to the routing of high-frequency current loops as well as ground.

Figure 3−1. Top Assembly Layer

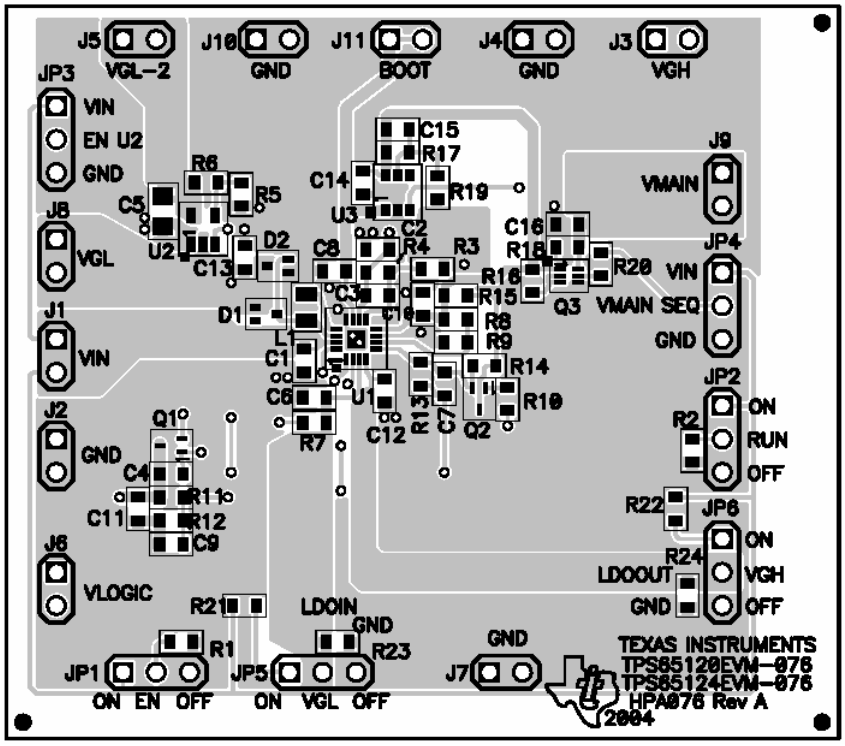


Figure 3−2. Top Layer Routing

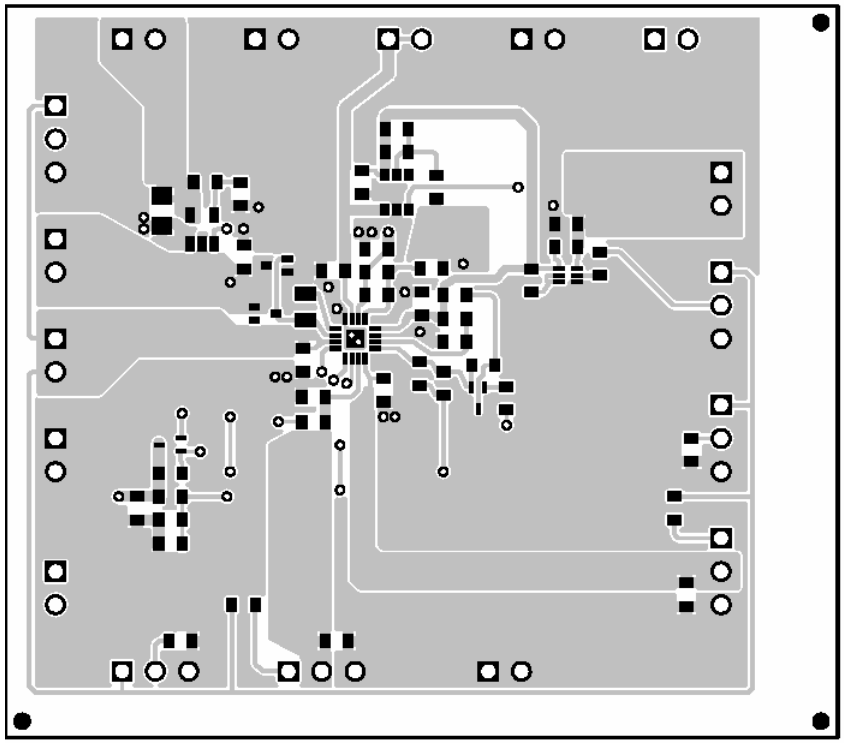
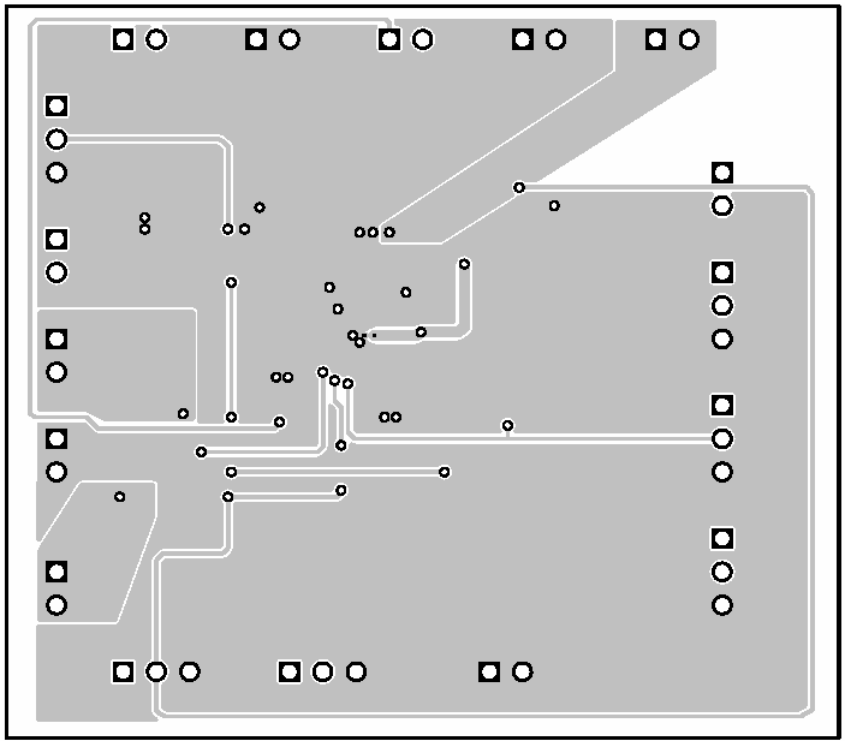


Figure 3−3. Bottom Layer Routing



Chapter 4

Bill of Materials and Schematic

This chapter provides the TPS65120EVM and TPS65124EVM bill of materials and schematic.

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4.1 Bill of Materials

Table 4−1. HPA076 Bill of Materials

Count		RefDes	Description	Size	MFR	Part Number
−001	−002					
1	1	C1	Capacitor, ceramic, 2.2−µF, 6.3−V, X5R, 10%	603	TDK	C1608X5R0J225KT
1	1	C10	Capacitor, ceramic, 0.47−µF, 16−V, X5R, 10%	603	TDK	C1608X5R1C474KT
1	1	C16	Capacitor, ceramic, 0.1−µF, 25−V, X7R, 10%	603	TDK	C1608X7R1E104KT
1	0	C12	Capacitor, ceramic, 0.22−µF, 16−V, X5R, 10%	603	AVX	0603YD224KAT2A
2	2	C2, C13	Capacitor, ceramic, 0.22−µF, 16−V, X5R, 10%	603	AVX	0603YD224KAT2A
1	0	C6	Capacitor, ceramic, 0.1−µF, 25−V, X7R, 10%	603	TDK	C1608X7R1E104KT
0	0	C3, C4, C7, C9, C11, C14, C15	Capacitor, ceramic, xxx−µF, vv−V	603		
0	0	C5	Capacitor, ceramic, xxx−µF, vv−V	805		
1	1	C8	Capacitor, ceramic, 1.0−µF, 16−V, X5R, 10%	603	TDK	C1608X5R1C105KT
1	0	D1	Diode, Schottky, 200−mA, 30−V	LLP75−3B	Vishay	BAT54−HT3−GS08
0	1	D2	Diode, Dual Schottky, 200−mA, 30−V	LLP75−3B	Vishay	BAT54A−HT3−GS08
0	0	J5, J6	Header, 2−pin, 100 mil spacing, (36−pin strip)	0.100 x 2		
9	9	J1−J4, J7−J11	Header, 2−pin, 100 mil spacing, (36−pin strip)	0.100 x 2	Sullins	PTC36SAAN
0	0	JP3, JP4	Header, 3−pin, 100 mil spacing, (36−pin strip)	0.100 x 3		
4	4	JP1, JP2, JP5, JP6	Header, 3−pin, 100 mil spacing, (36−pin strip)	0.100 x 3	Sullins	PTC36SAAN
1	1	L1	Inductor, 10−µH, 500−mΩ, 200−mA	805	Taiyo Yuden	CB2012T100M
0	0	Q1	MOSFET, P−ch, −20V, −150 mA, 8 Ω	SC89−3	Siliconix	Si1031X
0	0	Q2	MOSFET, N−ch, 20V, 200 mA, 5 Ω	SC89−3	Siliconix	Si1032X
0	0	Q3	MOSFET, Dual Nch, 20V, 0.6A, 0.7 Ω, Pch, −20V, −0.4 A, 1.2 Ω	SOT−563	Siliconix	Si1016X
3	3	R1, R2, R3	Resistor, chip, 100 kΩ, 1/16−W, 1%	603	Std	Std
0	2	R23, R24	Resistor, chip, 100 kΩ 1/16−W, 1%	603	Std	Std
1	1	R14	Resistor, chip, 365 kΩ, 1/16−W, 1%	603	Std	Std
3	3	R4, R8, R13	Resistor, chip, 887 kΩ, 1/16−W, 1%	603	Std	Std
0	0	R5, R6, R10, R11, R12, R16, R17, R19, R20	Resistor, Chip, xx−Ω, 1/16−W	603		
1	0	R7	Resistor, Chip, 0−Ω, 1/16−W, 1%	603	Std	Std
0	2	R21, R22	Resistor, Chip, 0−Ω, 1/16−W, 1%	603	Std	Std
2	2	R15, R18	Resistor, Chip, 0−Ω, 1/16−W, 1%	603	Std	Std
1	1	R9	Resistor, Chip, 287 kΩ, 1/16−W, 1%	603	Std	Std

Count		RefDes	Description	Size	MFR	Part Number
−001	−002					
1		U1	IC, Single Inductor Quadruple−Output TFT LCD Power Supply	QFN16	TI	TPS65120QFN
	1		IC, Single Inductor Quadruple−Output TFT LCD Power Supply	QFN16	TI	TPS65124QFN
0	0	U2	IC, 100 mA Negative Output LDO Linear Regulators	SOT23−5	TI	TPS72301DBV
0	0	U3	IC, High PSRR, Low Noise LDO, Adj Output, 100−mA	SOT23−6	TI	TPS79201DBV
1	1	−−	PCB, 2.5 In x 2.2 In x .062 In		Any	HPA076
2	4	−−	Shunt, 100−mil, Black	0.100	3M	929950−00

4.2 Schematic

The HPA076 schematic (Figure 4−1) appears on the following page.

Figure 4−1. HPA076 Schematic