INTEGER-N PLL WITH INTEGRATED VCO

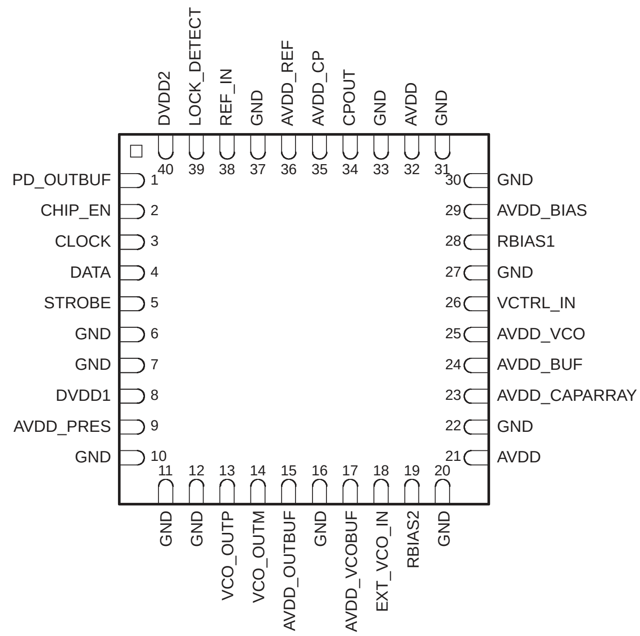
FEATURES

- Fully Integrated VCO
- Low Phase Noise: –138dBc/Hz (at 600kHz, f_{VCO} of 1.9GHz)
- Low Noise Floor: –160dBc/Hz at 10MHz Offset
- Integer-N PLL
- Input Reference Frequency range: 10MHz to 104MHz
- VCO Frequency Divided by 2-4 Output
- Output Buffer Enable Pin
- Programmable Charge Pump Current
- Hardware and Software Power Down
- 3-Wire Serial Interface
- Single Supply: 4.5V to 5.25V Operation
- Silicon Germanium Technology

APPLICATIONS

- Wireless Infrastructure
  - – WCDMA
  - – CDMA
  - – GSM

RHA PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

AVAILABLE DEVICE OPTIONS

PART NUMBER	DIV1 MODE		DIV2 MODE		DIV4 MODE	
	Fstart	Fstop	Fstart	Fstop	Fstart	Fstop
TRF3761-1579	1500	1658	750.0	829.0	375.00	414.50
TRF3761-1700	1600	1700	800	850	400	425
TRF3761-1817	1726	1908	863.0	954.0	431.50	477.00
TRF3761-1947	1850	2045	925.0	1022.5	462.50	511.25
TRF3761-2116	2080	2180	1040	1090	520	545
TRF3761-2289	2175	2404	1087.5	1202.0	543.75	601.00

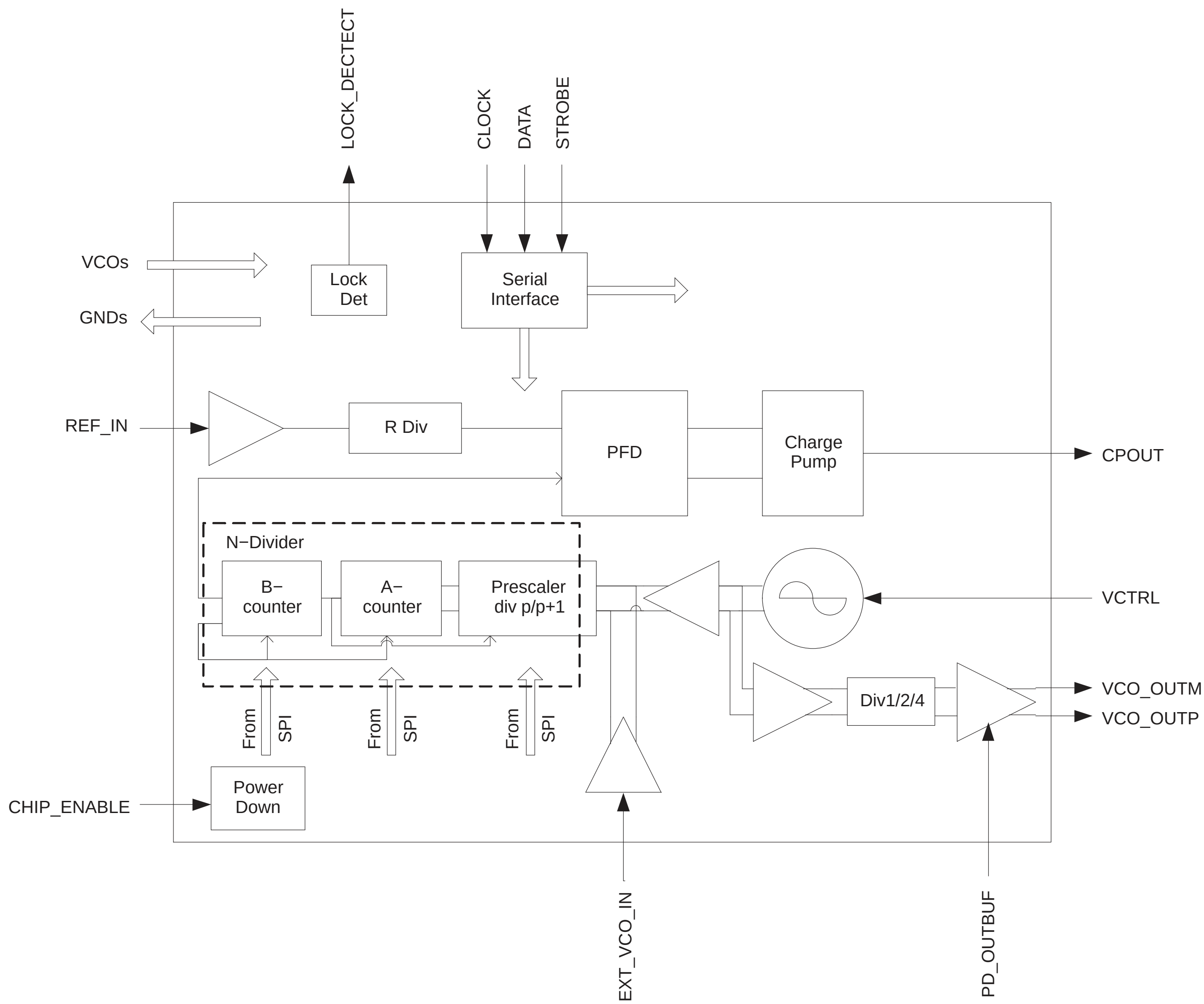
DESCRIPTION

TRF3761 is a family of high performance, highly integrated frequency synthesizers, optimized for wireless infrastructure applications. The TRF3761 includes a low-noise, voltage-controlled oscillator (VCO) and an integer-N PLL.

TRF3761 integrates divide-by 1, 2, or 4 options for a more flexible output frequency range. It is controlled through a 3-wire serial-interface-programming (SPI) interface. It can be powered down when not used by the SPI or external pin.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PD_OUTBUF	1	I	Output buffer power down
CHIP_EN	2	I	Chip enable
CLOCK	3	I	Serial interface clock
DATA	4	I/O	Serial interface data
STROBE	5	I	Serial interface strobe
GND	6, 7		Digital ground
DVDD1	8		Power supply for DIG regulator
AVDD_PRES	9		Power supply for prescaler
VCO_OUTP	13	O	VCO output
VCO_OUTM	14	O	VCO output
AVDD_OUTBUF	15		Power supply for output buffers
AVDD_VCOBUF	17		Power supply for VCO buffers
EXT_VCO_IN	18	I	External VCO input to prescaler
RBIAS2	19	I/O	External bias resistor
AVDD	21		Analog power supply
AVDD_CAPARRAY	23		Power supply for VCO core and buffer
AVDD_BUF	24		Power supply for VCO core and buffer
AVDD_VCO	25		Power supply for VCO core and buffer
VCTRL_IN	26	I	VCO control voltage
RBIAS1	28	I/O	External bias resistor
AVDD_BIAS	29		Power supply for BG current bias
GND	10, 11, 12, 16, 20, 22, 27, 30, 31, 33, 37		Analog ground
AVDD	32		Power supply for FUSE cell
CPOUT	34	O	Charge pump output
AVDD_CP	35		Analog power supply for charge pump
AVDD_REF	36		Power supply for REF FREQ block
REF_IN	38	I	Reference signal input
LOCK_DETECT	39	O	Lock detect output
DVDD2	40		Power supply for DIG regulator

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
	Supply voltage range(2)	–0.3 to 5.5	V
	Digital I/O voltage range	–0.3 to V_I +0.3	V
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_A	Operating free-air temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	4.5	5	5.25	V

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR(2)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKINGS	ORDERING NUMBER	TRANPORT MEDIA, QUANITY
TRF3761-1579	QFN-40	RHA	–40°C to 85°C	TRF3761-1579	TRF376115IRHAR	Tape and Reel, 2500
					TRF376115IRHAT	Tape and Reel, 250
TRF3761-1700	QFN-40	RHA	–40°C to 85°C	TRF3761-1700	TRF376117IRHAR	Tape and Reel, 2500
					TRF376117IRHAT	Tape and Reel, 250
TRF3761-1817	QFN-40	RHA	–40°C to 85°C	TRF3761-1817	TRF376118IRHAR	Tape and Reel, 2500
					TRF376118IRHAT	Tape and Reel, 250
TRF3761-1947	QFN-40	RHA	-40°C to 85°C	TRF3761-1947	TRF376119IRHAR	Tape and Reel, 2500
					TRF376119IRHAT	Tape and Reel, 250
TRF3761-2116	QFN-40	RHA	–40°C to 85°C	TRF3761-2116	TRF376121IRHAR	Tape and Reel, 2500
					TRF376121IRHAT	Tape and Reel, 250
TRF3761-2289	QFN-40	RHA	–40°C to 85°C	TRF3761-2289	TRF376122IRHAR	Tape and Reel, 2500
					TRF376122IRHAT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Thermal pad size: 177 × 177 mils.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Thermal derating, junction-to-ambient	Soldered slug, no airflow		26		°C/W
		Soldered slug, 200-LFM airflow		20.1		°C/W
		Soldered slug, 400-LFM airflow		17.4		°C/W

(1) Determined using JEDEC standard JESD-51 with High K board

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

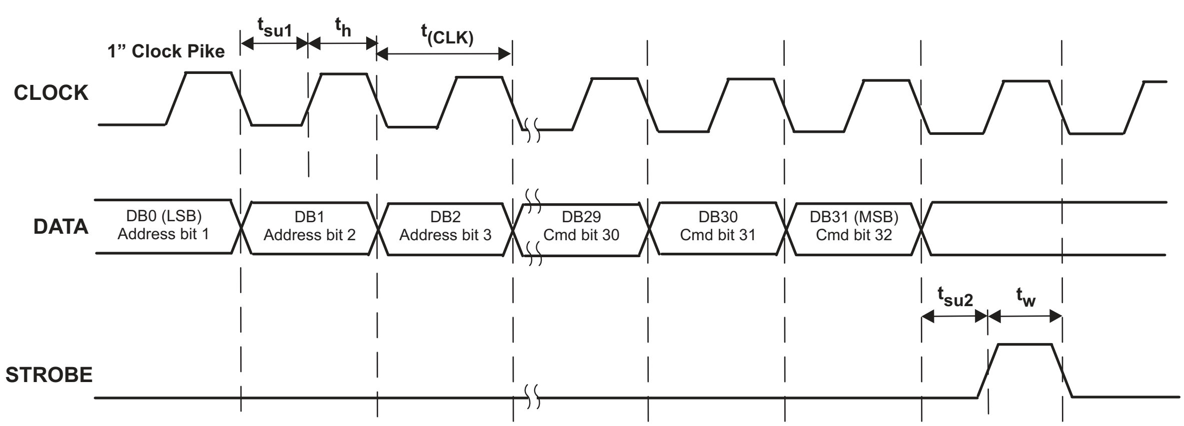
Supply voltage = 4.5V to 5.25V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC Parameters							
I_{CC}	Total supply current	T_A = 25°C	Divide by 1 output		130		mA
			Divide by 2 output		140		mA
			Divide by 4 output		150		mA
Reference Oscillator Parameters							
f_{ref}	Reference frequency			10		104	MHz
	Reference input sensitivity			0.2		2.5	Vpp
	Reference input impedance	Parallel capacitance			5	6.52	pF
		Parallel resistance		3913			Ω
PFD Charge Pump							
	PFD frequency					30	MHz
	Charge pump current	SPI programmable			5.6		mA
Digital Interface							
V_{IH}	High-level input voltage			2.5		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
V_{OH}	High-level output voltage			$0.8V_{CC}$			V
V_{OL}	Low-level output voltage					$0.2V_{CC}$	V

TIMING REQUIREMENTS

Supply voltage = 4.5V to 5.25V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CLK)}$	Clock period		50			ns
t_{su1}	Setup time, data		10			ns
t_h	Hold time, data		10			ns
t_w	Pulse width, STROBE		20			ns
t_{su2}	Setup time, STROBE		10			ns



A. The first 4 bits, DB(3-0), of data are Address bits. The 28 remaining bits, DB(31-4), are part of the command. The command is little endian or lower bits first.

Figure 1. Serial Programming Timing Diagram

PRODUCT PREVIEW

TRF3761-1579 ELECTRICAL CHARACTERISTICS

Supply voltage = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1579MHz, f_O = 1579MHz	100kHz offset		–116		dBc/Hz
		600kHz offset		–138.5		
		1MHz offset		-141		
		6MHz offset		–156		
		10MHz offset		–159.5		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1579MHz, f_O = c	100kHz offset		–122		dBc/Hz
		600kHz offset		–143		
		1MHz offset		–148		
		6MHz offset		–157.5		
		10MHz offset		–158.5		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1579MHz, f_O = 394.75MHz	100kHz offset		–126		dBc/Hz
		600kHz offset		-149		
		1MHz offset		-152.4		
		6MHz offset		–155.5		
		10MHz offset		–155.7		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1579MHz, f_O = 1579MHz	1kHz offset		–85.5		dBc/Hz
		600kHz offset		–136		
		1MHz offset		–140.5		
		10MHz offset		–158.9		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.84°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1579MHz, f_O = 789.5MHz	1kHz offset		–91.5		dBc/Hz
		600kHz offset		–143.5		
		1MHz offset		–147		
		10MHz offset		–158.3		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.37°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1579MHz, f_O = 394.75MHz	1kHz offset		-97.5		dBc/Hz
		600kHz offset		–149		
		1MHz offset		–152		
		10MHz offset		–155.7		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.17°		
VCO gain	VCO free running			30		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

PRODUCT PREVIEW

TRF3761-1700 ELECTRICAL CHARACTERISTICS

Supply voltage = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1700MHz, f_O = 1700MHz	100kHz offset		–120		dBc/Hz
		600kHz offset		–138		
		1MHz offset		-143		
		6MHz offset		–156		
		10MHz offset		–158		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1700MHz, f_O = 850	100kHz offset		–127		dBc/Hz
		600kHz offset		–144.5		
		1MHz offset		–149.5		
		6MHz offset		–157.5		
		10MHz offset		–158.4		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1700MHz, f_O = 425MHz	100kHz offset		–134		dBc/Hz
		600kHz offset		-150.5		
		1MHz offset		-153.8		
		6MHz offset		–156		
		10MHz offset		–156.3		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1700MHz, f_O = 1700MHz	1kHz offset		–84		dBc/Hz
		600kHz offset		–138		
		1MHz offset		–141		
		10MHz offset		–157.5		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			0.86°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1700MHz, f_O = 850MHz	1kHz offset		–90		dBc/Hz
		600kHz offset		–144.5		
		1MHz offset		–148		
		10MHz offset		–158		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.39°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1700MHz, f_O = 425MHz	1kHz offset		–97.5		dBc/Hz
		600kHz offset		–150		
		1MHz offset		–159		
		10MHz offset		–156		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.17°		
VCO gain	VCO free running			30		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
www.ti.com

TRF3761-1817 ELECTRICAL CHARACTERISTICS

Supply voltage = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1817MHz, f_O = 1817MHz	100kHz offset		–120		dBc/Hz
		600kHz offset		–138.5		
		1MHz offset		-143.5		
		6MHz offset		–157		
		10MHz offset		–159		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1817MHz, f_O = 908.5MHz	100kHz offset		–126.5		dBc/Hz
		600kHz offset		–145		
		1MHz offset		–150		
		6MHz offset		–156.5		
		10MHz offset		–159		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1817MHz, f_O = 454.25MHz	100kHz offset		–131		dBc/Hz
		600kHz offset		-149.5		
		1MHz offset		-154		
		6MHz offset		–159		
		10MHz offset		–159		
VCO phase noise, Closed loop phase noise direct output[1][2][1]	f_{VCO} = 1817MHz, f_O = 1817MHz	1kHz offset		–84		dBc/Hz
		600kHz offset		–138.5		
		1MHz offset		–143.5		
		10MHz offset		–159		
RMS phase error Closed loop phase noise direct output[1]	100Hz to 10MHz			1°		
VCO phase noise, Closed loop phase noise divide-by-2 output[1][3][4]	f_{VCO} = 1817MHz, f_O = 908.5MHz	1kHz offset		–94		dBc/Hz
		600kHz offset		–145		
		1MHz offset		–150		
		10MHz offset		–159		
RMS phase error Closed loop phase noise divide-by-2 output[3]	100Hz to 10MHz			0.35°		
VCO phase noise, Closed loop phase noise divide-by-4 output[1][3][5]	f_{VCO} = 1817MHz, f_O = 454.25MHz	1kHz offset		–100		dBc/Hz
		600kHz offset		–149.5		
		1MHz offset		–154		
		10MHz offset		–159		
RMS phase error Closed loop phase noise divide-by-4 output[3]	100Hz to 10MHz			0.19°		
VCO gain	VCO free running			30		MHz/V
Reference spur[2]				–80		dBc

(1) See Application Circuit
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.
(4) PFD = 400kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(5) PFD = 400kHz, Loop Filter BW = 15kHz, Output frequency step = 100kHz.

PRODUCT PREVIEW

TRF3761-1947 ELECTRICAL CHARACTERISTICS

Supply voltage = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 1947MHz, f_O = 1947MHz	100kHz offset		–117		dBc/Hz
		600kHz offset		–133		
		1MHz offset		-141		
		6MHz offset		–155		
		10MHz offset		–158.5		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 1947MHz, f_O = 973.5	100kHz offset		–125		dBc/Hz
		600kHz offset		–144		
		1MHz offset		–148		
		6MHz offset		–158		
		10MHz offset		–159		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 1947MHz, f_O = 486.75MHz	100kHz offset		–131		dBc/Hz
		600kHz offset		-150		
		1MHz offset		-153		
		6MHz offset		–156.5		
		10MHz offset		–157		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 1947MHz, f_O = 1947MHz	1kHz offset		–83.7		dBc/Hz
		600kHz offset		–136		
		1MHz offset		–140		
		10MHz offset		–158		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			1°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 1947MHz, f_O = 973.5MHz	1kHz offset		-89.5		dBc/Hz
		600kHz offset		–143.5		
		1MHz offset		–147.4		
		10MHz offset		–159		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.43°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 1947MHz, f_O = 486.75MHz	1kHz offset		–95.5		dBc/Hz
		600kHz offset		–149		
		1MHz offset		–152.5		
		10MHz offset		-157		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.2°		
VCO gain	VCO free running			30		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

PRODUCT PREVIEW

PRODUCT PREVIEW

TRF3761-2116 ELECTRICAL CHARACTERISTICS

Supply voltage = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 2116MHz, f_O = 2116MHz	100kHz offset		–117		dBc/Hz
		600kHz offset		–136		
		1MHz offset		-140		
		6MHz offset		–154		
		10MHz offset		–156		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 2116MHz, f_O = 1058	100kHz offset		–124		dBc/Hz
		600kHz offset		–142.5		
		1MHz offset		–147		
		6MHz offset		–157.3		
		10MHz offset		–158		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 2116MHz, f_O = 529MHz	100kHz offset		–130		dBc/Hz
		600kHz offset		-149		
		1MHz offset		-152		
		6MHz offset		–156.5		
		10MHz offset		–157		
VCO phase noise, Closed loop phase noise direct output[1][2][3]	f_{VCO} = 2116MHz, f_O = 2116MHz	1kHz offset		–83.5		dBc/Hz
		600kHz offset		–136		
		1MHz offset		–139		
		10MHz offset		–157		
RMS phase error Closed loop phase noise direct output[3]	100Hz to 10MHz			1.13°		
VCO phase noise, Closed loop phase noise divide-by-2 output[1][2][3]	f_{VCO} = 2116MHz, f_O = 1058MHz	1kHz offset		-89		dBc/Hz
		600kHz offset		–142.5		
		1MHz offset		–146.5		
		10MHz offset		–158		
RMS phase error Closed loop phase noise divide-by-2 output[3]	100Hz to 10MHz			0.5°		
VCO phase noise, Closed loop phase noise divide-by-4 output[1][2][3]	f_{VCO} = 2116MHz, f_O = 529MHz	1kHz offset		–95		dBc/Hz
		600kHz offset		–148.5		
		1MHz offset		–151.5		
		10MHz offset		–157		
RMS phase error Closed loop phase noise divide-by-4 output[3]	100Hz to 10MHz			0.23°		
VCO gain	VCO free running			30		MHz/V
Reference spur[2]				–80		dBc

(1) See Application Circuit
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

TRF3761-2289 ELECTRICAL CHARACTERISTICS

Supply voltage = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE CHARACTERISTICS						
VCO phase noise, Free running VCO direct output	f_{VCO} = 2289MHz, f_O = 2289MHz	100kHz offset		–116		dBc/Hz
		600kHz offset		–135		
		1MHz offset		-138		
		6MHz offset		–153		
		10MHz offset		–155		
VCO phase noise, Free running VCO divide-by-2 output	f_{VCO} = 2289MHz, f_O = 1144.5	100kHz offset		–124		dBc/Hz
		600kHz offset		–141		
		1MHz offset		–145		
		6MHz offset		–156		
		10MHz offset		–157.5		
VCO phase noise, Free running VCO divide-by-4 output	f_{VCO} = 2289MHz, f_O = 572.25MHz	100kHz offset		–129.5		dBc/Hz
		600kHz offset		-147.5		
		1MHz offset		-150.5		
		6MHz offset		–156.5		
		10MHz offset		–157		
VCO phase noise, Closed loop phase noise direct output(1)(2)(3)	f_{VCO} = 2289MHz, f_O = 2289MHz	1kHz offset		–82.5		dBc/Hz
		600kHz offset		–134		
		1MHz offset		–137.5		
		10MHz offset		–155		
RMS phase error Closed loop phase noise direct output(3)	100Hz to 10MHz			1.22°		
VCO phase noise, Closed loop phase noise divide-by-2 output(1)(2)(3)	f_{VCO} = 2289MHz, f_O = 1144.5MHz	1kHz offset		–88		dBc/Hz
		600kHz offset		-141		
		1MHz offset		–144.5		
		10MHz offset		–157		
RMS phase error Closed loop phase noise divide-by-2 output(3)	100Hz to 10MHz			0.55°		
VCO phase noise, Closed loop phase noise divide-by-4 output(1)(2)(3)	f_{VCO} = 2289MHz, f_O = 572.25MHz	1kHz offset		–94		dBc/Hz
		600kHz offset		–147		
		1MHz offset		–150.5		
		10MHz offset		–157		
RMS phase error Closed loop phase noise divide-by-4 output(3)	100Hz to 10MHz			0.26°		
VCO gain	VCO free running			30		MHz/V
Reference spur(2)				–80		dBc

(1) See Application Circuit
(2) PFD = 200kHz, Loop Filter BW = 15kHz, Output frequency step = 200kHz.
(3) Reference oscillator RMS phase error = 0.008250°, RMS jitter = 881.764 fs.

PRODUCT PREVIEW

TRF3761-1817 TYPICAL CHARACTERISTICS

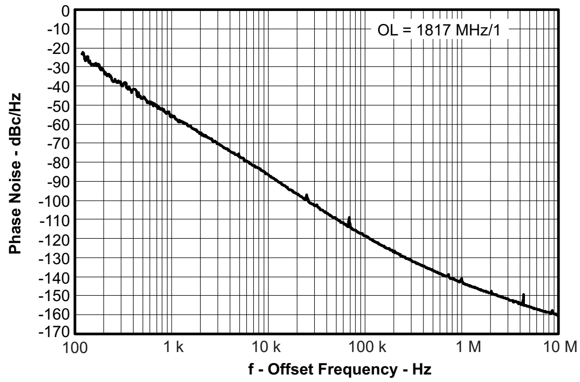


Figure 2. Open Loop VCO Phase Noise

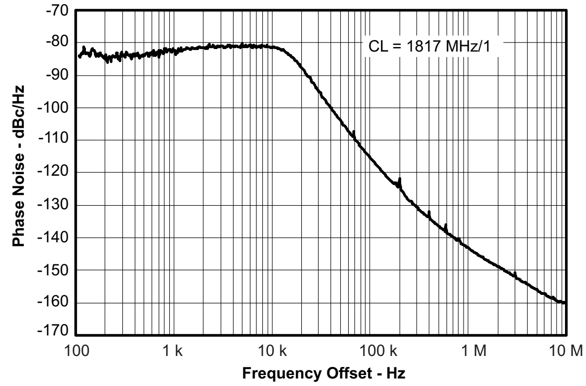


Figure 3. Closed Loop VCO Phase Noise

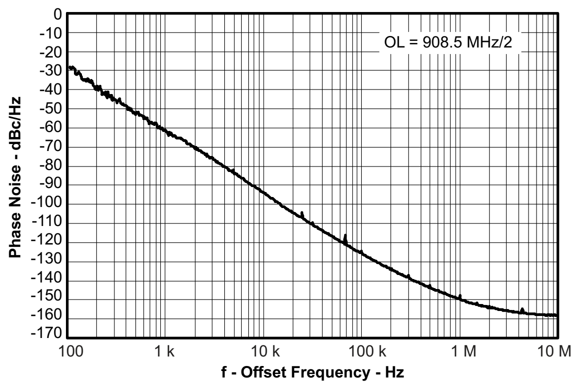


Figure 4. Open Loop VCO Phase Noise

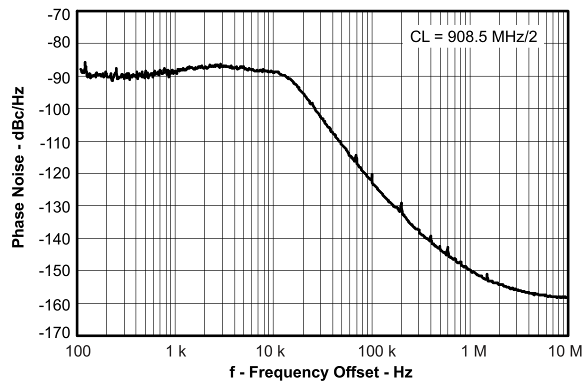


Figure 5. Closed Loop VCO Phase Noise

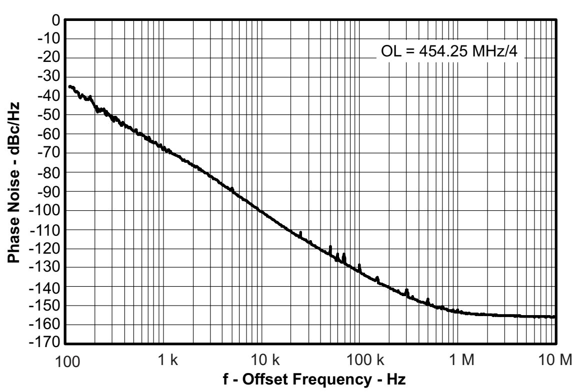


Figure 6. Open Loop VCO Phase Noise

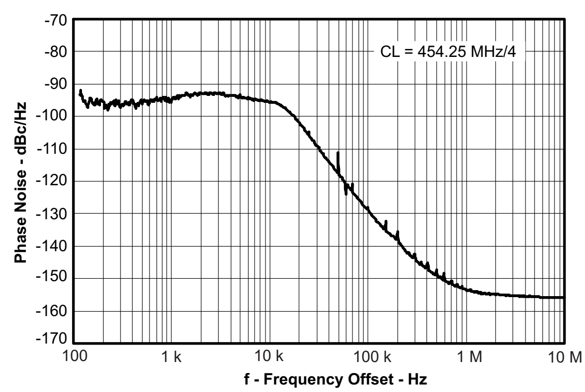


Figure 7. Closed Loop VCO Phase Noise

TRP3761-1579 TYPICAL CHARACTERISTICS

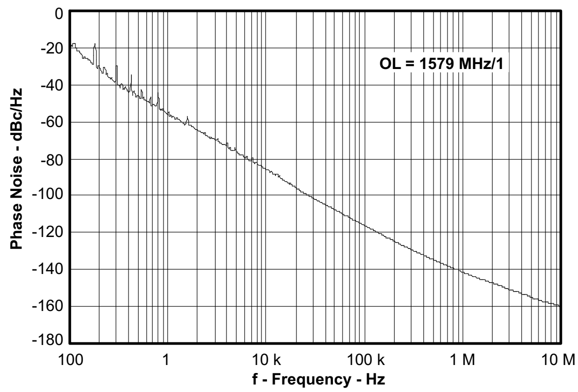


Figure 8. Open Loop VCO Phase Noise

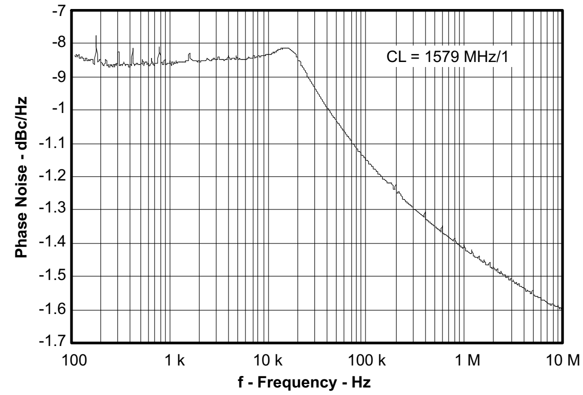


Figure 9. Closed Loop VCO Phase Noise

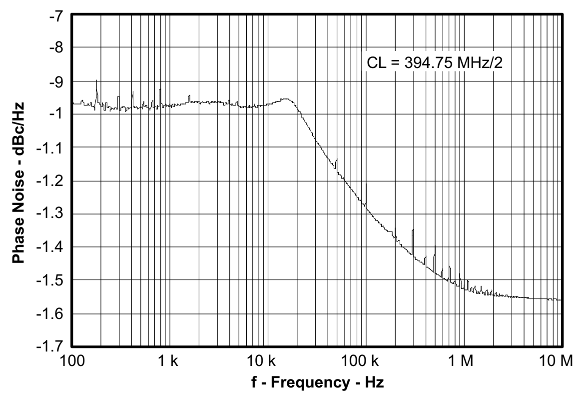


Figure 10. Open Loop VCO Phase Noise

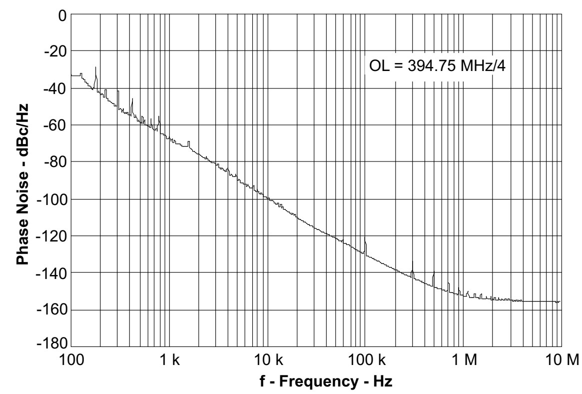


Figure 11. Closed Loop VCO Phase Noise

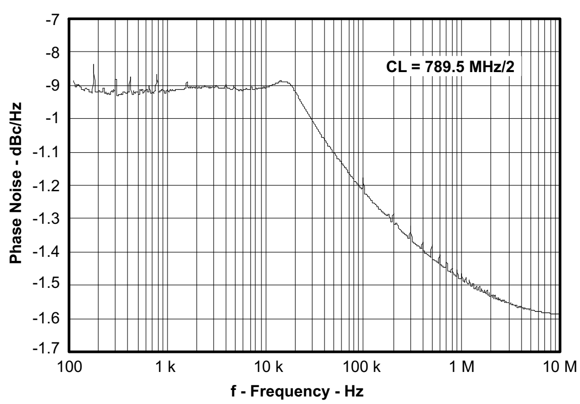


Figure 12. Open Loop VCO Phase Noise

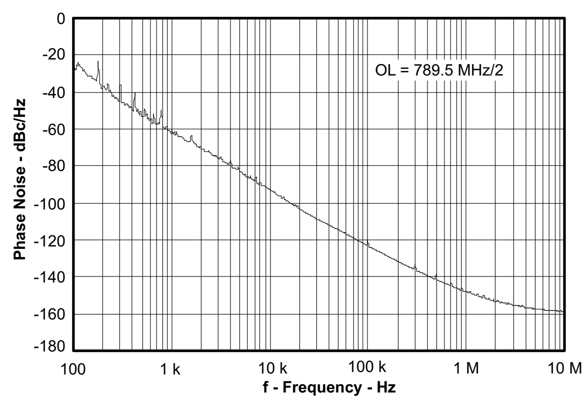


Figure 13. Closed Loop VCO Phase Noise

PRODUCT PREVIEW

TRP3761-1579 TYPICAL CHARACTERISTICS (continued)

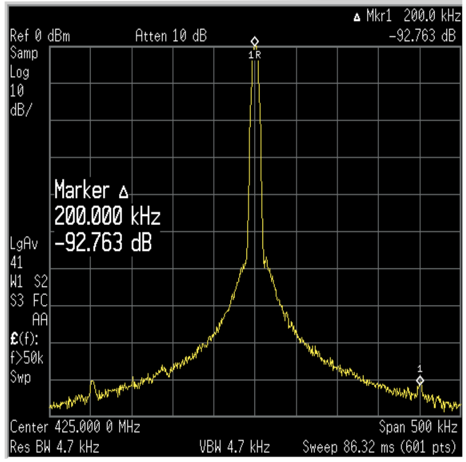


Figure 14. Direct Output: PFD Frequency Spurs

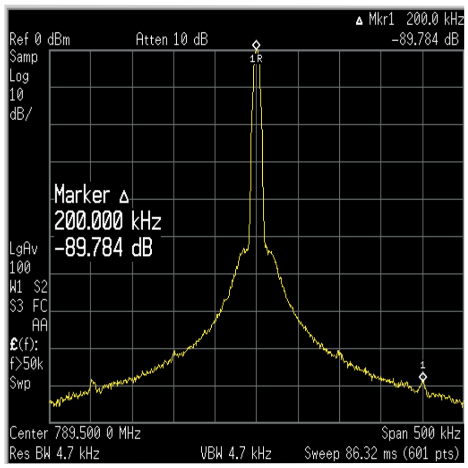


Figure 15. Divide-By-2 Output: PFD Frequency Spurs

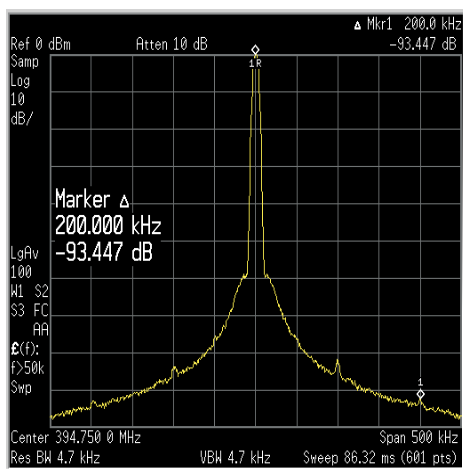


Figure 16. Divide-By-4 Output: PFD Frequency Spurs

TRP3761-1700 TYPICAL CHARACTERISTICS

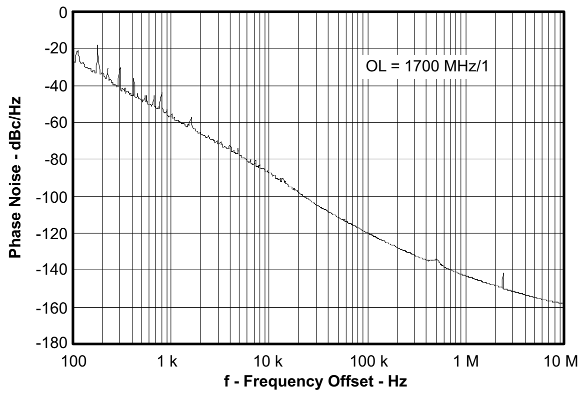


Figure 17. Open Loop VCO Phase Noise

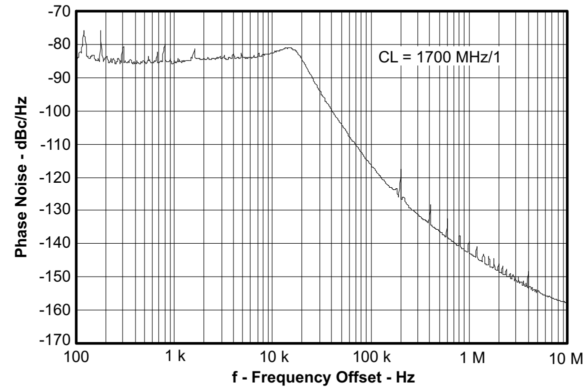


Figure 18. Closed Loop VCO Phase Noise

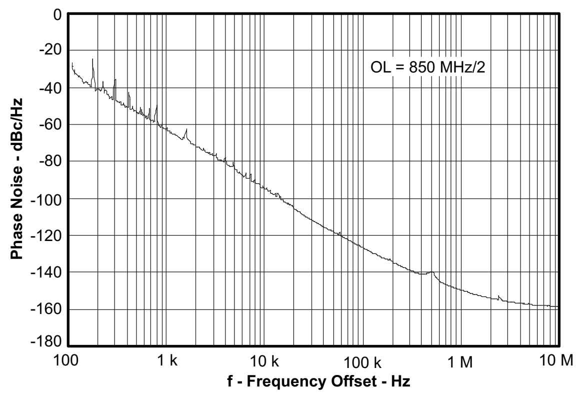


Figure 19. Open Loop VCO Phase Noise

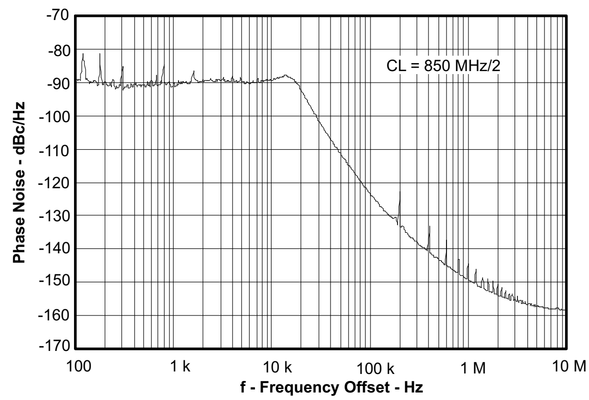


Figure 20. Closed Loop VCO Phase Noise

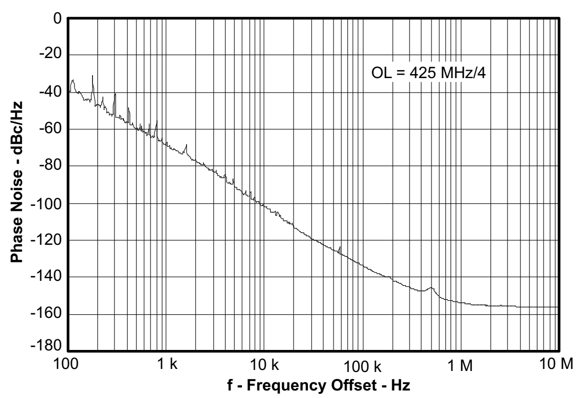


Figure 21. Open Loop VCO Phase Noise

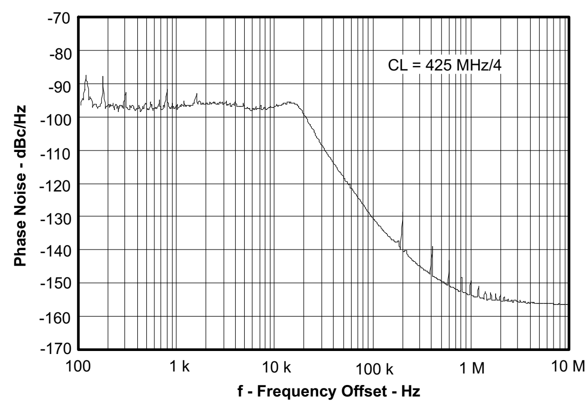


Figure 22. Closed Loop VCO Phase Noise

PRODUCT PREVIEW

TRP3761-1700 TYPICAL CHARACTERISTICS (continued)

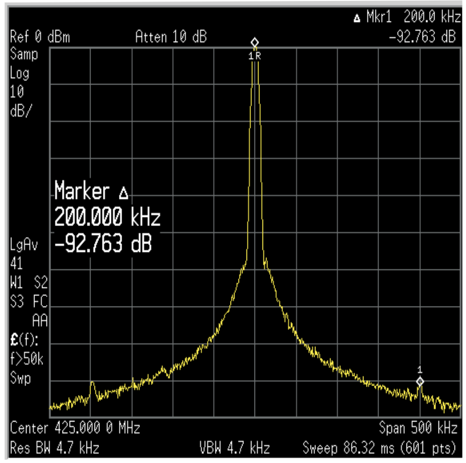


Figure 23. Direct Output: PFD Frequency Spurs

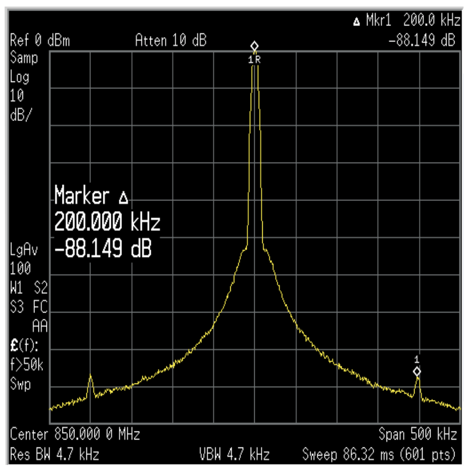


Figure 24. Divide-By-2 Output: PFD Frequency Spurs

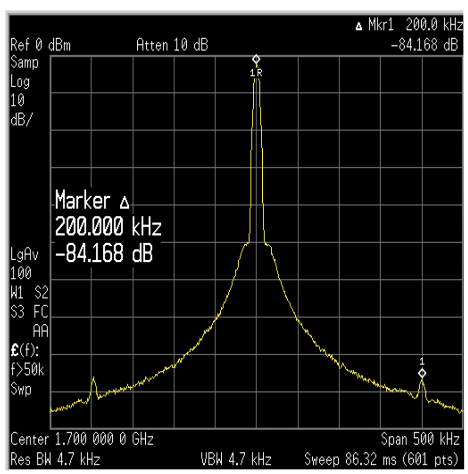


Figure 25. Divide-By-4 Output: PFD Frequency Spurs

TRF3761-1817 TYPICAL CHARACTERISTICS (Continued)

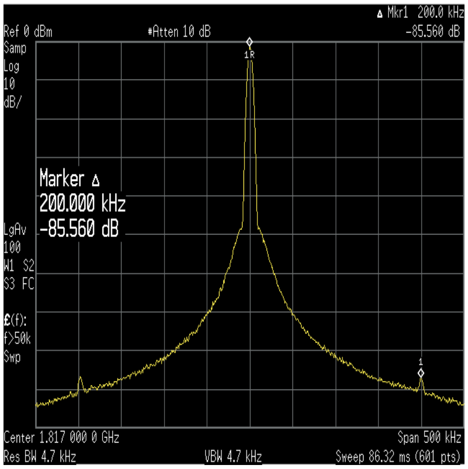


Figure 26. Direct Output: PFD Frequency Spurs

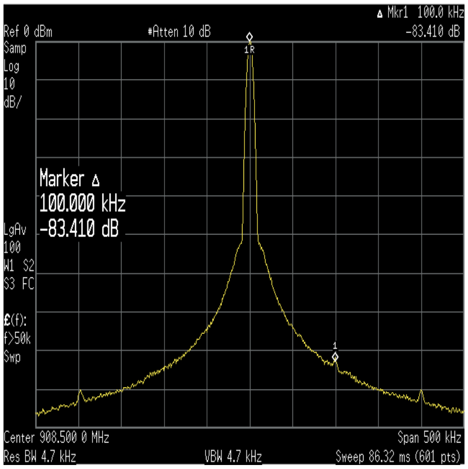


Figure 27. Divide-By-2 Output: PFD Frequency Spurs

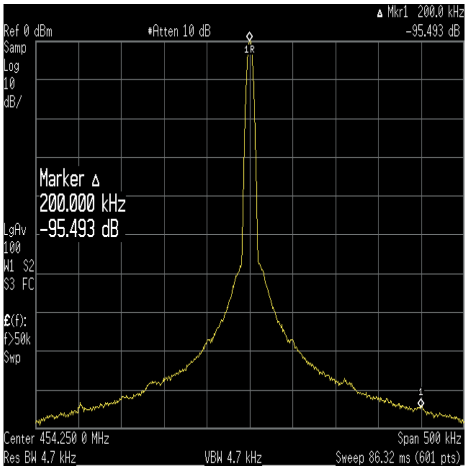


Figure 28. Divide-By-4 Output: PFD Frequency Spurs

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TRP3761-1947 TYPICAL CHARACTERISTICS

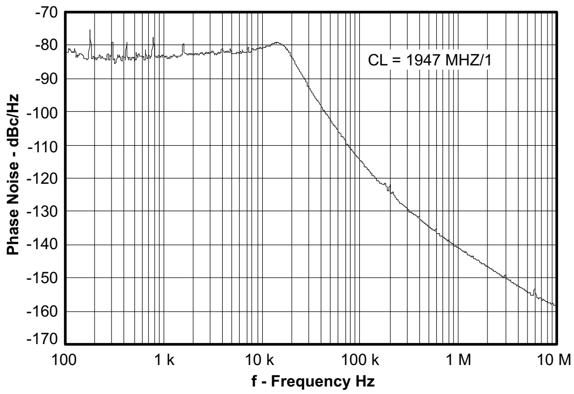

Figure 29. Open Loop VCO Phase Noise

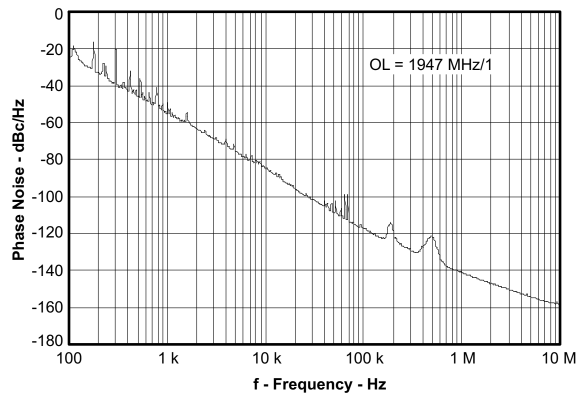

Figure 30. Closed Loop VCO Phase Noise

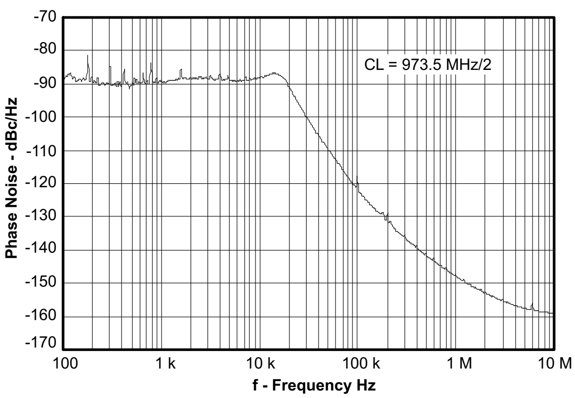

Figure 31. Open Loop VCO Phase Noise

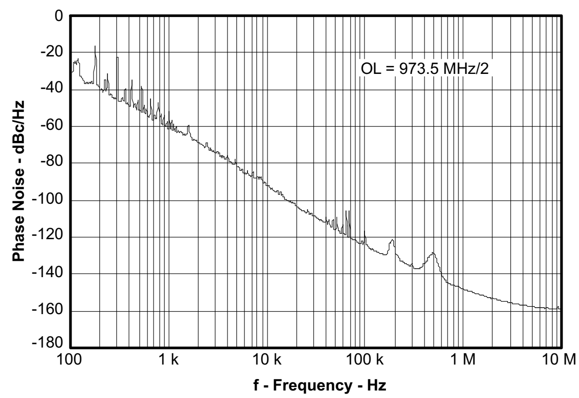

Figure 32. Closed Loop VCO Phase Noise

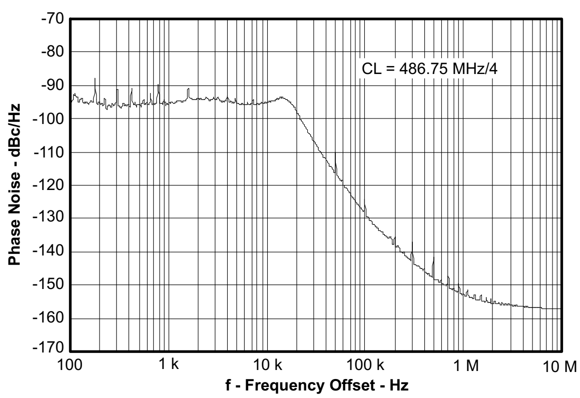

Figure 33. Open Loop VCO Phase Noise

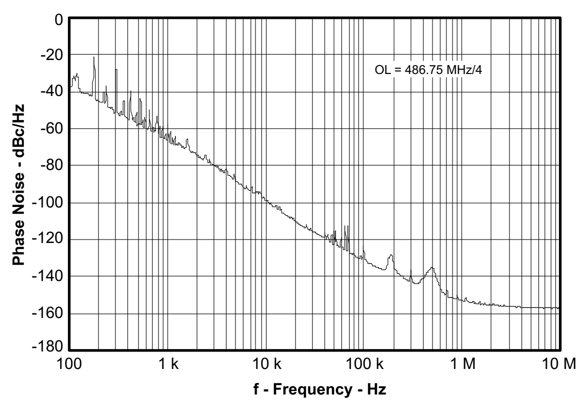

Figure 34. Closed Loop VCO Phase Noise

PRODUCT PREVIEW

TRP3761-1947 TYPICAL CHARACTERISTICS (continued)

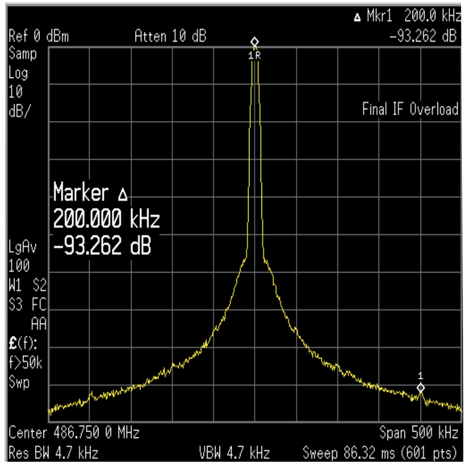

Figure 35. Direct Output: PFD Frequency Spurs

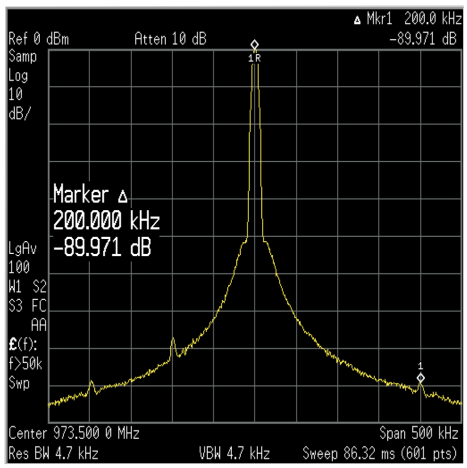

Figure 36. Divide-By-2 Output: PFD Frequency Spurs

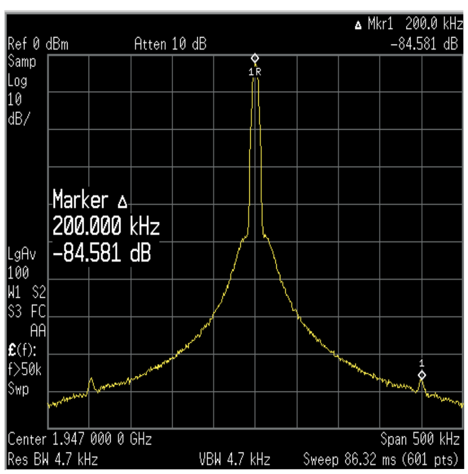

Figure 37. Divide-By-4 Output: PFD Frequency Spurs

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TRP3761-2116 TYPICAL CHARACTERISTICS

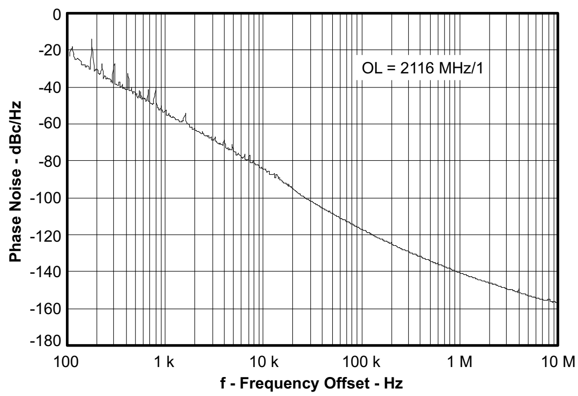

Figure 38. Open Loop VCO Phase Noise

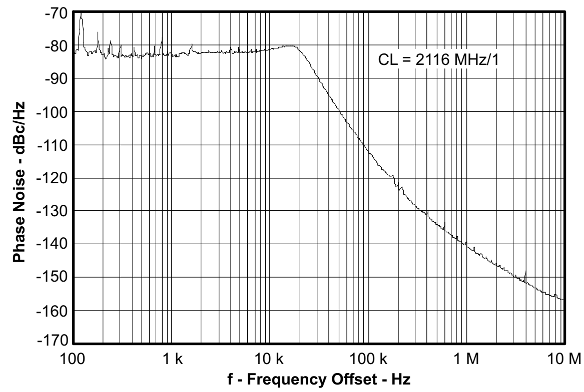

Figure 39. Closed Loop VCO Phase Noise

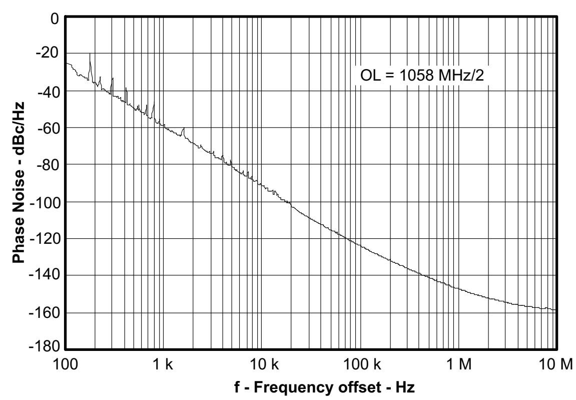

Figure 40. Open Loop VCO Phase Noise

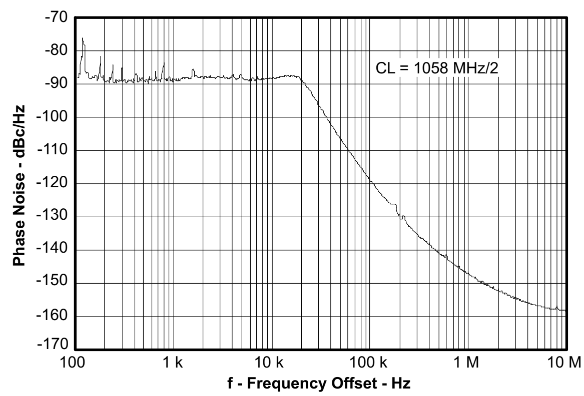

Figure 41. Closed Loop VCO Phase Noise

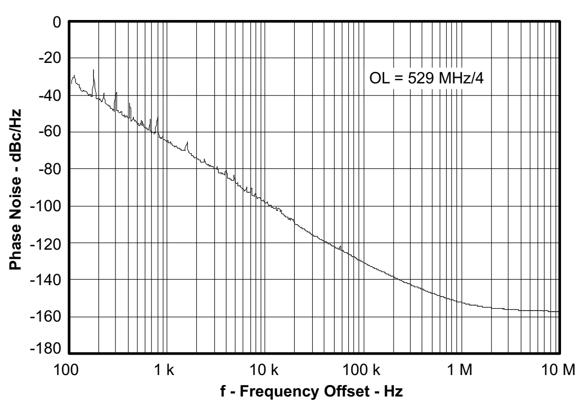

Figure 42. Open Loop VCO Phase Noise

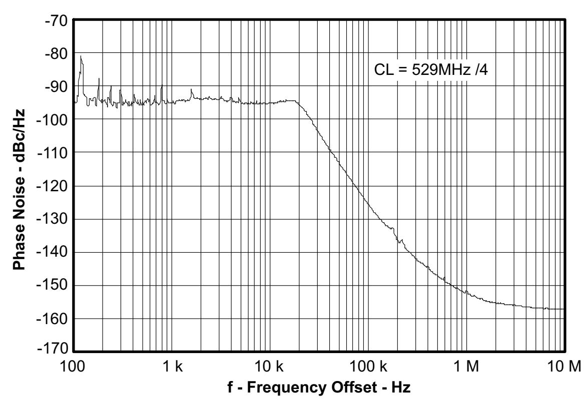

Figure 43. Closed Loop VCO Phase Noise

PRODUCT PREVIEW

TRP3761-2116 TYPICAL CHARACTERISTICS (continued)

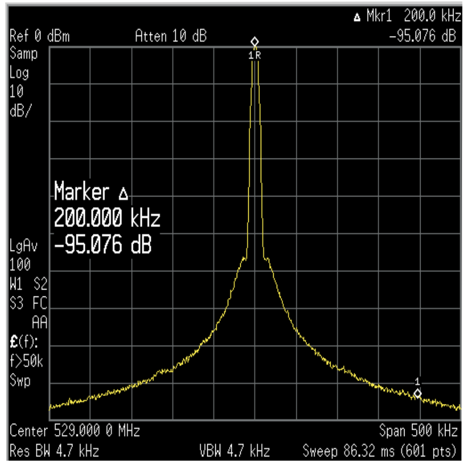

Figure 44. Direct Output: PFD Frequency Spurs

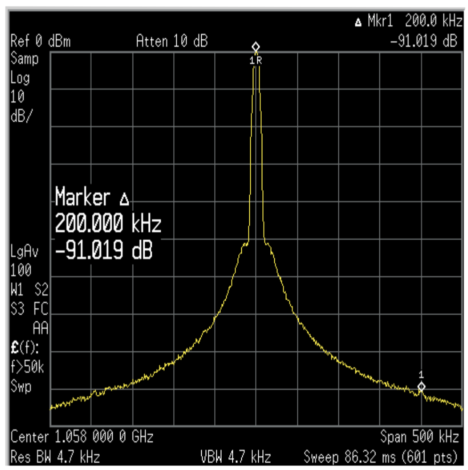

Figure 45. Divide-By-2 Output: PFD Frequency Spurs

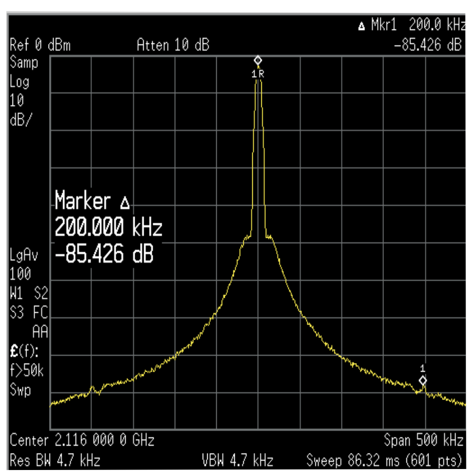

Figure 46. Divide-By-4 Output: PFD Frequency Spurs

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TRP3761-2289 TYPICAL CHARACTERISTICS

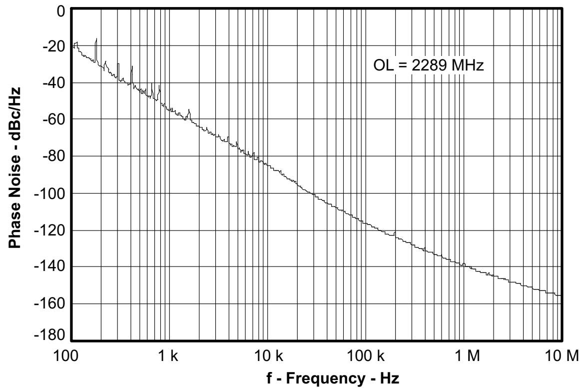

Figure 47. Open Loop VCO Phase Noise

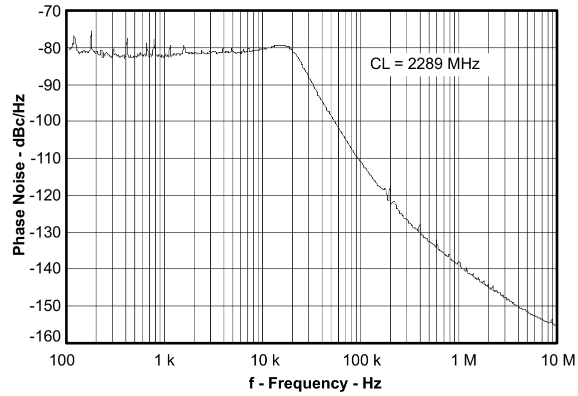

Figure 48. Closed Loop VCO Phase Noise

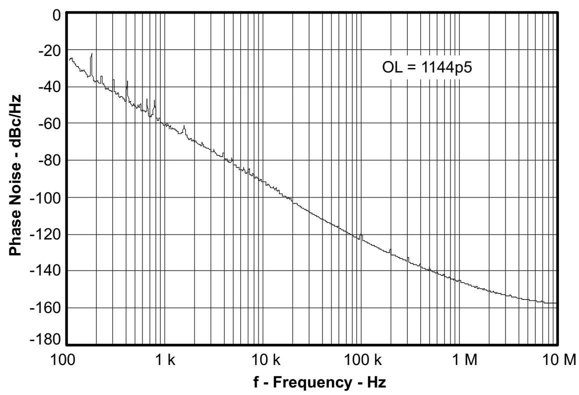

Figure 49. Open Loop VCO Phase Noise

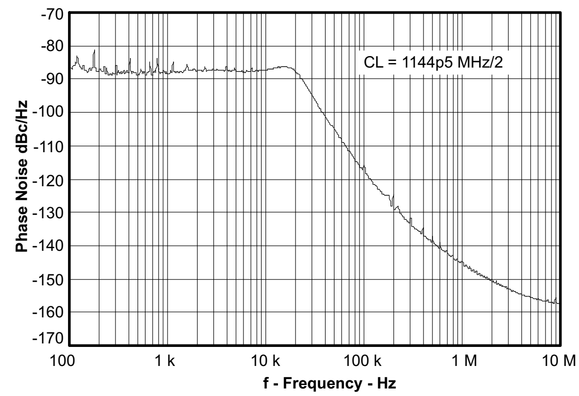

Figure 50. Closed Loop VCO Phase Noise

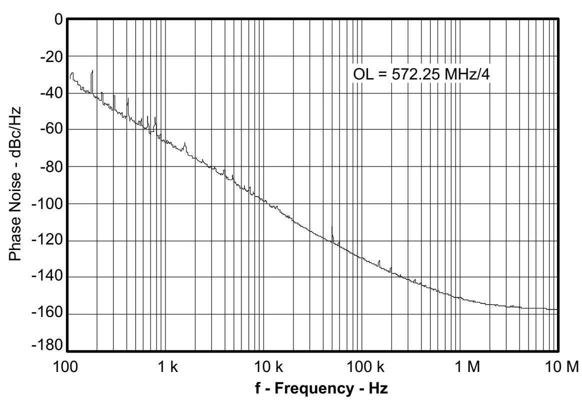

Figure 51. Open Loop VCO Phase Noise

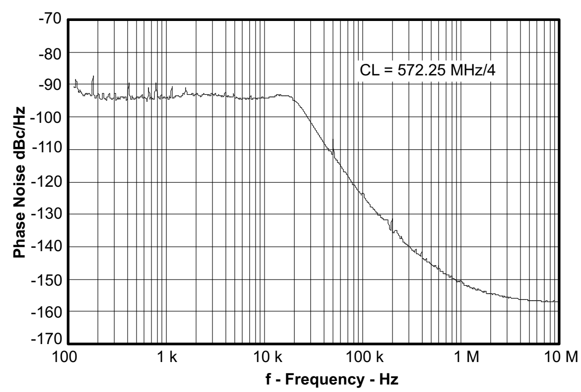

Figure 52. Closed Loop VCO Phase Noise

TRP3761-2289 TYPICAL CHARACTERISTICS (continued)

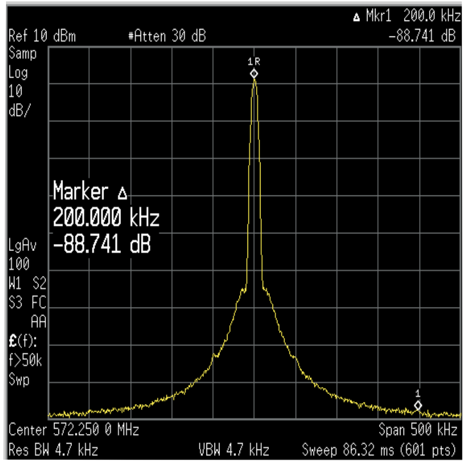

Figure 53. Direct Output: PFD Frequency Spurs

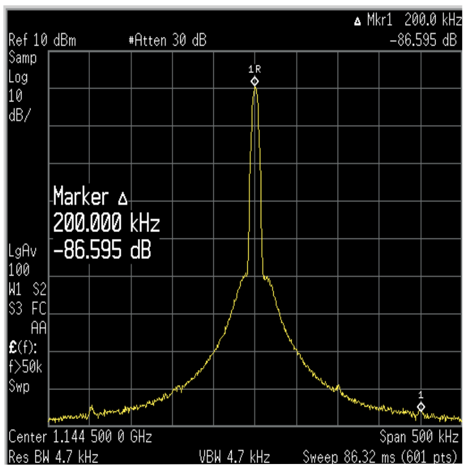

Figure 54. Divide-By-2 Output: PFD Frequency Spurs

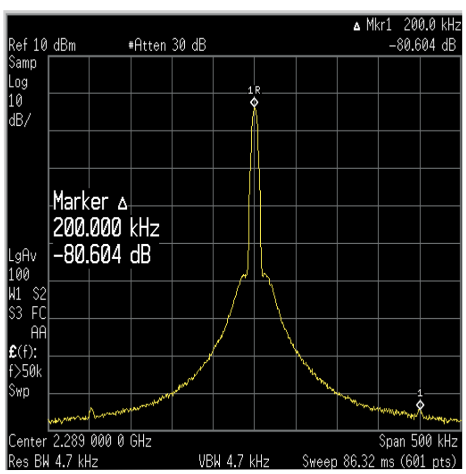

Figure 55. Divide-By-4 Output: PFD Frequency Spurs

PRODUCT PREVIEW

SERIAL INTERFACE PROGRAMMING REGISTERS DEFINITION

The TRF3761 features a 3-wire serial programming interface that controls an internal, 32-bit shift register. There are a total of 3 signals that need to be applied: the CLOCK (pin 3), the serial DATA (pin 4) and the STROBE (pin 5). The DATA (DB0-DB31) is loaded LSB first and is read on the rising edge of the CLOCK. The STROBE is asynchronous to the CLOCK and at it's rising edge the data in the shift register gets loaded onto the selected internal register. The first four bits (DB0-DB3) is the address to select the available internal registers.

Table 1. Register 1: Device Setup

REGISTER 1 MAPPING				
Data Field	**DB31**	FULL_CAL_REQ	This is a read only bit, that indicates if a power-up cal is required	0 power-up cal is not required 1 power-up cal is required
	DB30	CP_TEST	Up and down pulse charge pump test	1 test enabled
	DB29	TRIS_CP	High-impedance state charge pump output	1 CP high-impedance state
	DB28	PFD_POL	Select Polarity of PFD	0 negative 1 positive
	DB27	ABPW1	ABPW<1,0>: antibacklash pulse width	00 1.5ns delay 01 0.9ns delay 10 3.8ns delay 11 2.7ns delay
	DB26	ABPW0		
	DB25	RDIV_13	14-bit reference clock divider	RDIV<13,0>:00...01: divide by 1 RDIV<13,0>:00...10: divide by 2 RDIV<13,0>:00...11: divide by 3
	DB24	RDIV_12		
	DB23	RDIV_11		
	DB22	RDIV_10		
	DB21	RDIV_9		
	DB20	RDIV_8		
	DB19	RDIV_7		
	DB18	RDIV_6		
	DB17	RDIV_5		
	DB16	RDIV_4		
	DB15	RDIV_3		
	DB14	RDIV_2		
	DB13	RDIV_1		
	DB12	RDIV_0		
	DB11	PD_BUFOUT	If Bit10 = 0 then it controls power down of output buffer	<DB10:11>: 00 default; output buffer on 01 output buffer off 1x output buffer on/off controlled by OUTBUF_EN pin
	DB10	OUTBUF_EN_SEL	Select Output Buffer enable control: 0 internal 1 through OUTBUF_EN pin	
	DB9	OUT_MODE_1	OUTBUFMODE<1,0>: Selection of RF output buffer division ratio	00 divide by 1 01 divide by 2 10 divide by4
	DB8	OUT_MODE_0	ICP<2,0>: select charge pump current (1 mA step)	
	DB7	ICP2		
	DB6	ICP1		
	DB5	ICP0		
	DB4	RESET	Registers reset	

PRODUCT PREVIEW

Table 1. Register 1: Device Setup (continued)

REGISTER 1 MAPPING				
Address Bits	**DB3**	0		
	DB2	0		
	DB1	0		
	DB0	0		

OUT_MODE<1,0>: TRF3761 has an optional divide by 2 or 4 output, which is selectable by programming bits <OUT_MODE_1, OUT_MODE_0> of register 1 (see Table 1).

Up and Down Pulse Test: By setting bit DB30 to 1 it is possible to test the PFD up or down pulses.

Charge Pump Tristate: If bit DB29 is set to 1, the charge pump output goes in tri-state. For normal operation, DB29 must be set to 0.

Anti-Backlash Pulse: Bits <DB27, DB26> are used to program the width of the anti-backlash pulses of the PFD. The user selects one of the following values: 0.9ns, 1.5ns, 2.7ns and 3.8ns.

PFD Polarity: Bit DB28 of register 0 sets the polarity of the PFD: A 0 selects a negative polarity, and a 1 selects a positive polarity. By choosing the correct polarity, the TRF3761 works with an external VCO having both positive and negative Kv.

Reference Divider: A 14-bit word programs the R divider for the reference signal, DB25 is the MSB and DB12 is the LSB.

Charge Pump Current: Bits <DB7, DB5> set the charge pump current.

OUTBUF_EN_SEL: Output buffer on/off state is controlled through serial interface or an external pin. If bit DB10 is a 0 (default state) the output buffers state is elected through bit DB11. If DB10 is a 1, the buffers on/off are directly controlled by the OUTBU_EN pin.

Reset: Setting bit DB4 to 1, all registers are reset to default values.

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Table 2. Register 2: VCO Calibration

REGISTER 2 MAPPING				
Data Field	**DB31**	START_CAL	VCO frequency in MHz start calibration	1 start calibration
	DB30	FOUT12		
	DB29	FOUT11		
	DB28	FOUT10		
	DB27	FOUT9		
	DB26	FOUT8		
	DB25	FOUT7		
	DB24	FOUT6		
	DB23	FOUT5		
	DB22	FOUT4		
	DB21	FOUT3		
	DB20	FOUT2		
	DB19	FOUT1		
	DB18	FOUT0		
	DB17	REF_FRAC6	Reference frequency in MHz (fractional part)	0000000 = X.00MHz 0000001 = X.01MHz 0000010 = X.02MHz . . . . . 1100011 = X.99MHz
	DB16	REF_FRAC5		
	DB15	REF_FRAC4		
	DB14	REF_FRAC3		
	DB13	REF_FRAC2		
	DB12	REF_FRAC1		
	DB11	REF_FRAC0		
	DB10	REF6	Reference frequency in MHz (integer part)	0001010 =10MHz 0001011 =11MHz . . . . . 1101000 = 104MHz
	DB9	REF5		
	DB8	REF4		
	DB7	REF3		
	DB6	REF2		
	DB5	REF1		
	DB4	REF0		
Address Bits	**DB3**	0		
	DB2	0		
	DB1	0		
	DB0	1		

Reference Frequency: The 14 bits <DB17, DB4> are used to specify the input reference frequency as multiples of 10kHz. Bits <DB10,DB4> specify the integer part of the reference frequency expressed in MHz. Bits <DB17,DB11> set the fraction part. Those values are then used during the calibration of the internal VCO.

Start Calibration: A 1 in DB31 starts the internal VCO calibration. When the calibration is complete, DB31 bit is internally reset to 0.

FOUT<12,0>: This 13-bit word <DB30,DB18> specifies the VCO output frequency in MHz. If output frequency is not a integer multiple of MHz, this value must be approximated to the closest integer in MHz.

Table 3. Register 3: A and B Counters

REGISTER 3 MAPPING				
Data Field	**DB31**	Rsrv	Reserved	
	DB30	Rsrv	Reserved	
	DB29	START_LK	Lock PLL to frequency	1 active
	DB28	TEST_MUX_3		0001 = LOCK_DETECT enabled
	DB27	TEST_MUX_2		
	DB26	TEST_MUX_1		
	DB25	TEST_MUX_0		
	DB24	B_12	13-bit B counter	
	DB23	B_11		
	DB22	B_10		
	DB21	B_9		
	DB20	B_8		
	DB19	B_7		
	DB18	B_6		
	DB17	B_5		
	DB16	B_4		
	DB15	B_3		
	DB14	B_2		
	DB13	B_1		
	DB12	B_0		
	DB11	A_5	6-bit A counter	
	DB10	A_4		
	DB9	A_3		
	DB8	A_2		
	DB7	A_1		
	DB6	A_0		
	DB5	PRESC_MOD1	Dual-modulus prescaler mode	<B5,B4>:00 8/9 <B5,B4>:01 16/17 <B5,B4>:10 32/33 <B5,B4>:11 64/65
	DB4	PRESC_MOD0		
Address Bits	**DB3**	0		
	DB2	0		
	DB1	1		
	DB0	0		

B<12,0>: This 13-bit word <DB24,DB12> controls the value of the B counter of the N divider. The valid range is from 3 to 8191.

A<5,0>: These 6 bits <DB11,DB6> control the value of the A counter. The valid range is from 0 to 63.

PRESC_MOD<1,0>: These bits <DB5,DB4> define the mode of the dual-modulus prescaler according Table 3.

START_LK: TRF3761 does not load the serial interface registers values into the dividers registers until bit DB29 of register 3 is set to 1. After TRF3761 is locked to the new frequency, bit DB29 is internally reset to 0.

PRODUCT PREVIEW

FUNCTIONAL DESCRIPTION

VCO

TRF3761 integrates a high-performance, LC tank, voltage-controlled oscillator (VCO). For each of the devices of TRF3761 family, the inductance and capacitance of the tank are optimized to yield best phase-noise performance. The VCO output is fed externally and to the prescaler through a series of very low noise buffers, that greatly reduce the effect of load pulling onto the VCO.

Divider by 2, by 4, and Output Buffer

To extend the frequency coverage, the TRF3761 integrates a divider by 2 and by 4 with very low noise floor. The VCO signal is fed externally through a final open-collector differential-output buffer. This buffer is able to provide up to 3dBm (typical) of power into a 200Ω differential resistive load. The open-collector structure gives the flexibility to choose different load configurations to meet different requirements.

Prescaler Stage

This stage divides down the VCO frequency before the A and B counters. This is a dual-modulus prescaler and the user can select any of the following settings: 8/9, 16/17, 32/33, and 64/65.

A and B Counter Stage

The TRF3761 includes a 6-bit A counter and a 13-bit B counter that operate on the output of the prescaler. The A counter can take values from 0 to 63, while the B counter can take values from 3 to 8191. Also, the value for the B counter must be greater than or equal to the value for the A counter. The A and B counter with the prescaler stage create the VCO N-divider.

R Divider

TRF3761 includes a 14-bit R divider that allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

Phase Frequency Detector (PFD) and Charge Pump Stage

The outputs of the R divider and the N counter are fed into the PFD stage, where the two signals are compared in frequency and phase. The TRF3761 features an anti-backlash pulse, whose width is controllable by the user through the serial programming interface. The PFD feeds the charge pump, whose output current pulses are fed into an external loop filter, which eventually produces the tuning voltage needed to control the integrated VCO to the desired frequency.

APPLICATION INFORMATION

Initial Calibration and Frequency Setup at Power Up

The integrated high performance VCO requires an internal frequency calibration at power up. To perform such calibration the following procedure is recommended:

- Apply 5V power supply to IC.
- Apply an input reference frequency and ensure the signal is stable.
- Turn on the TRF3761 using the chip enable pin (CHIP_EN, pin 2).
- Setup the device through Register 1 referencing Table 1.
  a. The first 4 bits of the 32-bit code sent to the chip are set DB <3:0> to 0000; which is the address of register 1.
  b. Bit 5, DB4 sets the soft reset for the chip. If a soft reset is used then write to register 1 twice: once with DB4 set high and once with DB4 set low. Typically, this bit is only used when the chip has been powered up and registers 1, 2, and 3 have been already written to, so on power-up reset is not required, so DB4 is, by default, set low.
  c. DB <7: 5> sets the charge pump current based on the resistor value on pin 28 of the TRF3761 and the decimal value of Register 1, DB<7:5> used in this equation, Icp = (1.2V/Rbias)×((n+1)×22.168)/8, where n = decimal value of [Reg1 DB<7:5>]. This equation reduces to Icp = 3.3252×(n+1)/Rbias.
  d. DB <9: 8> sets the mode of the chip. The mode is how the device will or will not divide down the VCO's frequency. There are 3 choices for the mode setting, divide by 1, 2 or 4. For example if 525MHz is required from the TRF3761 then the divide-by-4 mode is chosen by setting DB <9: 8> to 10. With a 2100MHz VCO frequency set on Register 2 the output frequency will be divided by 4 to give 525MHz.
  e. DB <11:10> controls the output buffer. Both of these are set to 00 by default, so the buffer is controlled internally. See Table 2 for more information.
  f. DB <25:12> sets the R-divide value. Once the calculations under the *Synthesizing a Selected Frequency* have been completed the value is known, based on the external reference oscillator. The value for R is entered into the DB <25:12>. For example, if the reference oscillator is at 61.44MHz and a 120kHz step is required, which is also the Fpfd, then Refin /Fpfd = 512, which is entered as follows: MSB: LSB 0001000000000.
  g. By default, DB <27:26> are set to 00 for a 1.5ns delay on the ant backlash pulse width. See Table 1 for more information.
  h. DB 28 is set to 1 for positive by default. See Table 1 for more information.
  i. DB 29 is set to 0 for normal operation. See Table 1 for more information.
  j. DB 30 is set to 0 by default. See Table 1 for more information.
  k. DB 31 is set to 0 by default. See Table 1 for more information.
- Initiate calibration procedure by programming register 2 as follows: Reference Table 2
  a. Use bits DB<17, 4> of register 2 to specify the input reference frequency in MHz. The value is split into an integer and a fraction part. For example: to insert a f_{REF} of 30.72MHz, set:
  b. DB<10, 4> (integer part) equal to 0011110 (30) and
  c. DB<17, 11> (fraction part) equal to 1001000 (72).
  d. Set DB<30:18> of register 2 to the desired frequency. For example: 2200MHz would be 0100010011000 (2200).
  e. Set DB31of register 2 to 1 to start the calibration. The VCO calibration runs for 5ms. During the cal procedure it will not be possible to program register 2 and 3. At the end of the calibration, bit DB31 of register 2 resets to 0.
  f. Subsequent frequency programming requires DB31 to be set to 0.

APPLICATION INFORMATION (continued)

- Completion of the frequency set up, on initial calibration, cannot proceed until 5ms has elapsed, due to full calibration, then it will require that the A and B values, the prescalar ratio, be known. See *Synthesizing a Selected Frequency* section below for calculation. Reference Table 3.
  a. Register 3 DB<3:0> is the address of register 3, 0010 (2).
  b. DB<5:4> sets the prescalar ratio, 8/9, 16/17, 32/33, 64/65. For example: if 16/17 are required, set the register bits DB<5:4> to 01.
  c. DB<11:6> sets the A value for the N counter. For example: if A is 4, set DB<11:6> as follows: 000100 (4).
  d. DB<24:12> sets the B value for the N counter. For example: if B is 1156, set DB<24:12> as follows: 0010010000100 (4).
  e. DB<28:25> sets the TEST_MUX.

Table 4. Settings

STATE	DB<28:25>	STATE	DB<28:25>
3-state o/p	0000	R-divider o/p	0100
Digital lock Detect	0001	Analog lock detect	0101
N-Divider o/p	0010	Read back	0110
DVDD	0011	DGND	0111

  f. DB29 sets the START LOCK, which is set to 0, on the initial frequency setup and then set to 1 on additional frequency changes.

Once all registers are written to the TRF3761 will lock to the desired frequency.

Re-Calibration After Power Up

Assuming the TRF3761 is powered up and operational, a VCO calibration is also possible without powering down the IC. To perform such calibration the following procedure is recommended:

- Set bit DB4 (RESET) of register 1 to 1. This performs a software reset and clears all registers of VCO calibration data.
- Repeat form *Initial Calibration and Frequency setup at Power up* from above at section A.

Synthesizing a Selected Frequency

The TRF3761 is an integer-N PLL synthesizer, and because of its flexibility (14-bit R, 6-bit A, 13-bit B counter, and dual modulus prescaler), is ideal for synthesizing virtually any desired frequency. Let us assume that we need to synthesize a 900MHz local oscillator, with spacing capability (minimum frequency increment) of 200kHz, as in a typical GSM application. The choice of the external reference oscillator to be used is beyond the scope of this section, but assuming that a 10MHz reference is selected, the settings are calculated to yield the desired output frequency and channel spacing. There is more than one solution to a specific set of conditions, so below is one way of achieving the desired result. First, select the appropriate R counter value. Since a channel spacing of 200kHz is desired, the PFD is set to 200kHz. Calculate the R value through R = REFIN/PFD = 10MHz/ 200kHz = 50. Assume a prescaler value of 8/9 is selected. This is a valid choice, since the prescaler output is well within the 200MHz limit (900MHz / 8 = 112.5MHz). Select the appropriate A and B counter values. RFOUT = Fpfd $\times$ N = (fREFIN / R) $\times$ (A + P $\times$ B). Therefore, the following equation must be solved: 900MHz = 200kHz x (A + 8 $\times$ B). There are many solutions to this single equation with two unknowns; there are some basic constraints on the solution, since $3 \leq B \leq 8191$, and also $B \geq A$. So, if A = 4, solving the equation yields B = 562. One complete solution would be to choose: R = 50, A = 4, B = 562 and P = 8/9, resulting in the desired N = 4500.

When this procedure is complete the values for A, B, R, and the prescalar ratio should be known. Registers 2 and 3 need to be set up for operation of the chip. See Table 2 and Table 3 for this procedure. Register 2 bits <DB30:DB18> 12:0 set the output frequency of the device along with register 3.

Application Schematic

Figure 56 shows a typical application schematic for the TRF3761. In this example, the output signal is taken differential using the 2 resistive pull-up resistors of the final output buffer. A single-ended and tuned load configuration is also available.

The loop filter components, shown in the application schematic, are typical ones used for the plots shown above. Those values can be optimized differently according to the requirements of the different applications.

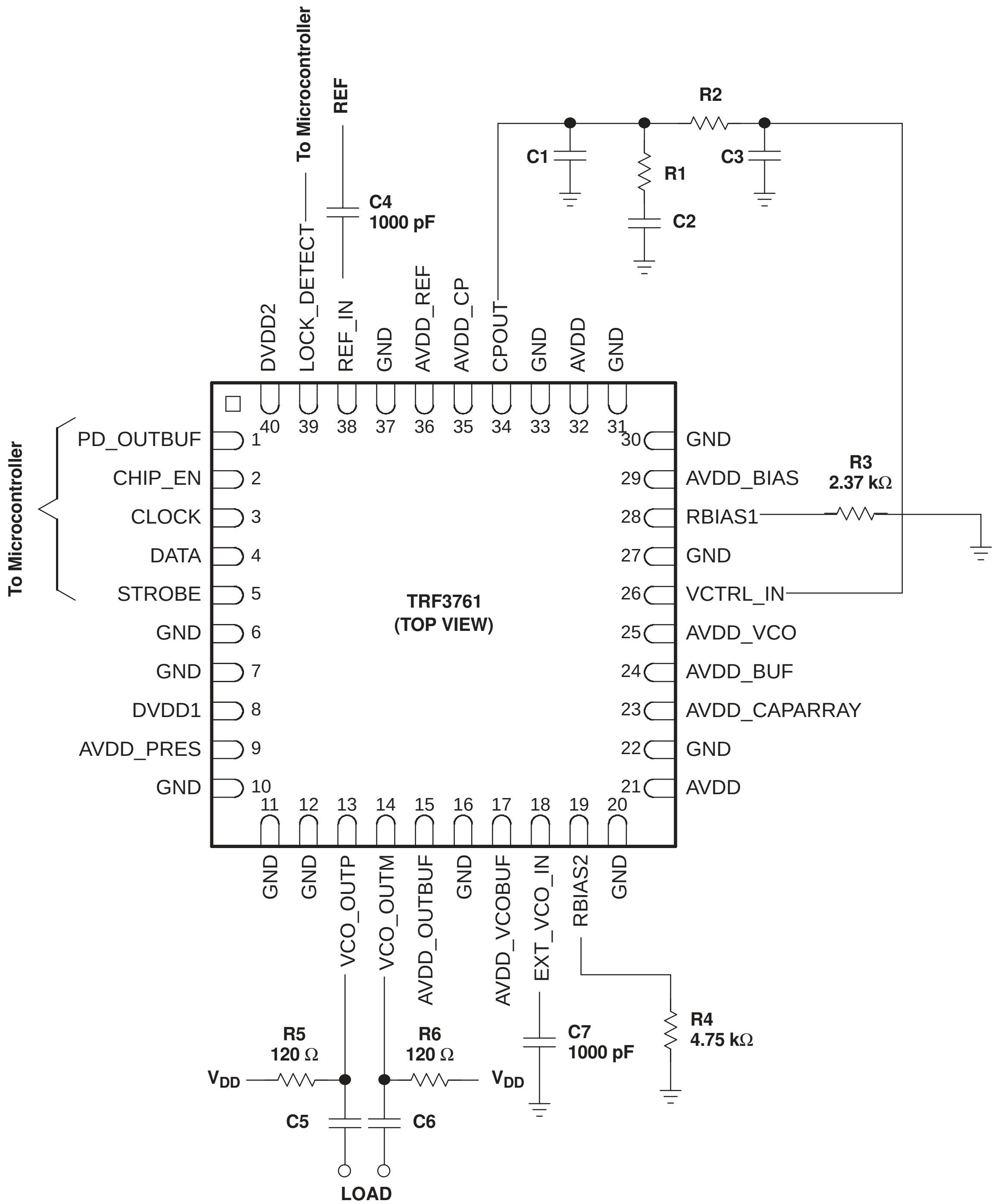

Figure 56. TRF3761 Application Schematic

PRODUCT PREVIEW

PRODUCT PREVIEW

Loop Filter Design

Numerous methodologies and design techniques exist for designing optimized loop filters for particular applications. The loop filter design can affect the stability of the loop, the lock time, the bandwidth, the extra attenuation on the reference spurs, etc. The role of the loop filter is to integrate and lowpass the pulses of the charge pump and eventually yield an output tuning voltage that drives the VCO. Several filter topologies can be implemented, including both passive and active. In this section, a third-order passive filter is used. For this example, assume these several design parameters. The internal VCO has a value of 23MHz/V, meaning that in the linear region, changing the tuning voltage of the VCO by 1V induces a change of the output frequency of about 23MHz. It is known that N = 4500 and Fpfd = 200kHz. It is assumed that current setting 1 will be used and be set to a maximum current of 5.6mA. In addition, the bandwidth of the loop filter must be determined. This is a critical consideration as it affects the lock time of the system. Assuming an approximate bandwidth of around 20kHz is required and that for stability a phase margin of about 45 degrees is desired, the following values for the components of the loop filter can be derived. There is almost an infinite number of solutions to the problem of designing the loop filter and the designer is called to make tradeoff decisions for each application.

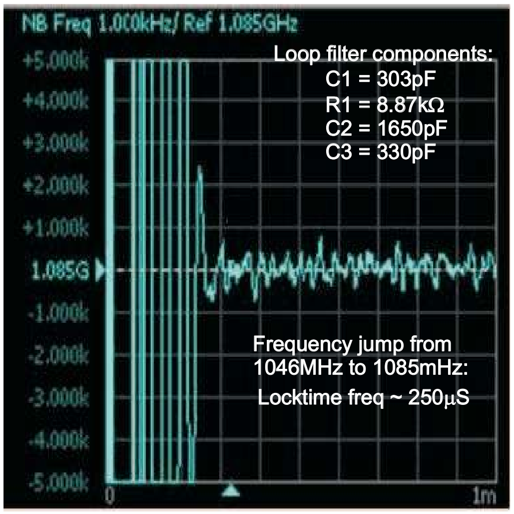

Figure 57. Frequency Locktime

Layout/PCB Considerations

This section of the design of the complete PLL is of paramount importance in achieving the desired performance. Wherever possible, a multi-layer PCB board should be used, with at least one dedicated ground plane. A dedicated power plane (split between the supplies if necessary) is also recommended. The impedance of all RF traces (the VCO output and feedback into the PLL) should be controlled to 50Ω. All small value decoupling capacitors should be placed as close to the device pins as possible. It is also recommended that both top and bottom layers of the circuit board be flooded with ground, with plenty of ground vias dispersed as appropriate. The most sensitive part of any PLL is the section between the charge pump output and the input to the VCO. This includes the loop filter components, and the corresponding traces. The charge pump is a precision element of the PLL and any extra leakage on its path can adversely affect performance. Extra care should be given to ensure that parasitics are minimized in the charge pump output, and that the trace runs are short and optimized. Similarly, it is also recommend that extra care is taken in ensuring that any flux residue is thoroughly cleaned and moisture baked out of the PCB. From an EMI perspective, and since the synthesizer is typically a small portion of a bigger, complex circuit board, shielding is recommended to minimize EMI effects.

Application Example for a High Performance RF Transmit Signal Chain

Much in the same way as described above, the TRF3761 is an ideal synthesizer to use in implementing a complete high performance RF transmitter chain such as the TSW3000 and up-and-coming TSW 3003 Demonstration kits. Using a complete suite of high performance Texas Instruments components, a state-of-the-art transmitter can be implemented featuring excellent performance. Texas Instruments offers ideal solutions for the digital-to-analog conversion portion of transmitter as well as the analog and RF components needed to complete the transmitter. The baseband digital data is converted to I and Q signals through the dual

DAC5687, which features a 16-bit interpolating dual digital-to-analog converter (DAC). The device incorporates a digital modulator, independent differential offset control, and I/Q amplitude control. The device is typically used in baseband mode or in low IF mode in conjunction with an analog quadrature modulator. The DAC5687, after filtering, feeds a TRF3703, which is a direct, upconversion IQ modulator. This device accepts a differential input voltage quadrature signal at baseband or low IF frequencies and outputs a modulated RF signal based on the LO drive frequency. The LO drive input of the IQ modulator is generated by the TRF3761. The TRF3761 is a family of high performance, highly integrated frequency synthesizers, optimized for wireless infrastructure applications. The TRF3761 includes an integrated VCO and integer-N PLL. Different members of the TRF3761 family can be chosen for application specific VCO frequency ranges. In addition, the CDC7005 clocking solution can be used to clock the DAC and other portions of the transmitter. A block diagram of the proposed architecture is shown in Figure 58 and Figure 59. For more details, contact Texas Instruments directly.

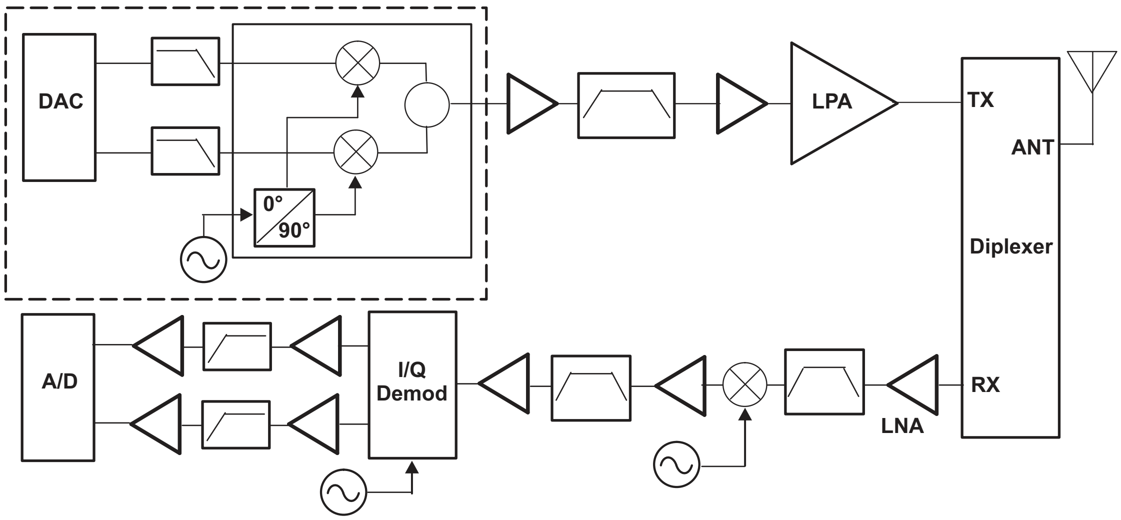

Figure 58. Transmit Chain Block Diagram

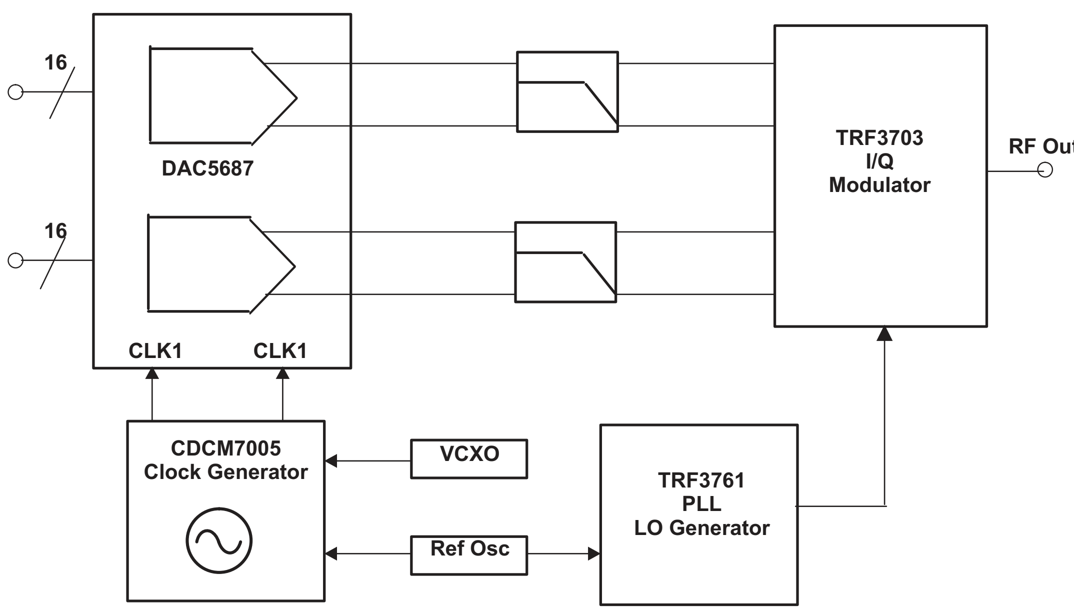

Figure 59. Transmit Chain Block Diagram

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TRF3761IRHAR	PREVIEW	QFN	RHA	40	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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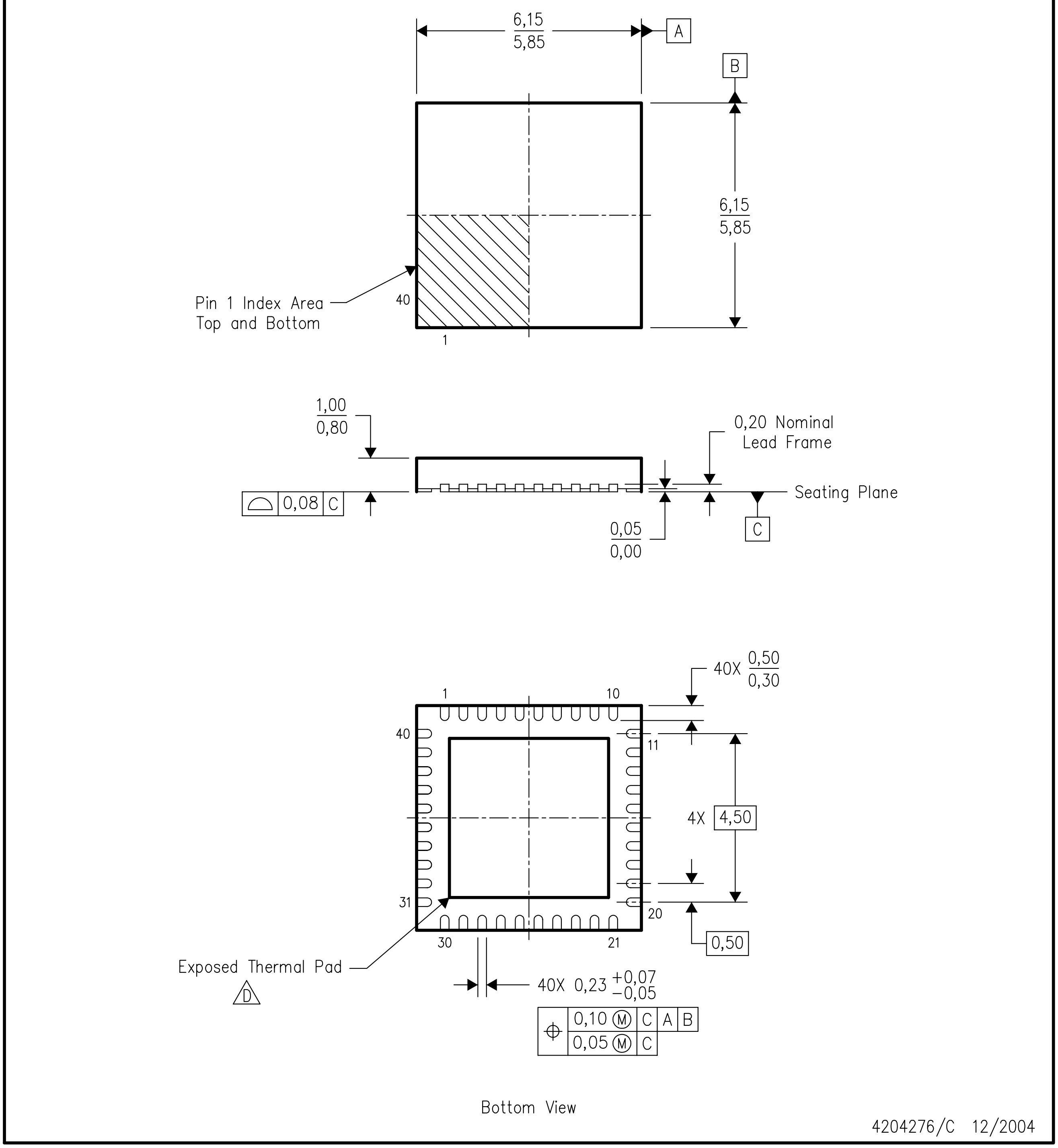
RHA (S-PQFP-N40) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO−220 variation VJJD−2.

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