

HA1631D01/02/03/04 Series

Dual CMOS Comparator (Push Pull/Open Drain Output)

REJ03D0804-0200 Rev.2.00 Nov 20, 2006

Description

The HA1631D01/02/03/04 are low power dual CMOS Comparator featuring low voltage operation with typical current supply of $10 \,\mu\text{A}/100 \,\mu\text{A}$. They are designed to operate from a single power supply and have push-pull full swing outputs that allow direct connections to logic devices. The Open Drain version HA1631D03/04 enable Output Level shifting through external pull up resistors. Available in MMPAK-8 and TSSOP-8 package.

Features

• Low supply current

HA1631D01/03 : $I_{DDtyp} = 5 \mu A$ (per comparators) HA1631D02/04 : $I_{DDtyp} = 50 \mu A$ (per comparators)

Low voltage operation : V_{DD} = 1.8 to 5.5 V
 Low input offset voltage : V_{IOmax} = 5 mV
 Low input bias current : I_{IBtyp} = 1 pA

• Maximum output voltage : $V_{OHmin} = 2.9 \text{ V}$ (at $V_{DD} = 3.0 \text{ V}$)

Input common voltage range includes ground

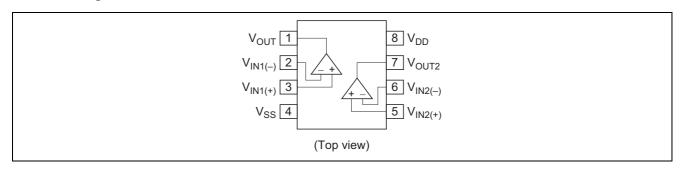
• On-chip ESD protection

Available in MMPAK-8, TSSOP-8 package using Pb free lead frame

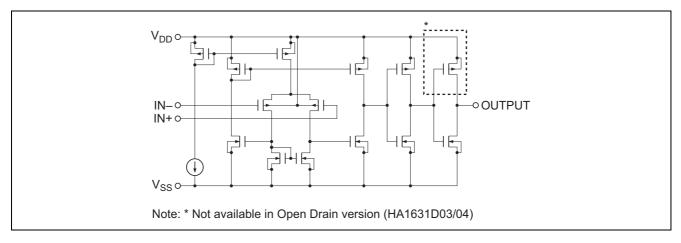
Ordering Information

Type No.	Package Name	Package Code		
HA1631D01T				
HA1631D02T	TTP-8DAV	PTSP0008JC-B		
HA1631D03T	TIF-ODAV	PTSPUUU6JC-B		
HA1631D04T				
HA1631D01MM				
HA1631D02MM	MMPAK-8	PLSP0008JC-A		
HA1631D03MM	IVIIVIPAN-0			
HA1631D04MM				

Pin Arrangement



Equivalent Circuit (1/2)



Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	7.0	V	
Differential input voltage	V _{IN(diff)}	$-V_{DD}$ to $+V_{DD}$	V	Note 1
Input voltage	V _{IN}	-0.1 to +V _{DD}	V	
Output current	l _{оит}	28	mA	Note 2
Power dissipation	P _T	192	mW	TSSOP-8
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +125	°C	

Notes: 1. Do not apply input voltage exceeding V_{DD} or 7 V.

Electrical Characteristics

 $(Ta = 25^{\circ}C, V_{DD} = 3.0 \text{ V}, V_{SS} = 0 \text{ V})$

						C, V _{DD} = 3.0 V, V _{SS} = 0 V)	
Item		Symbol	Min	Тур	Max	Unit	Test Conditions
Input offset voltage		V _{IO}	_	_	5	mV	$V_{IN} = V_{DD}/2$, $R_L = 1 M\Omega$
Input bias current	Input bias current		_	(1)	_	pА	$V_{IN} = V_{DD}/2$
Input offset current		I _{IO}	_	(1)	_	pА	$V_{IN} = V_{DD}/2$
Common mode inp	ut voltage range	V _{CM}	-0.1		2.1	V	
Supply current	HA1631D01/03	I _{DD}	_	10	20	μΑ	$V_{DD} = 3 V, V_{IN} + = 1 V,$
	HA1631D02/04		_	100	200	μА	$V_{IN}-=0$ V
Response time	HA1631D01	TP _{LH}	_	(1.20)	_	μS	1 V DC bias,
	HA1631D01/03	TP _{HL}	_	(0.55)	_	μS	100 mV overdrive,
	HA1631D01	t _r	_	(24)	_	ns	$C_L = 15 pF$
	HA1631D01/03	t _f	_	(7)	_	ns	
	HA1631D02	TP _{LH}	_	(0.33)	_	μS	
	HA1631D02/04	TP _{HL}	_	(0.17)	_	μS	
	HA1631D02	t _r	_	(12)	_	ns	
	HA1631D02/04	t _f	_	(7)	_	ns	
Output source current		I _{OSOURCE}	6	13	_	mA	Vout = 2.5 V
(Only for HA1631D	01/02)						
Output sink current		I _{OSINK}	7	14	_	mA	Vout = 0.5 V
Common mode	HA1631D01/03	CMRR	60	80	_	dB	$V_{IN}1 = 0 V, V_{IN}2 = 2 V$
rejection ratio	HA1631D02/04		50	70	_	dB	
Power supply rejection ratio		PSRR	60	80	_	dB	$V_{DD}1 = 1.8 \text{ V}, V_{DD}2 = 5 \text{ V}$
Output voltage high		V _{OH}	V _{DD} -0.1	_	_	V	$R_L = 10 \text{ k}\Omega \text{ to V}_{SS}$
(Only for HA1631D01/02)							
Output voltage low		V _{OL}	_		0.1	V	$R_L = 10 \text{ k}\Omega \text{ to } V_{DD}$
Output leakage current		I _{LO}	_	_	0.1	μΑ	$V_{IN}+=1 \ V, \ V_{IN}-=0 \ V,$
(Only for HA1631D03/04)							$V_O = 3 V$
Operating voltage range		Vopr	1.8	_	5.5	V	

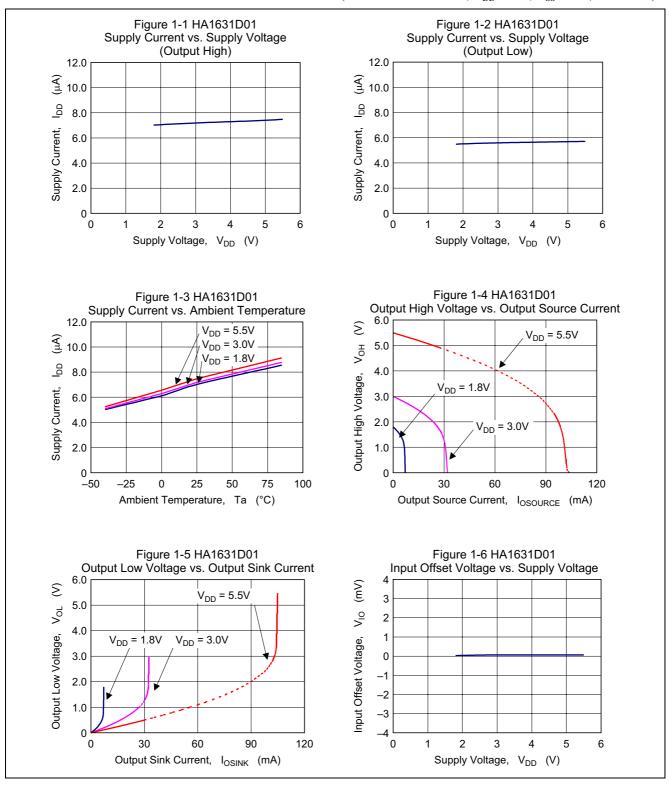
Note: (): Design specification

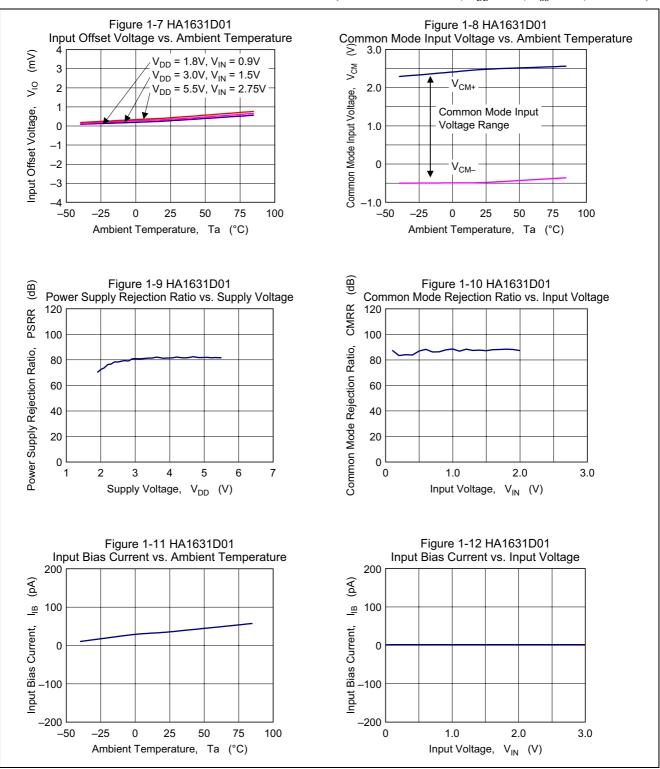
^{2.} The maximum output current is the maximum allowable value for continuous operation.

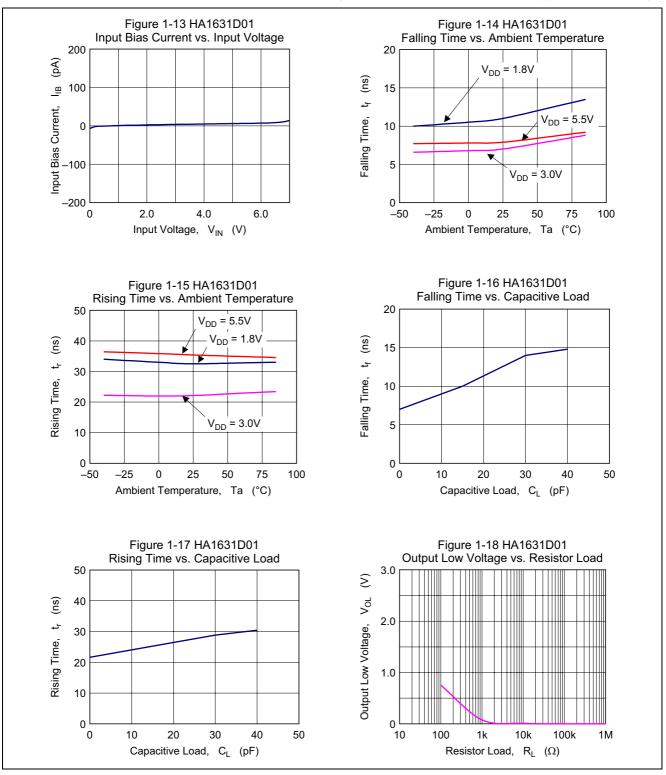
Table of Graphs

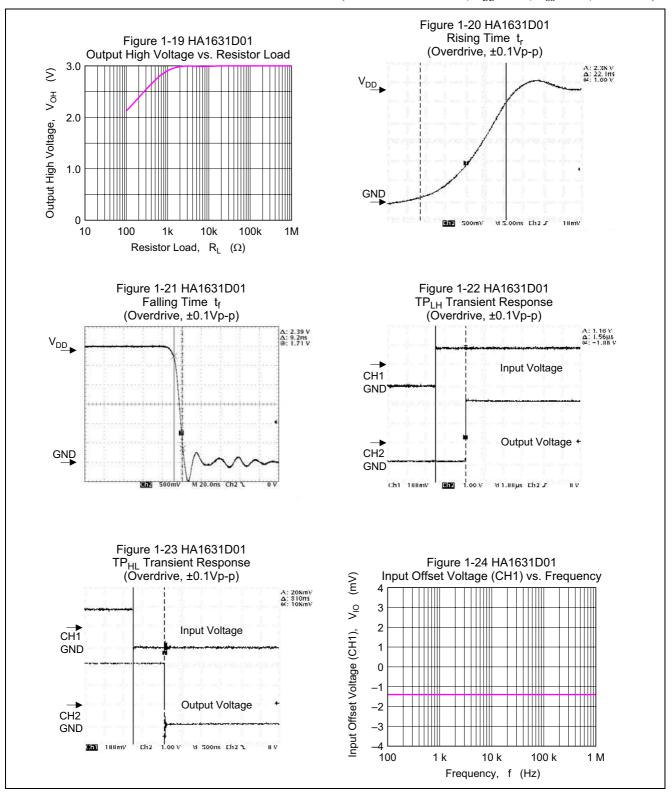
			HA1631D01	HA1631D02	HA1631D03	HA1631D04	Test
Electrical Characteristics		Figure	Figure	Figure	Figure	Circuit No.	
Supply current	I _{DD}	vs. Supply voltage(Out H)	1-1	2-1	3-1	4-1	1
		vs. Supply voltage(Out L)	1-2	2-2	3-2	4-2	2
		vs. Temperature(Out H)	1-3	2-3	3-3	4-3	1
		vs. Frequency(Out H)	1-26	2-26	3-20	4-20	15
Output high voltage	V _{OH}	vs. Rload	1-19	2-19	_	_	4
Output source current	I _{OSOURCE}	vs. Output high voltage	1-4	2-4	_	_	3
Output low voltage	V _{OL}	vs. Rload	1-18	2-18	3-15	4-15	6
Output sink current	I _{OSINK}	vs. Output low voltage	1-5	2-5	3-4	4-4	5
Input offset voltage	V _{IO}	vs. Supply voltage	1-6	2-6	3-5	4-5	8
		vs. Temperature	1-7	2-7	3-6	4-6	7
Common mode input voltage range	V _{CM}	vs. Temperature	1-8	2-8	3-7	4-7	9
Power supply rejection ratio	PSRR	vs. Supply voltage	1-9	2-9	3-8	4-8	11
Common mode rejection ratio	CMRR	vs. Input voltage	1-10	2-10	3-9	4-9	12
Input bias current	I _{IB}	vs. Temperature	1-11	2-11	3-10	4-10	10
		vs. Input voltage(V _{DD} = 3 V)	1-12	2-12	3-11	4-11	10
		vs. Input voltage(V _{DD} = 7 V)	1-13	2-13	3-12	4-12	10
Falling time	t _f	vs. Temperature	1-14	2-14	3-13	4-13	13
		vs. Cload	1-16	2-16	3-14	4-14	13
		Time waveform	1-21	2-21	3-16	4-16	13
Rising time	t _r	vs. Temperature	1-15	2-15	_	_	13
		vs. Cload	1-17	2-17	_	_	13
		Time waveform	1-20	2-20	_	_	13
Propagation delay time	TP _{LH}	Time waveform	1-22	2-22	_	_	13
	TP _{HL}	Time waveform	1-23	2-23	3-17	4-17	13
Cross talk	V _{OUT} (CH1)	vs. Input voltage	1-24	2-24	3-18	4-18	14
	V _{OUT} (CH2)	vs. Input voltage	1-25	2-25	3-19	4-19	14

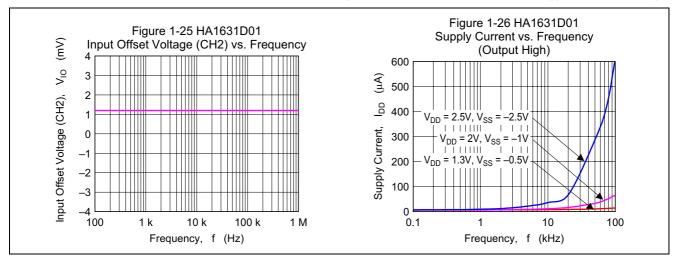
Main Characteristics

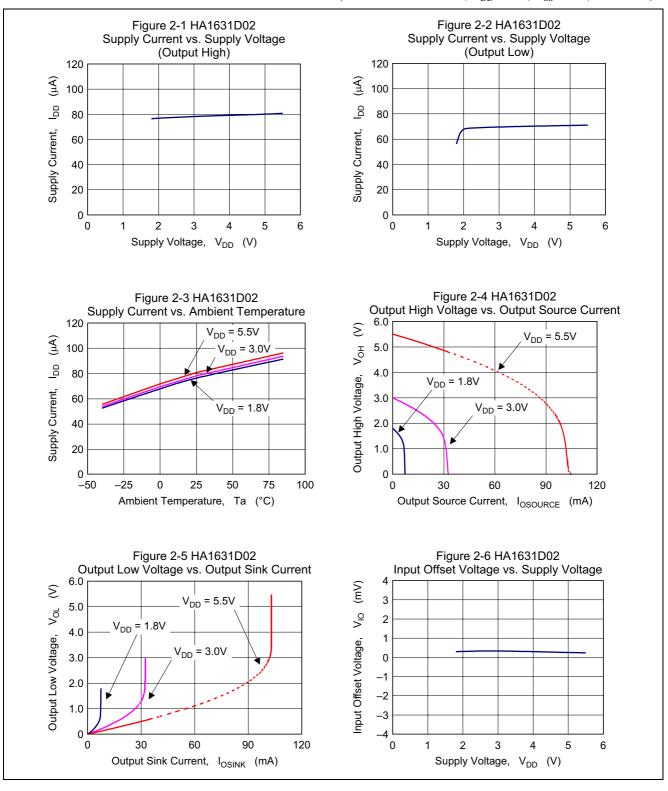


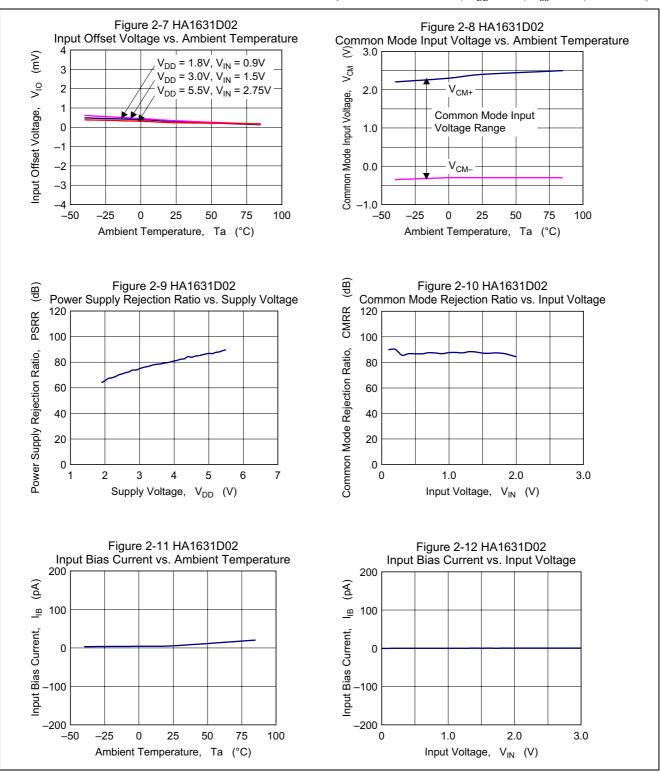


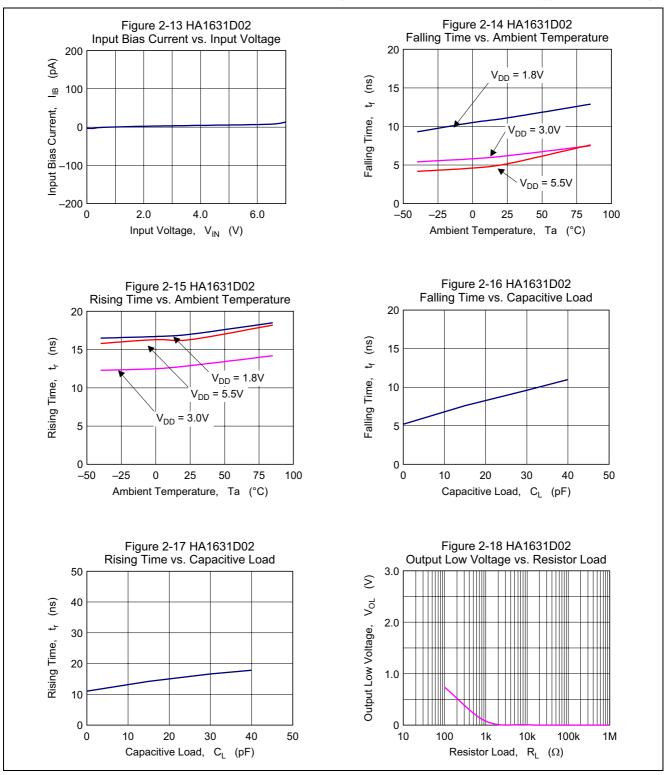


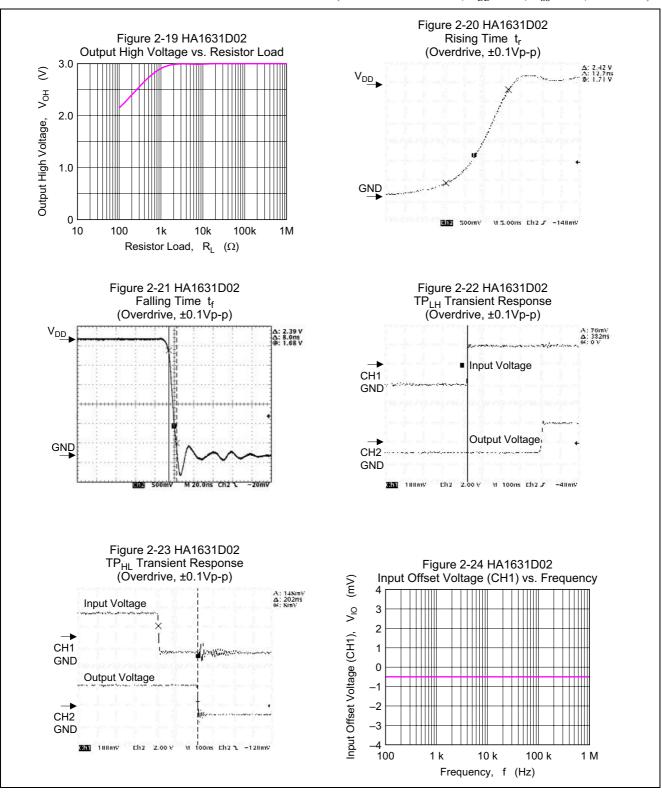


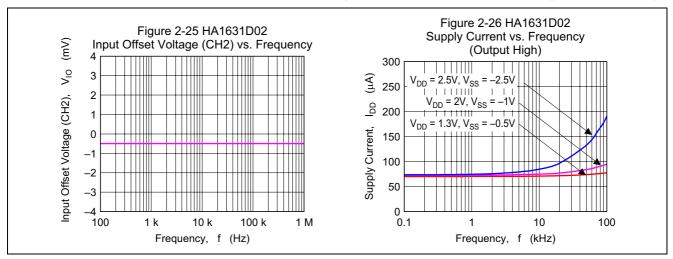


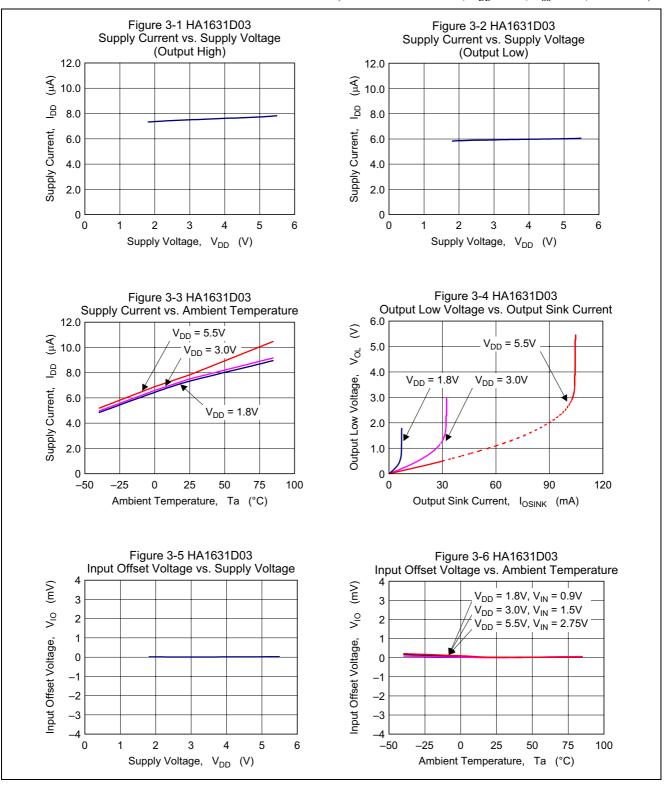


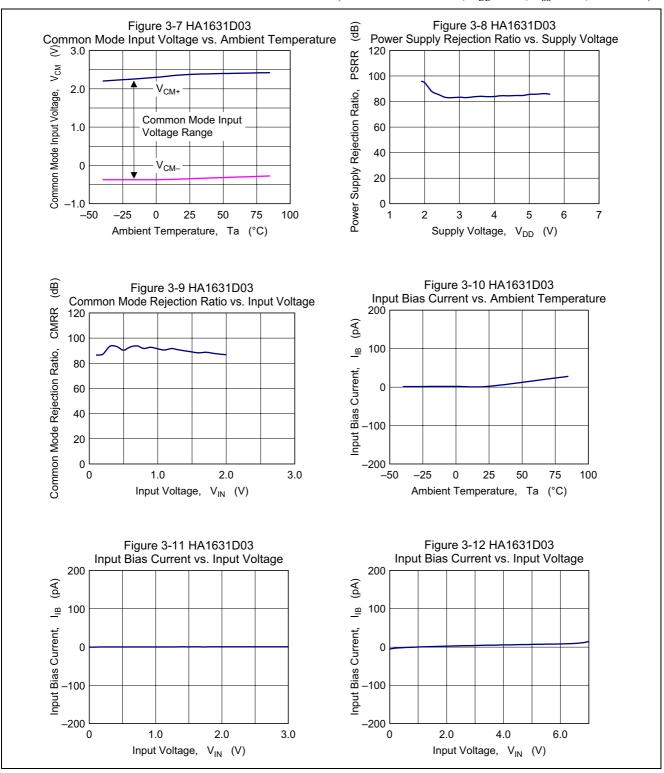


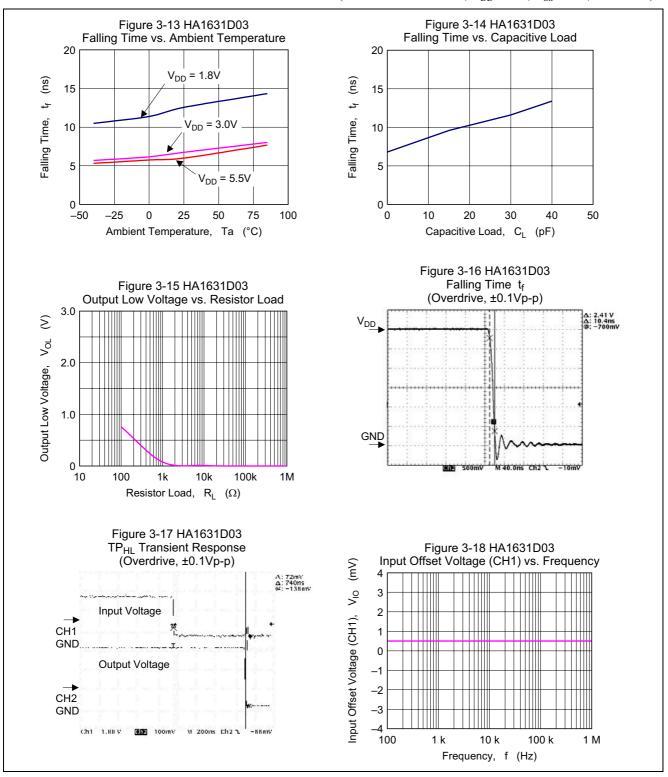


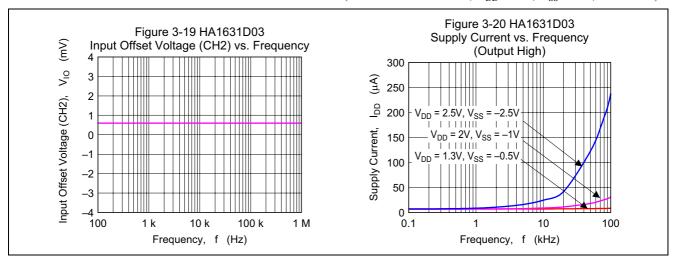


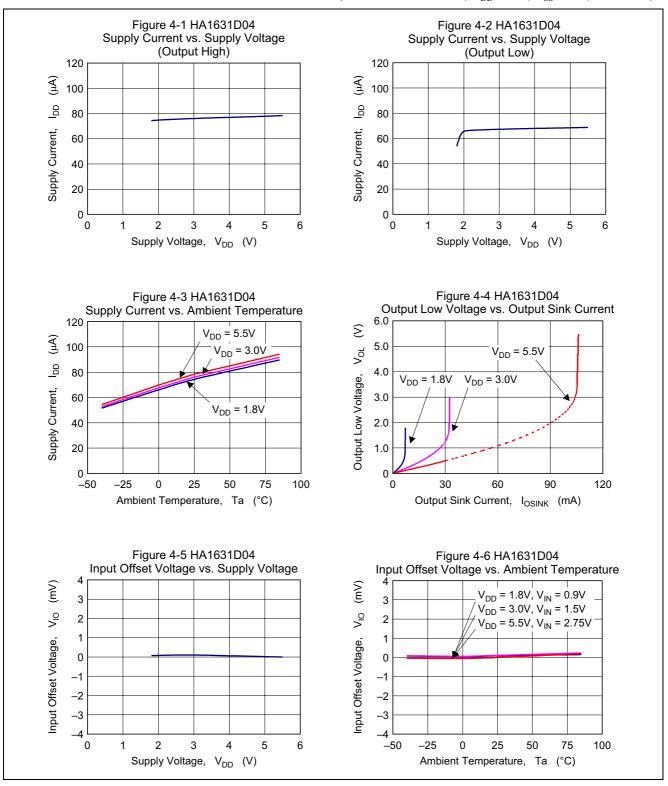


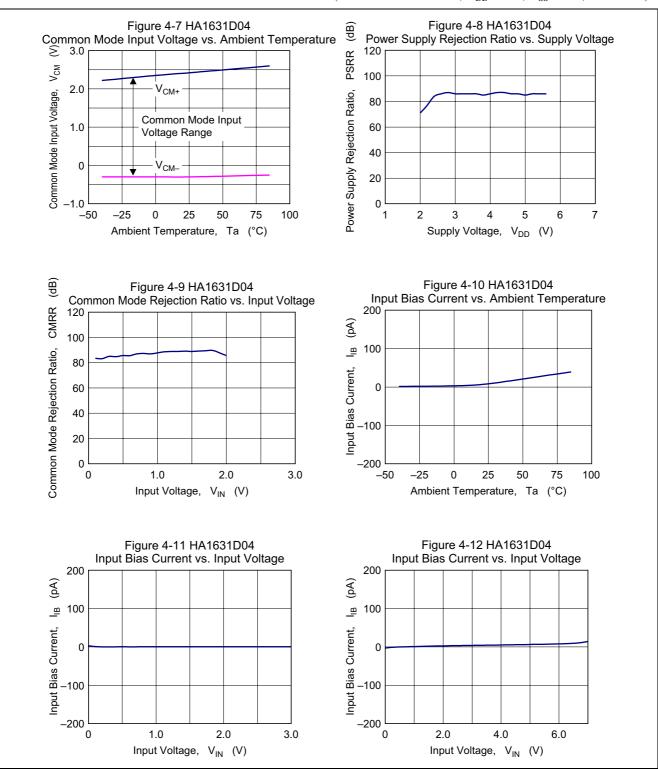


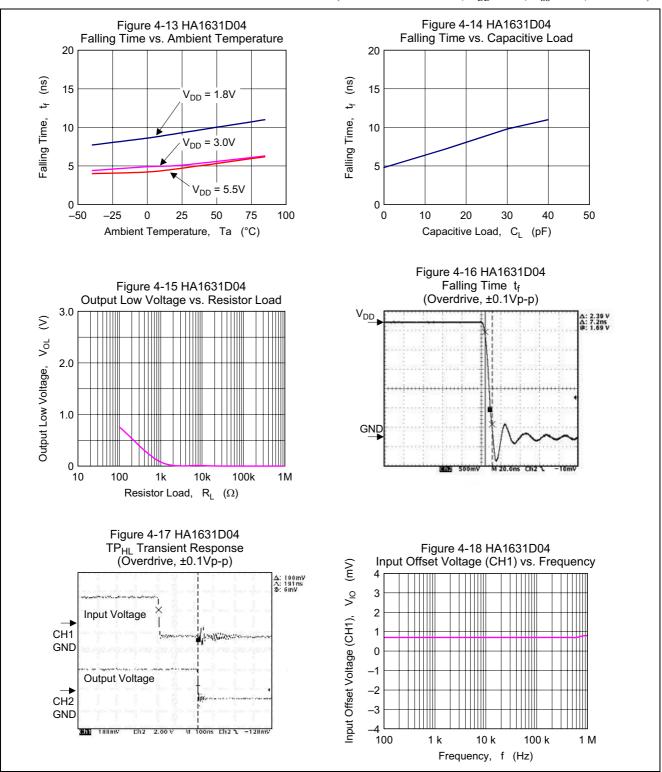


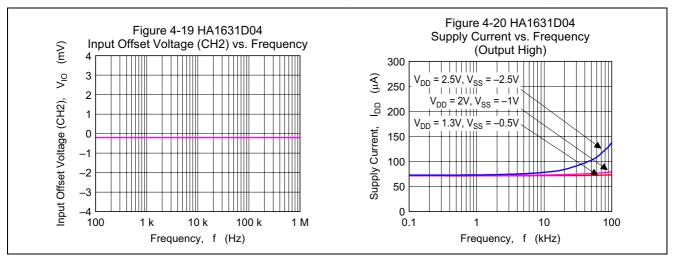








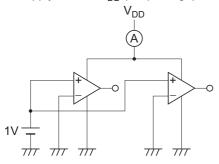




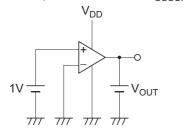
Test Circuits

(unless otherwise noted, $V_{DD} = 3 \text{ V}$, $V_{SS} = 0 \text{ V}$, $Ta = 25^{\circ}\text{C}$)

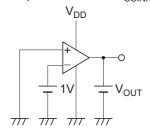
1. Supply Current, I_{DD} (Output High)



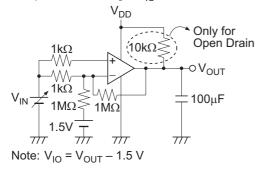
3. Output Source Current, $I_{OSOURCE}$



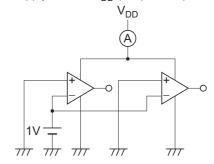
5. Output Sink Current, I_{OSINK}



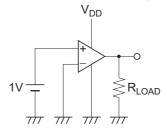
7. Input Offset Voltage, V_{IO}



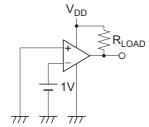
2. Supply Current, I_{DD} (Output Low)



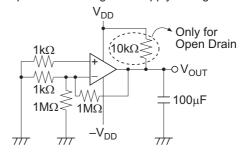
4. Output Voltage High, V_{OH}



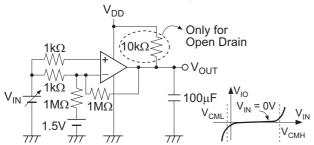
6. Output Voltage Low, V_{OL}



8. Input Offset Voltage vs. Supply Voltage

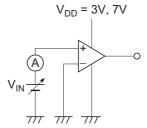


9. Common Mode Input Voltage, V_{CM}

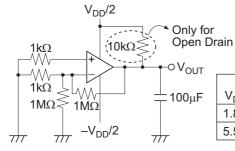


Note: V_{CML} and V_{CMH} are values of V_{IN} when V_{IO} changes more than 50dB taking V_{IN} = 0V as reference.

10. Input Bias Current, $I_{\rm IB}$

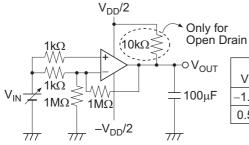


11. Power Supply Rejection Ratio, PSRR

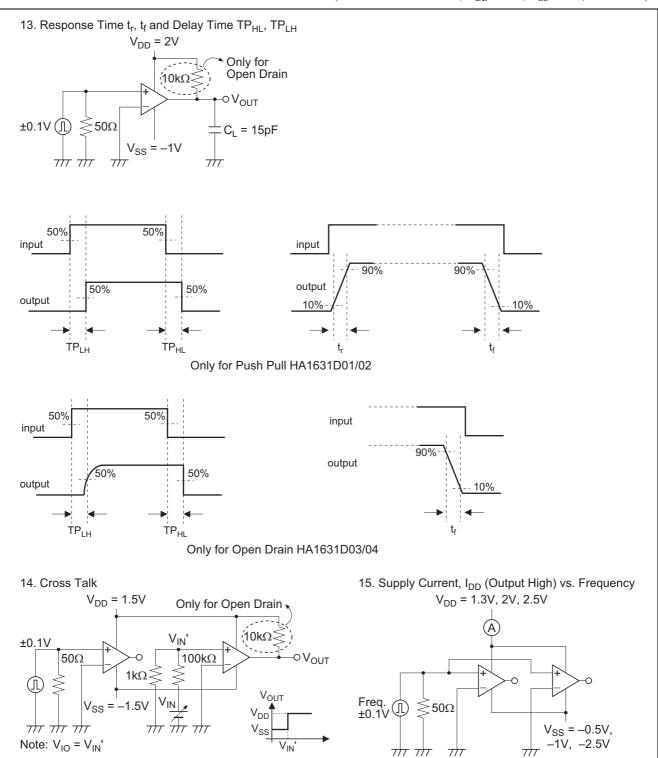


V _{DD}	Measure Point		PSRR Calculation
1.8V	V _{OUT1}	$V_{IO1} = V_{OUT1}/1000$	$PSRR = 20log \frac{ (V_{IO2} - V_{IO1}) }{ (V_{IO2} - V_{IO1}) }$
5.5V	V _{OUT2}	$V_{IO2} = V_{OUT2}/1000$	$\frac{ 75009 }{5.5V - 1.8V}$

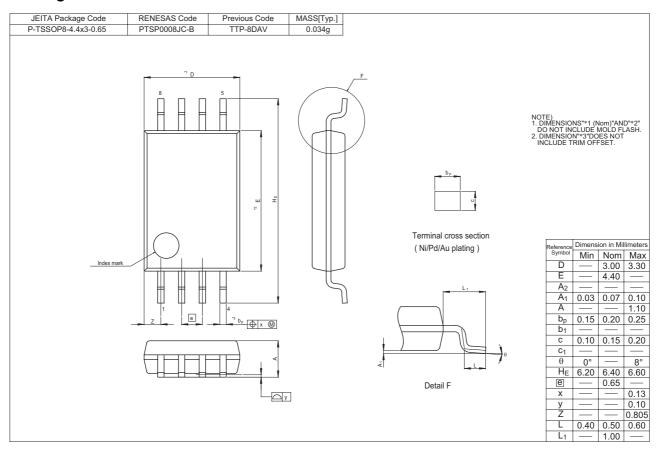
12. Common Mode Rejection Ratio, CMRR

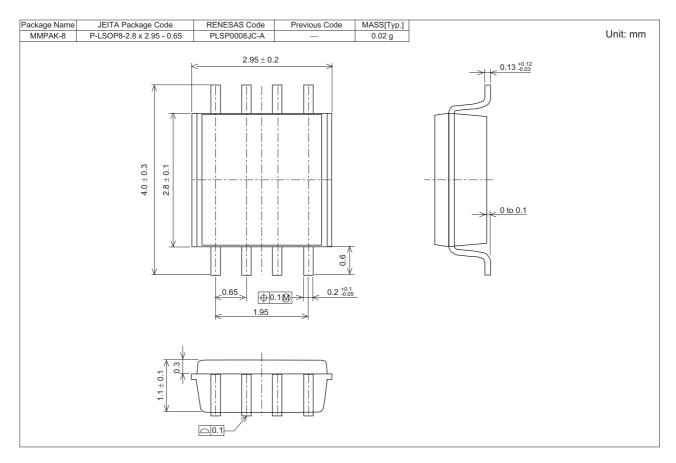


1	Measure Point	Calculate V _{IO}	CMRR Calculation
-1.5V	V _{OUT1}	$V_{IO1} = V_{OUT1}/1000$	CMRR = $\left 20 \log \frac{ (V_{IO2} - V_{IO1}) }{0.5V - (-1.5V)} \right $
0.5V	V _{OUT2}	$V_{IO2} = V_{OUT2}/1000$	$\frac{ \text{CWRR} - \text{2010g}}{ \text{0.5V} - (-1.5V) }$



Package Dimensions





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Old Company Name in Catalogs and Other Documents

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April 1st, 2010 Renesas Electronics Corporation

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