August 1986 Revised March 2000 DM74LS283 4-Bit Binary Adder with Fast Carry

DM74LS283 4-Bit Binary Adder with Fast Carry

General Description

FAIRCHILD

SEMICONDUCTOR

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

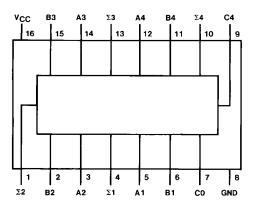
- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
 Two 8-bit words 25 ns
 Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS283M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS283N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



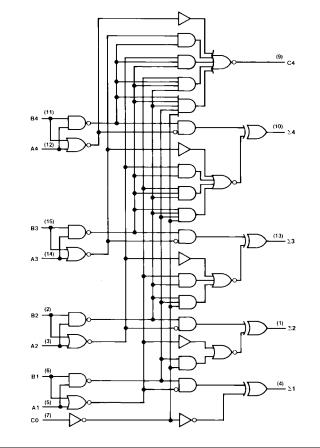


Input				Outputs						
				When C0 = L			When C0 = H			
					W	nen C2 = L	L When C2			
A1 /	B1	A2	B2	Σ1	Σ2 C2		Σ1	Σ2	C2 /	
A3	B 3	A4	В4	Σ3	Σ4	C4	Σ3	Σ4	C4	
L	L	L	L	L	L	L	Н	L	L	
н	L	L	L L	н	L L	L	L	н	L L	
L	н	L	L	н	L	L	L	н	L	
н	н	L	L	i L	н	L	н	н	L	
L	L	н	L	L	н	L	н	н	L	
н	L	н	L	н	н	L	L	L	н	
L	н	н	L	н	н	L	L	L	н	
н	н	н	L	L	L L	н	н	L	н	
L	L	L	н	L L	н	L	н	н	L	
н	L	L	н	н	н	L	L	L	н	
L	н	L	н	н	н	L	L	L	н	
н	н	L L	н	L	L	н	н	L	н	
L	L	н	н	L	L	н	Н	L	н	
н	L	н	н	н	L	н	L	н	н	
L	н	н	н	н	j L	н	L	н	н	
н	н	н	н	L	н	н	н	н	н	

H = HIGH Level, L = LOW Level

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ 1 and Σ 2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ 3, Σ 4, and C4.

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS283

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
/ _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
ОН	HIGH Level Output Current			-0.4	mA
OL	LOW Level Output Current			8	mA
Τ _Α	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level	V _{CC} = Min, I _{OH} = Max		2.7	3.4		V
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$		2.7	3.4		v
V _{OL}	LOW Level	$V_{CC} = Min, I_{OL} = Max$			0.35	0.5	
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$		0.35	0.5	V	
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$			0.25	0.4	
l _l	Input Current @ Max	V _{CC} = Max	Α, Β			0.2	mA
	Input Voltage	$V_1 = 7V$	C0			0.1	
IIH	HIGH Level	V _{CC} = Max	Α, Β			40	μΑ
	Input Current	$V_1 = 2.7V$	C0			20	
IIL	LOW Level	V _{CC} = Max	А, В			-0.8	mA
	Input Current	$V_I = 0.4V$	C0			-0.4	
l _{os}	Short Circuit Output Current	V _{CC} = Max		-20		-100	mA
CC1	Supply Current	V _{CC} = Max (Note 4)	•		19	34	mA
I _{CC2}	Supply Current	V _{CC} = Max (Note 5)			22	39	mA

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

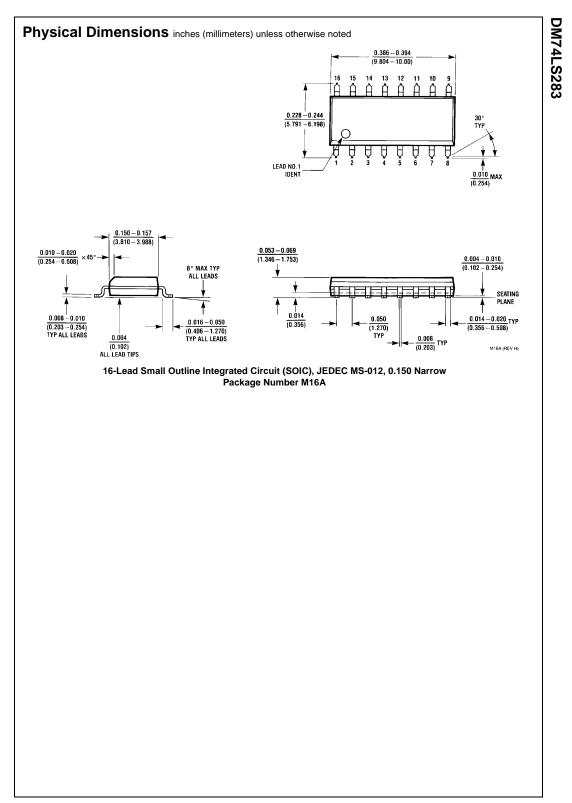
Note 4: I_{CC1} is measured with all outputs OPEN, all B inputs LOW and all other inputs at 4.5V, or all inputs at 4.5V.

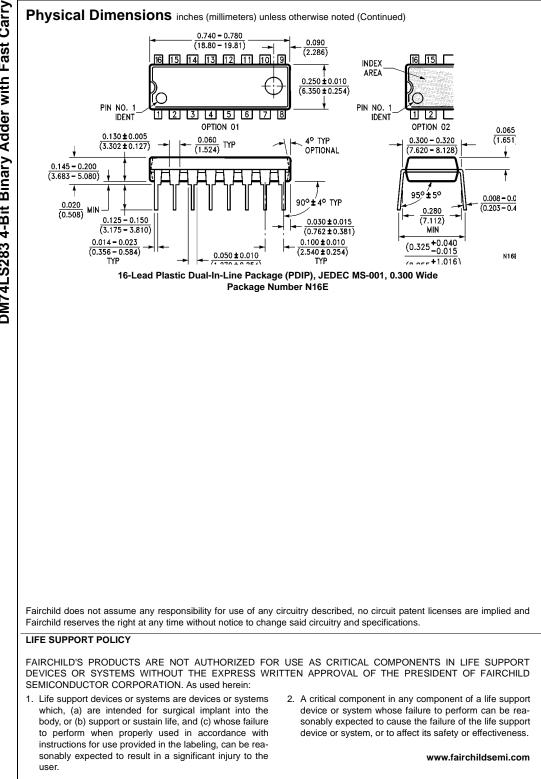
Note 5: I_{CC2} is measured with all outputs OPEN and all inputs GROUNDED.

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Switching Characteristics

at $V_{CC}=5V$ and $T_A=25^\circ C$ From (Input) $\mathbf{R}_{\mathbf{L}} = \mathbf{2} \mathbf{k} \Omega$ $\boldsymbol{C_L}=\boldsymbol{50}~\boldsymbol{pF}$ Units Symbol Parameter $C_L = 15 \text{ pF}$ To (Output) Min Max Min Max Propagation Delay Time t_{PLH} C0 to $\Sigma 1$, $\Sigma 2$ 24 28 ns LOW-to-HIGH Level Output t_{PHL} Propagation Delay Time C0 to $\Sigma 1$, $\Sigma 2$ 24 30 ns HIGH-to-LOW Level Output Propagation Delay Time t_{PLH} 28 C0 to ∑3 24 ns LOW-to-HIGH Level Output Propagation Delay Time t_{PHL} C0 to ∑3 24 30 ns HIGH-to-LOW Level Output t_{PLH} Propagation Delay Time C0 to $\Sigma 4$ 24 28 ns LOW-to-HIGH Level Output Propagation Delay Time t_{PHL} C0 to $\Sigma 4$ 24 30 ns HIGH-to-LOW Level Output t_{PLH} Propagation Delay Time A_i or B_i to Σ_i 24 28 ns LOW-to-HIGH Level Output Propagation Delay Time t_{PHL} $A_i \text{ or } B_i \text{ to } \Sigma_i$ 24 30 ns HIGH-to-LOW Level Output Propagation Delay Time t_{PLH} C0 to C4 17 24 ns LOW-to-HIGH Level Output t_{PHL} Propagation Delay Time C0 to C4 17 25 ns HIGH-to-LOW Level Output Propagation Delay Time t_{PLH} A_i or B_i to C4 17 24 ns LOW-to-HIGH Level Output Propagation Delay Time t_{PHL} 17 26 A_i or B_i to C4 ns HIGH-to-LOW Level Output





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