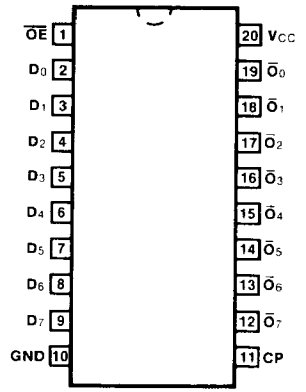
54LS/74LS564

OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A

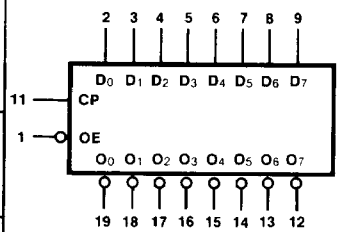


DESCRIPTION — The '564 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'LS574, but has inverted outputs. For complete discussions of operations, truth tables, ac and dc electrical specifications, refer to the 'LS374 data sheet.

- **INPUTS AND OUTPUTS ON OPPOSITE SIDES OF PACKAGE ALLOWING EASY INTERFACE WITH MICROPROCESSORS**
- **USEFUL AS INPUT OR OUTPUT PORT FOR MICROPROCESSORS**
- **FUNCTIONALLY IDENTICAL TO 'LS574**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS564PC		9Z
Ceramic DIP (D)	A	74LS564DC	54LS564DM	4E
Flatpak (F)	A	74LS564FC	54LS564FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.25
$\overline{O}_0 - \overline{O}_7$	3-State Outputs	65/15 (25)/(7.5)