MAX9890 Audio Click-Pop Suppressor

General Description

The MAX9890 provides click-and-pop suppression for devices such as CODECs with test integrated headphone amplifiers that lack a clickless/popless startup/power-up or shutdown/power-down. The device controls the ramping of the DC bias voltage on the output-coupling capacitors and the application of the audio signal to ensure that no audible transients are present at the headphones. The MAX9890A features a 200ms startup time for use with up to 100µF coupling capacitors. The MAX9890B features a 330ms startup time for use with greater than 100µF coupling capacitors.

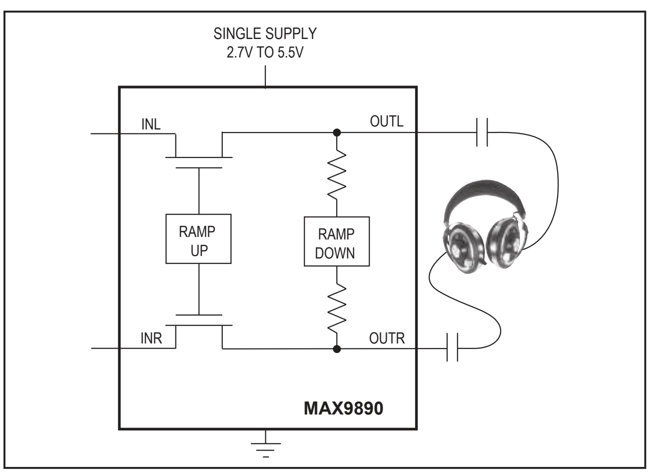
The MAX9890 consumes 14µA of supply current and 0.001µA in shutdown, while contributing less than 0.003% THD+N into a 32Ω load. ESD (Human Body Model) protection circuitry on the outputs protect the MAX9890 and devices further up the signal chain from ESD strikes up to ±8kV.

The MAX9890 is available in a miniature (1.5mm x 1.5mm x 0.6mm) 9-bump chip-scale package (UCSP™), as well as an 8-pin TDFN package (3mm x 3mm x 0.8mm), and is specified for operation over the -40°C to +85°C extended temperature range.

Applications

- High-End Notebook Audio
- Portable DVD Players
- Portable MP3 Players
- PDAs
- Cell Phones

Simplified Block Diagram



UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- 36dB Click-Pop Suppression
- 2.7V to 5.5V Single-Supply Operation
- Clickless/Popless Startup/Power-Up and Shutdown/Power-Down
- 0.001µA Low-Power Shutdown Mode
- THD+N < 0.003% Into 32Ω
- ±8kV ESD Protected Outputs (Human Body Model)
- Requires Only One 0.1µF Capacitor to Complete the Circuit
- Low 14µA Supply Current
- Tiny Packaging
  - 9-Bump UCSP (1.5mm x 1.5mm x 0.6mm)
  - 8-Pin TDFN (3mm x 3mm x 0.8mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9890AEBL+T	-40°C to +85°C	9 UCSP-9	ADV
MAX9890AETA	-40°C to +85°C	8 TDFN-EP**	AHA
MAX9890BEBL+T	-40°C to +85°C	9 UCSP-9	ADW
MAX9890BETA	-40°C to +85°C	8 TDFN-EP**	AHB
MAX9890BETA/V+	-40°C to +85°C	8 TDFN-EP**	BRQ

***EP = Exposed pad.*
+ Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
/V denotes an automotive qualified part that conforms to AEC-Q100.

Selector Guide

PART	PIN-PACKAGE	SWITCH TURN-ON TIME (ms)
MAX9890AEBL+T	9 UCSP-9	200
MAX9890AETA	8 TDFN-EP	200
MAX9890BEBL+T	9 UCSP-9	330
MAX9890BETA	8 TDFN-EP	330
MAX9890BETA/V+	8 TDFN-EP	330

Typical Application Circuit and Pin Configurations appear at end of data sheet.

Absolute Maximum Ratings

(All Voltages are Referenced to GND)
V_{CC} .... +6V
CEXT, $\overline{SHDN}$, OUT_ .... -0.3V to +6V
IN_ .... -0.3V to (V_{CC} + 0.3V)
Continuous Current (IN_, OUT_) .... ±150mA
Continuous Current (All Other Pins) .... ±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
9-Bump UCSP (derate 4.7mW/°C above +70°C)........379mW
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C
Bump Temperature (soldering)
Reflow .... +235°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 3V, $\overline{SHDN}$ = V_{CC}, GND = 0, C_{CEXT} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from R_{ON} test		2.7		5.5	V
Supply Current	I_{CC}	(Note 2)			14	22	µA
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND			0.001	1	µA
Input Voltage Range		Inferred from R_{ON} test		0		V_{CC}	V
On-Resistance	R_{ON}	Over input voltage range	V_{CC} = 5.5V		0.4	1	Ω
			V_{CC} = 2.7V		0.7	1.5	
On-Resistance Flatness	$R_{FLAT(ON)}$	Over input voltage range			2		mΩ
Output Discharge Resistance	$R_{OUT(DIS)}$				220		kΩ
Input Off-Leakage Current		$\overline{SHDN}$ = GND			0.001	1	µA
V_{CC} Power-Down Threshold (Note 3)	V_{UVLO}	V_{CC} falling			2.5		V
Click-Pop Reduction					36		dB
ESD Protection		OUT_, Human Body Model			±8		kV
DYNAMIC							
Turn-On Time (Note 4)	t_{ON}	MAX9890A			200		ms
		MAX9890B			330		
Turn-Off Time	t_{OFF}	(Note 5)			120		ns
Bandwidth					>100		kHz
Total Harmonic Distortion Plus Noise	THD+N	R_L = 32Ω, 30mW, f = 1kHz			0.003		%
Off-Isolation, IN_ to OUT_		f = 20kHz, $\overline{SHDN}$ = GND, R_L = 32Ω			-108		dB
Crosstalk (Switches ON)		f = 20kHz			-100		dB
Power-Supply Rejection Ratio (Note 6)	PSRR	V_{RIPPLE} = 0.5V_{P-P} at 20Hz, f_{IN} = 3kHz at 1V_{P-P}, R_L = 32Ω			-100		dB
		V_{RIPPLE} = 0.5V_{P-P} at 1kHz, f_{IN} = 3kHz at 1V_{P-P}, R_L = 32Ω			-100		
		V_{RIPPLE} = 0.5V_{P-P} at 20kHz, f_{IN} = 3kHz at 1V_{P-P}, R_L = 32Ω			-84		

Electrical Characteristics (continued)

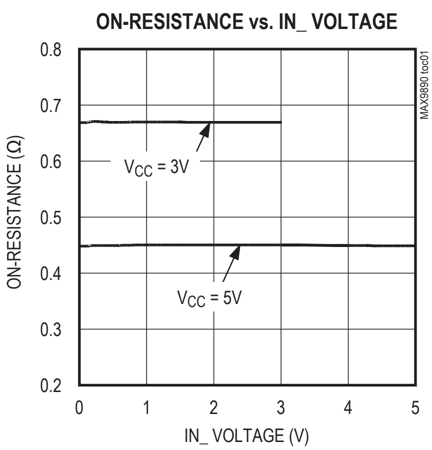
(V_{CC} = 3V, $\overline{SHDN}$ = V_{CC}, GND = 0, C_{CEXT} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

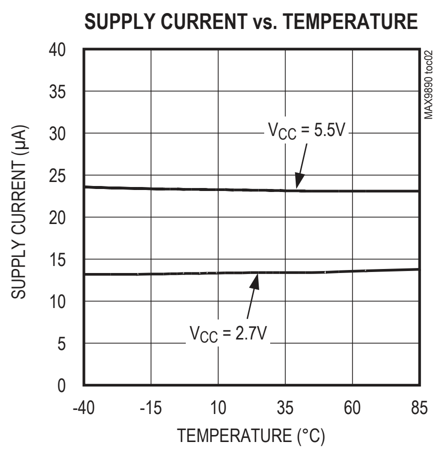
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUT ($\overline{SHDN}$)						
Logic-Input High Voltage	V_{IH}	V_{CC} = 2.7V to 5.5V	2.0			V
		V_{CC} = 2.7V to 5.5V, MAX9890BETA/V+ only, T_A = -40°C	2.2			
Logic-Input Low Voltage	V_{IL}	V_{CC} = 2.7V to 5.5V			0.8	V
Logic-Input Current	I_{IN}				±1	µA

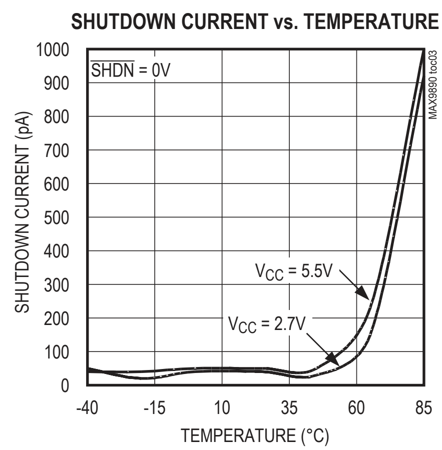
Note 1: All devices are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Supply current is measured when switch is on (i.e., $\overline{SHDN}$ = V_{CC}, t > t_{ON}).
Note 3: Supply voltage level where the device enters its power-down cycle.
Note 4: Turn-on time is measured from the time V_{CC} = 3V and $\overline{SHDN}$ > V_{IH} until the RON specification is met.
Note 5: Switch turn-off time is measured from the time $\overline{SHDN}$ < V_{IL} or V_{CC} < V_{UVLO} until the off-isolation specification is met.
Note 6: See the *Power-Supply Rejection Ratio* section for test method.

Typical Operating Characteristics

(V_{CC} = 3V, C_{CEXT} = 0.1µF, typical values are at T_A = +25°C, unless otherwise noted.)



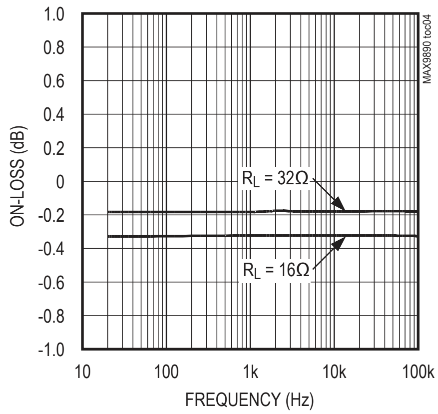




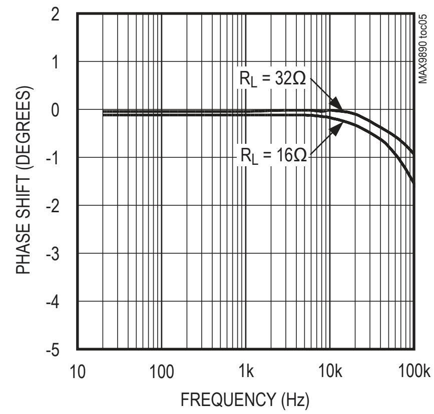
Typical Operating Characteristics (continued)

(V_{CC} = 3V, C_{CEXT} = 0.1µF, typical values are at T_A = +25°C, unless otherwise noted.)

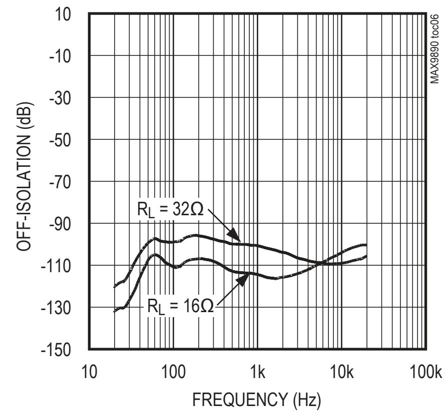
ON-LOSS vs. FREQUENCY



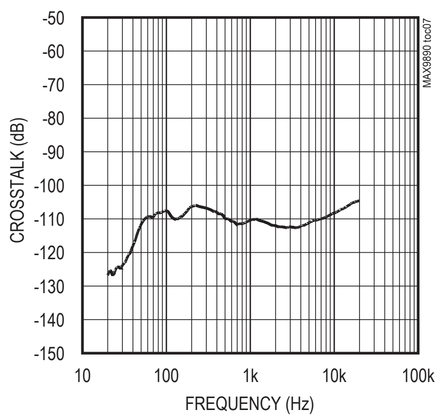
PHASE SHIFT vs. FREQUENCY



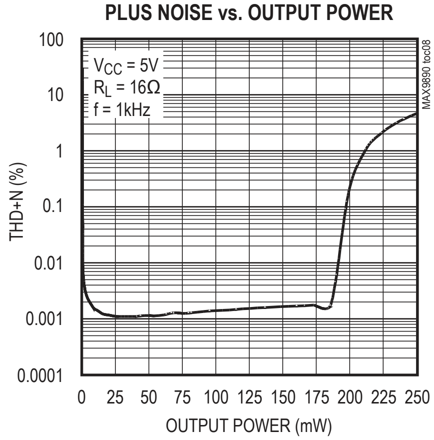
OFF-ISOLATION vs. FREQUENCY



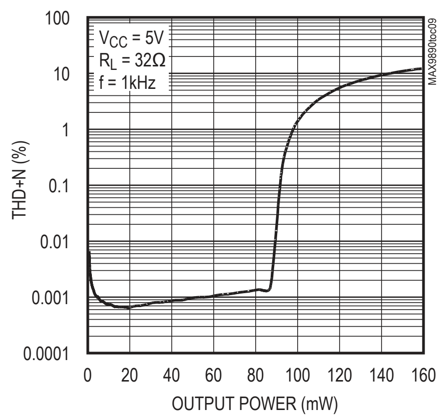
CROSSTALK vs. FREQUENCY



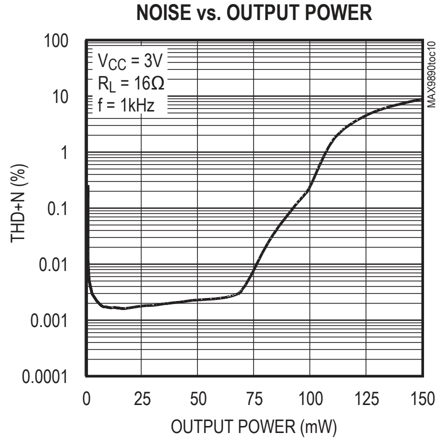
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



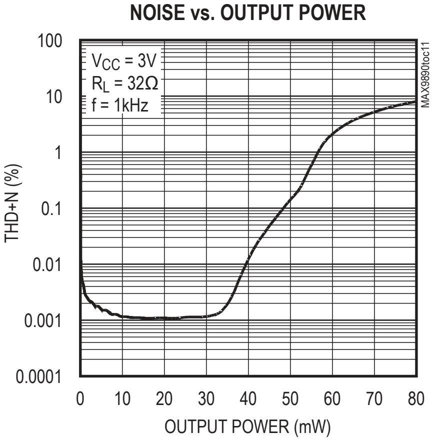
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



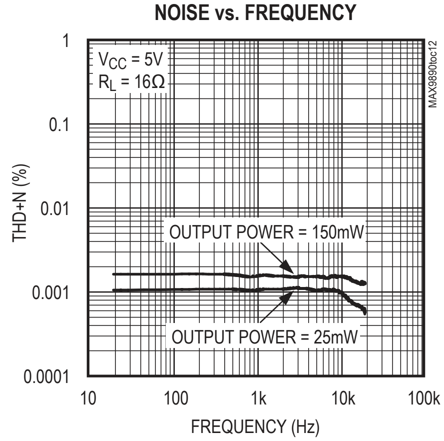
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



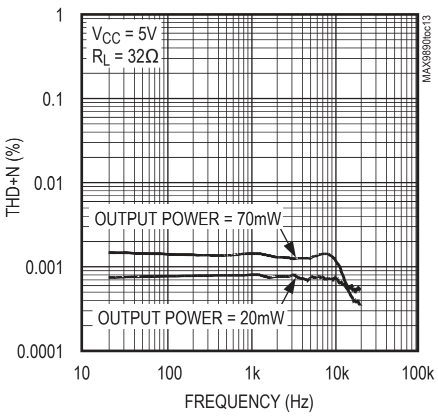
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



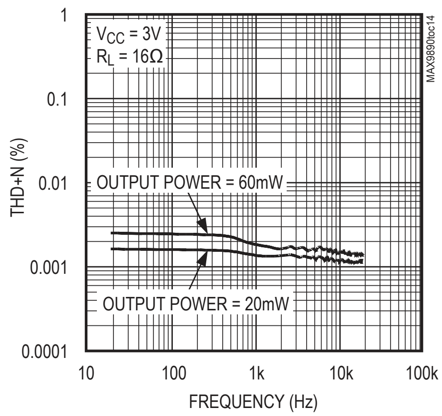
Typical Operating Characteristics (continued)

(V_{CC} = 3V, C_{CEXT} = 0.1μF, typical values are at T_A = +25°C, unless otherwise noted.)

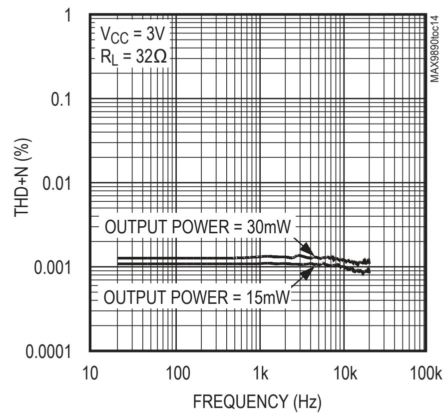
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



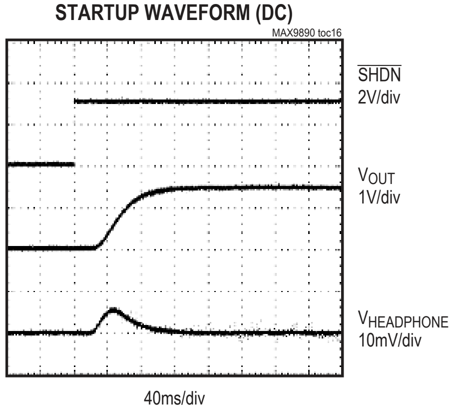
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



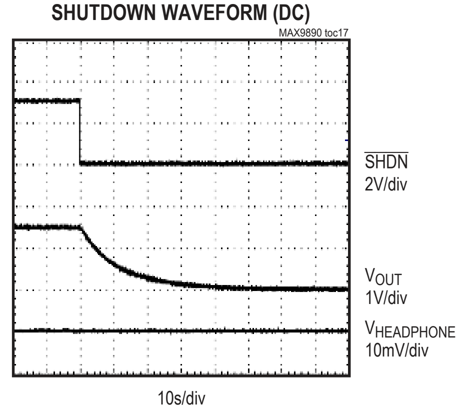
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



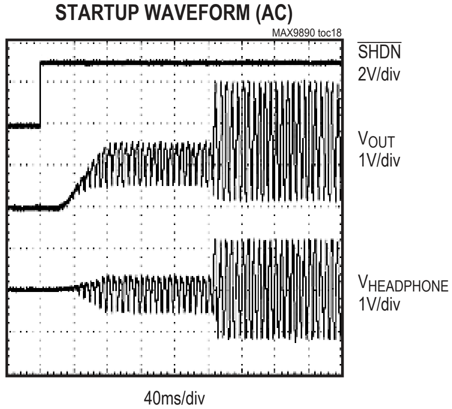
STARTUP WAVEFORM (DC)



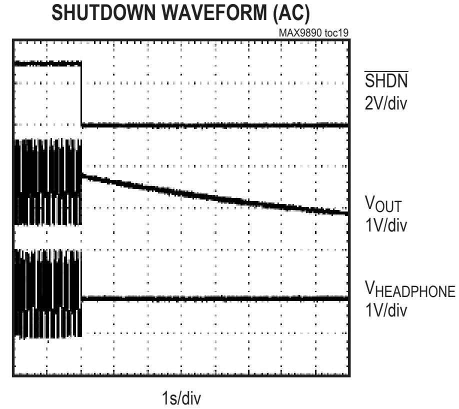
SHUTDOWN WAVEFORM (DC)



STARTUP WAVEFORM (AC)



SHUTDOWN WAVEFORM (AC)



Pin Description

PIN/BUMP		NAME	FUNCTION
TDFN	UCSP		
1	C2	V_{CC}	Power Supply. V_{CC} accepts 2.7V to 5.5V input supply. Bypass VCC to GND with a 1µF capacitor.
2	C1	$\overline{SHDN}$	Active-Low Shutdown. Connect $\overline{SHDN}$ to GND to enter a 0.1µA shutdown mode. Connect $\overline{SHDN}$ to V_{CC} for normal operation.
3	B1	INL	Left-Channel Audio Input. Connect to output of headphone amplifier.
4	A1	OUTL	Left-Channel Audio Output. AC couple to headphone.
5	A2	GND	Ground
6	A3	OUTR	Right-Channel Audio Output. AC couple to headphone.
7	B3	INR	Right-Channel Audio Input. Connect to output of headphone amplifier.
8	C3	CEXT	External Capacitor. Connect a 0.1µF capacitor from CEXT to GND.

Detailed Description

The MAX9890 provides click-and-pop suppression for single-supply devices such as CODECs and other headphone amplifiers that do not have click-and-pop suppression. Single-supply audio amplifier outputs have a DC bias voltage, V_{CC} / 2, and require large output-coupling capacitors to block the DC voltage from the speaker. During startup or shutdown, the DC bias voltage is quickly raised or lowered (Figure 1), resulting in an audible transient through the headphone load. The MAX9890 prevents the audible transient by slowly ramping the DC bias in an S-shaped waveform (Figure 2), suppressing the large transient at the output of the coupling capacitor. The S-shaped waveform shapes the frequency spectrum, minimizing the amount of audible components present at the output.

Internal switches couple the inputs to the outputs after the coupling capacitors have fully charged to the input common-mode bias voltage. When power is removed or the device is put into shutdown, the internal switches in the MAX9890 immediately disconnect the output and slowly discharge the coupling capacitors through 220kΩ resistors.

The MAX9890 has an undervoltage lockout (UVLO) that prevents device operation when V_{CC} is below the power-down threshold (2.5V, typ). The MAX9890 features ±8kV ESD (Human Body Model) protection on the audio outputs.

Startup

The MAX9890 monitors V_{CC} and $\overline{SHDN}$. The UVLO holds the device off when V_{CC} is below the power-down threshold (V_{UVLO}) or $\overline{SHDN}$ is held low. The device needs both V_{CC} above the power-down threshold and $\overline{SHDN}$ = high for the part to start up. Once the supply voltage is above the power-down threshold and $\overline{SHDN}$ is high, the device charges the coupling capacitors to the input DC bias voltage using CEXT to control the ramp. After the DC bias ramp, the internal switches close, coupling the audio input to the output. The MAX9890 provides click-pop suppression even if the output blocking capacitors are already partially or fully charged.

The MAX9890A features a 200ms switch turn-on time, enabling the use of up to 100µF coupling capacitors at the output for applications requiring only a limited low-frequency response and a rapid turn-on time. The MAX9890B features a 330ms switch turn-on time, enabling the use of >100µF coupling capacitors at the output for extended low-frequency response applications. For optional click-pop suppression, mute the audio signal until after the turn-on time has elapsed.

The internal switches stay closed as long as V_{CC} is above the power-down threshold voltage and $\overline{SHDN}$ is high. Figures 1 and 2 show typical startup/power-up sequences with and without click-pop suppression.

Shutdown

If the supply voltage falls below the UVLO threshold or if $\overline{SHDN}$ is driven low, the device enters low-power shutdown mode. In low-power shutdown mode, quiescent current reduces to 0.001µA. The switches are immediately turned off and 220kΩ resistors slowly bleed the charge off the coupling capacitors. Figures 3 and 4 show typical shutdown/power-down sequences with and without click-pop suppression. For optimal click-pop performance, mute the audio signal before shutting down the MAX9890.

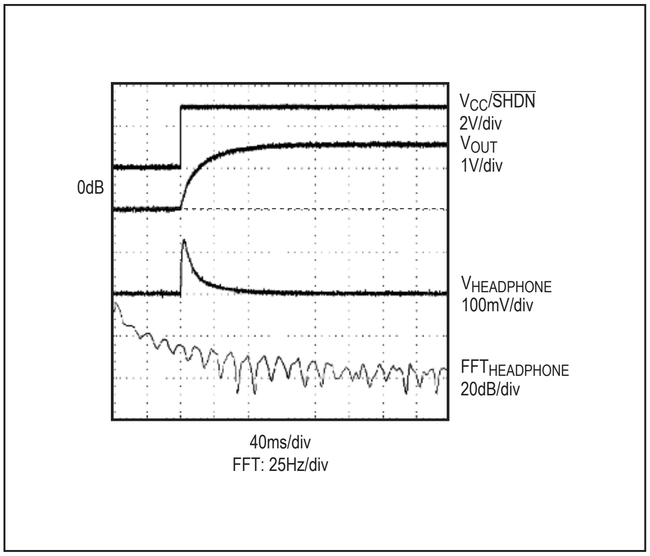


Figure 1. Startup/Power-Up Sequence Without Click-Pop Suppression

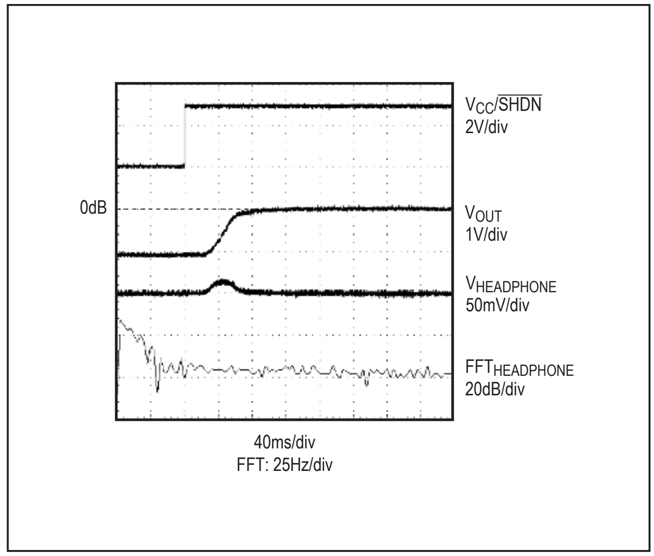


Figure 2. Startup/Power-Up Sequence With Click-Pop Suppression

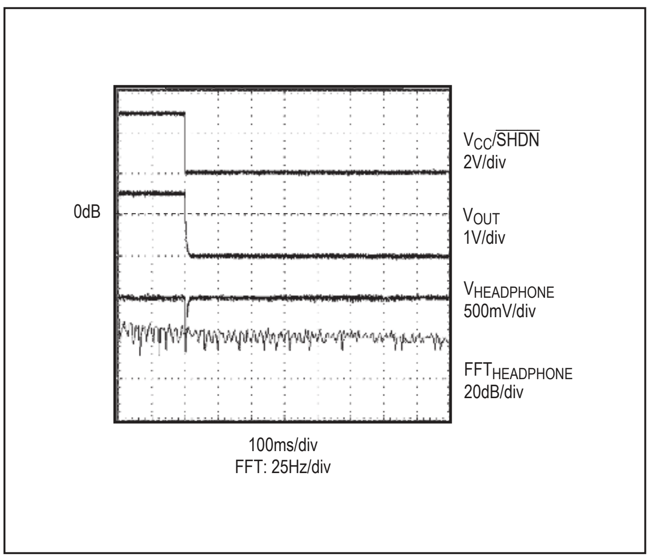


Figure 3. Shutdown/Power-Down Sequence Without Click-Pop Suppression

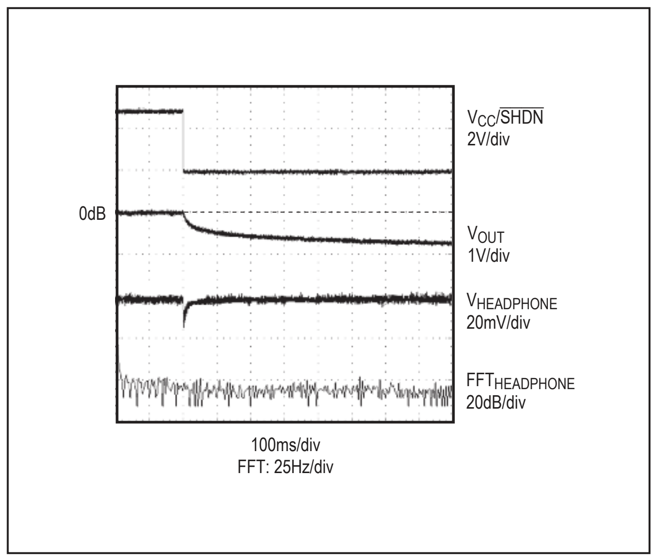


Figure 4. Shutdown/Power-Down Sequence With Click-Pop Suppression

Switches

The MAX9890's internal switches connect the input to the output after the coupling capacitors are fully charged. The MAX9890A holds the switches open for 200ms and is ideal for coupling capacitors less than 100µF. The MAX9890B has a longer turn-on time of 330ms and is ideal with larger coupling capacitors less than 220µF. The internal switches have a low on-resistance (R_{ON} = 0.5Ω) and on-resistance flatness ($R_{FLAT(ON)}$ = 2mΩ) minimizing total harmonic distortion plus noise (THD+N). The relationship below shows the contribution to THD+N through the switch, due to on-resistance and on-resistance flat-

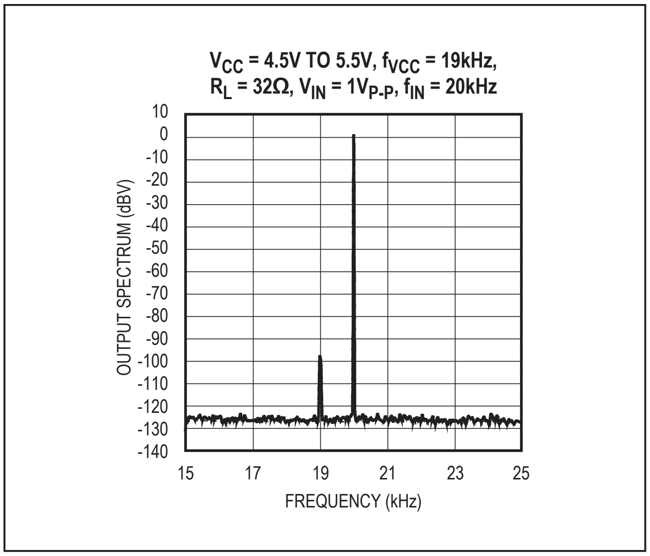


Figure 5. FFT for PSRR

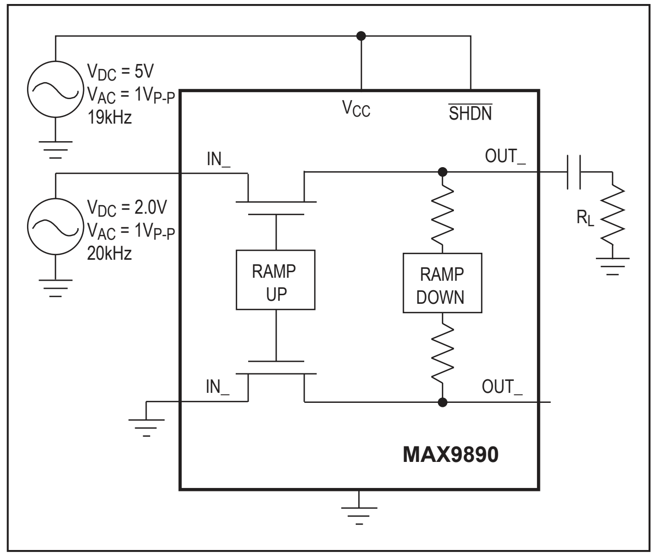


Figure 6. PSRR Test Circuit

ness (on-resistance flatness is defined as the difference between the maximum and minimum values of on-resistance measured over the specific analog-signal range).

$$THD_{MAXIMUM} = \frac{R_{FLAT(ON)}}{4R_{LOAD}} \times 100\%$$

Power-Supply Rejection Ratio (PSRR)

PSRR is the measurement of AC power-supply ripple or noise that couples to the output. Variations in supply voltage corrupt the audio signal, due to changes in the R_{ON} value by supply modulation. The FFT shown in Figure 5 was taken with a 19kHz $1V_{P-P}$ sine wave onto the 5V DC supply voltage, and a 20kHz $1V_{P-P}$ sine wave applied at IN_ with a 32Ω load is shown in Figure 6. The MAX9890 maintains a -100dB (typ) PSRR across the supply voltage range eliminating any corruption of the audio signal from supply variations. Therefore, with a zero audio signal, the R_{ON} variation due to supply voltage ripple does not contribute to any output signal modulation.

Low-Frequency Response

In addition to the cost and size disadvantages of the output-coupling capacitors, these capacitors limit the amplifier’s low-frequency response and can distort the audio signal.

The impedance of a headphone or speaker load and the output-coupling capacitor form a highpass filter with the -3dB point set by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

where R_L is the headphone impedance and C_{OUT} is the output-coupling capacitor value. The highpass filter is required by conventional single-ended, single power-supply headphone drivers to block the midrail DC bias component of the audio signal from the headphones. The drawback to the filter is that it can attenuate low-frequency signals. Larger values of C_{OUT} reduce this effect but result in physically larger, more expensive capacitors. Figure 7 shows the relationship between the size of C_{OUT} and the resulting low-frequency attenuation. Note that the -3dB point for a 16Ω headphone with a 100µF blocking capacitor is 100Hz, well within the normal audio band, resulting in low-frequency attenuation of the reproduced signal.

The MAX9890A and MAX9890B have different turn-on times to accommodate different size output-coupling capacitors (see Table 1). Using a capacitor smaller than the specified maximum allowed does not degrade click-pop suppression. Therefore, capacitors less than 100µF can be used with the A or B version devices.

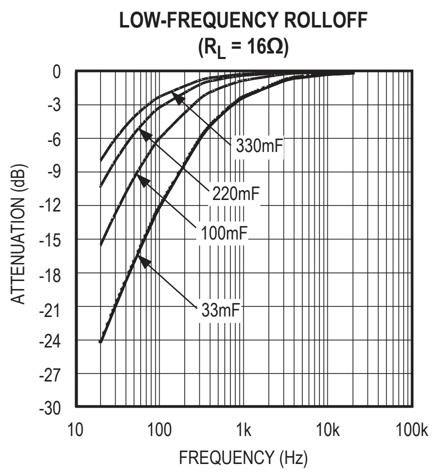


Figure 7. Low-Frequency Attenuation for Common DC-Blocking Capacitor Values

Table 1. Coupling Capacitor

CAPACITOR SIZE (µF)	MAX9890A TURN-ON TIME (200ms)	MAX9890B TURN-ON TIME (300ms)
33	√	√
47	√	√
100	√	√
150	*	√
220	*	√
330	—	*
470	—	*

**May experience some degradation of click-pop suppression.*

External Capacitor (C_{CEXT})

The external click-pop suppression capacitor at CEXT serves a dual purpose. On power-up, C_{CEXT} is charged by an internal current source and is used to slowly ramp up the external coupling capacitors. When the device is powered down, C_{CEXT} powers the internal circuitry used to drain the external coupling capacitors. A 0.1µF capacitor between CEXT and GND provides clickless/popless operation with coupling capacitors for both the MAX9890A and MAX9890B, even with the rapid removal of supply voltage.

Applications Information

Layout

Good layout improves performance by decreasing the amount of stray capacitance and noise. To decrease stray capacitance, minimize PC board trace lengths and resistor leads, and place external components as close to the device as possible.

Power Supply and Bypassing

The excellent PSRR of the MAX9890 allows it to operate from noisy power supplies. In most applications, a 0.1µF capacitor from V_{CC} to GND is sufficient. This bypass capacitor should be placed close to V_{CC}.

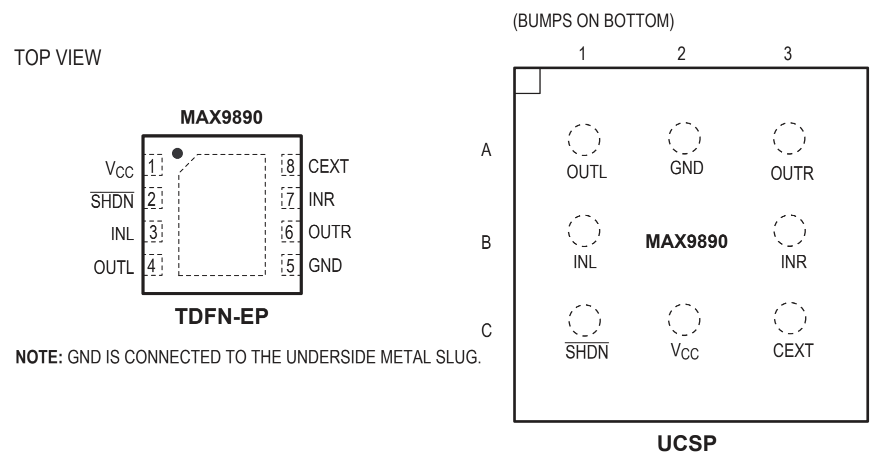
UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape-carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to *Application Note 1891: Wafer-Level Packaging (WLP) and its Applications* at www.maximintegrated.com/UCSP.

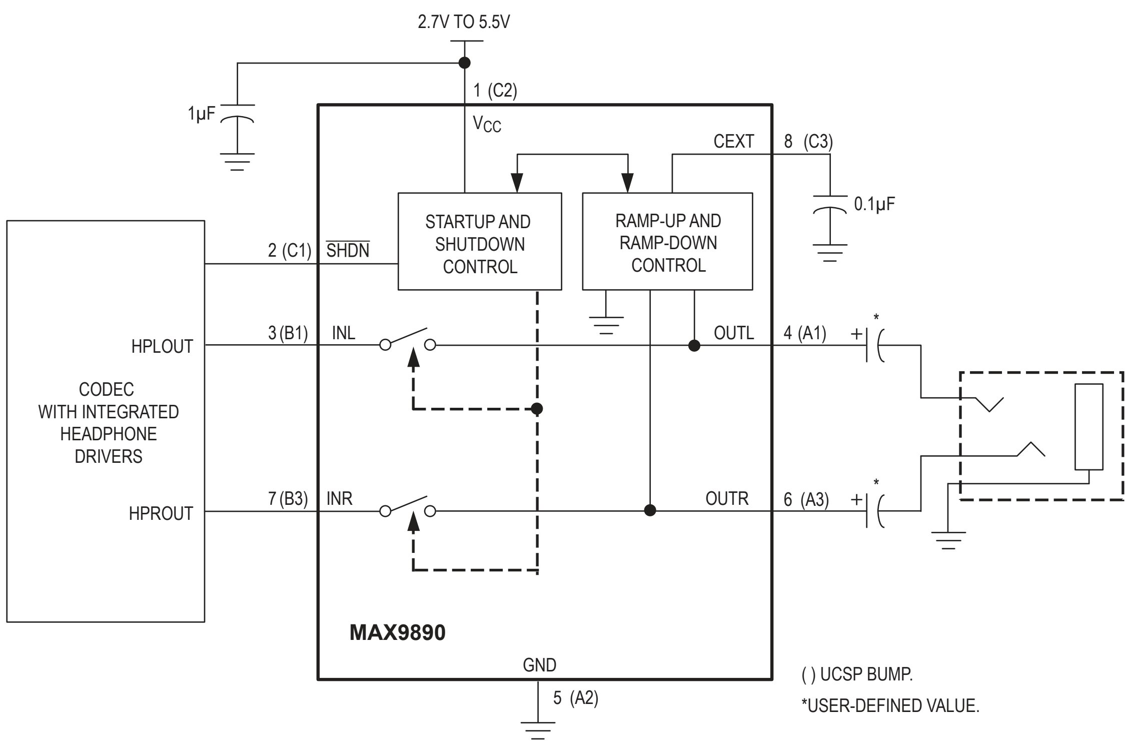
Chip Information

PROCESS: BiCMOS

Pin Configurations



Typical Application Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
UCSP	B9+2	**21-0093**	Refer to **Application Note 1891**
TDFN-EP	T833+2	**21-0137**	**90-0059**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	3/14	Added the MAX9890BETA/V+ to the *Ordering Information*, *Selector Guide*, and *Electrical Characteristics* tables	1, 3
4	5/17	Updated MAX9890AEBL-T, MAX9890BEBL-T to MAX9890AEBL+T, MAX9890BEBL+T in the *Ordering Information* and *Selector Guide* tables	1