# Description _____

Microsemi's™ PoE controller, the PD69000 is a cost-effective, pre-programmed unit with an application used to implement Enhanced mode. It is used in conjunction with Microsemi's PoE Managers PD69012 and PD69008 in Ethernet switches to allow next generation network devices to share power and data over the same cable, as specified in the IEEE standard 802.3af and the IEEE802.3at-draft2.0. When used in conjunction with the PD69000, the PD69012/PD69008 operate in Enhanced mode, which allows the user to operate in a total Power-over-Ethernet stand-alone mode.

The controller features an ESPI bus for each of the PoE devices and a communication interface with the Host CPU via UART or I^2C protocol.

The device is based on Freescale's MC9S08 MCUs family. It includes an asynchronous serial communications interface, a serial peripheral interface and a dual 2-channel, 16 bit timer. In addition, it includes an 8-channel 10-bit analog-to-digital converter.

Pin Configuration _____
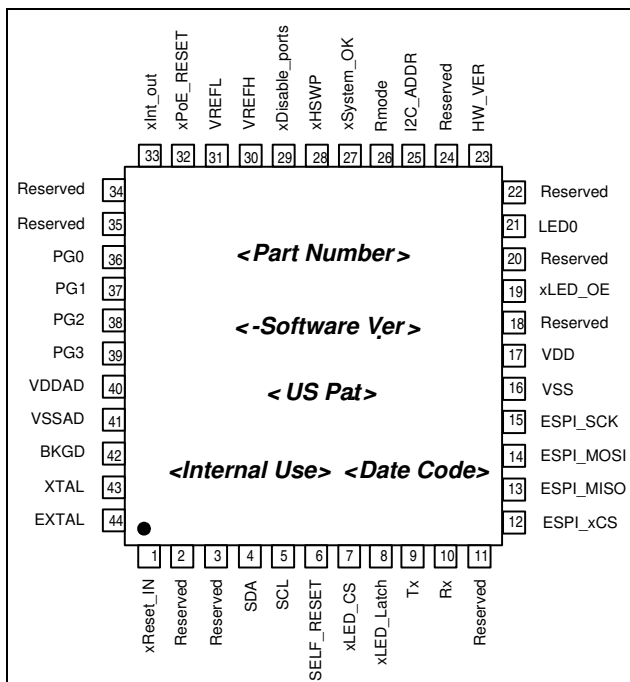
Marking Definitions_____

The label on the device includes the following:

♦ **<Part number>** Hardware P/N (e.g. PD69000)
♦ **<Software Ver>** software version (e.g. 0120)
♦ **<US Pat>** USA patent number of Microsemi
♦ **<Internal Use>** factory Internal Use
♦ **<Date Code>** Burning date code in the following format: yyww (yy = year, ww = week)

Supported Features _____

♦ Controls up to 96 PoE ports (8 x PD69012)
♦ Pre-Standard / Capacitor detection
♦ Detection of Cisco devices
♦ Supports both UART and I^2C interfaces to the Host CPU
♦ Backwards compatible with the PD63000, PD62000 and PDIC66000
♦ Power Management for up to 96 ports
♦ Rmode pin for default parameters selection
♦ Programmable over-voltage and under voltage
♦ Pre-defined power budget – 16 discrete levels
♦ LED stream support
♦ System-OK indication
♦ Software download via I^2C or UART
♦ System and port measurements
♦ Detailed port status
♦ Thermal protection and monitoring
♦ Programmable temperature alarm limit
♦ Interrupt out pin for system and port events
♦ Forced power for system testing
♦ System reset
♦ Port power limit setting
♦ Port matrix and priority
♦ Automatic PoE device type detection
♦ RoHS compliant

Ordering Information _____

Part Number	Disconnect	Detection	Version
PD69000xy-gggg	x = A: AC x = D: DC	y = R: Resistor y = C: Resistor/legacy	gggg*

*For the latest firmware version available, refer to Microsemi website or to customer care support.

Firmware Download _____
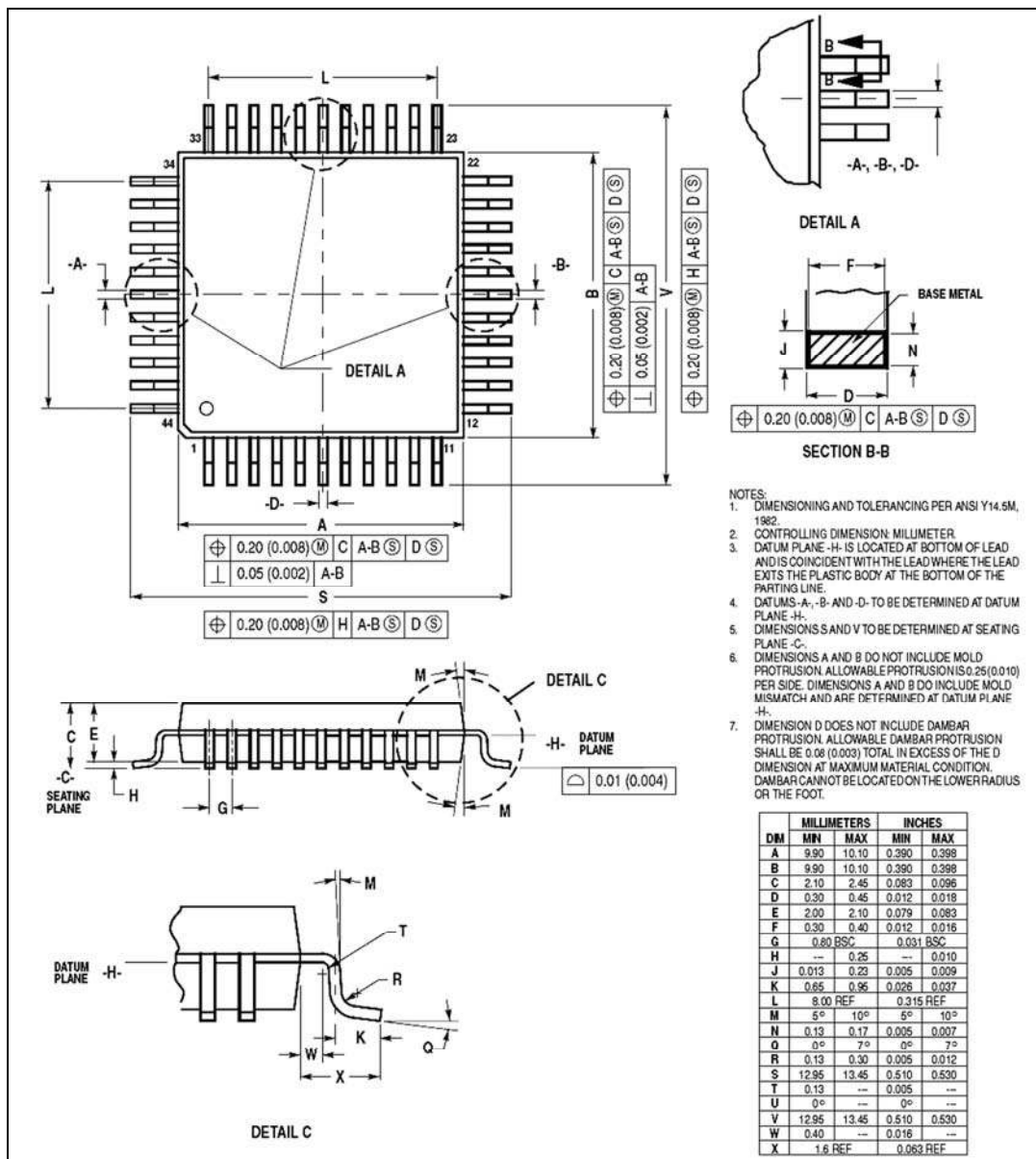
Initial burning of the controller's firmware is performed in the factory.
Firmware upgrades can be performed by the user using the communication interface (see Application Note 126 Cat No. 06-0006-080).

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Applicable Documents _____

- ♦ IEEE 802.3af-2003 standard, DTE Power via MDI
- ♦ IEEE 802.3at-draft2.0
- ♦ Microsemi PD69012 Data Sheet, Cat. No. 06-0072-058
- ♦ Microsemi PD69008 Data Sheet, Cat. No. 06-0071-058
- ♦ Serial communication protocol User Guide 06-0032-056
- ♦ Microsemi Application Note 174 for Designing 48-port Enhanced PoE System (802.3af/802.3at Compliant), Cat. No. 06-0054-080
- ♦ Application Note 126: Software Download for PoE Units, Cat. No. 06-0006-080
- ♦ Freescale Semiconductor MC9S08GT60ACFB electrical characteristics

Package Information _____

The PD69000 is housed in a 44-pin QFP plastic package, 10 x 10 x 2 mm.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	--	0.25	--	0.010
J	0.013	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	--	0.005	--
U	0°	--	0°	--
V	12.95	13.45	0.510	0.530
W	0.40	--	0.016	--
X	1.6 REF		0.063 REF	

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Pin Functionality _____

PIN	PIN NAME	PIN TYPE	PIN DESCRIPTION	PIN	PIN NAME	PIN TYPE	PIN DESCRIPTION
1.	xReset_In	Digital input	Reset input	23	HW_VER	A/D input	Hardware version
2.	Reserved	Digital output		24	Reserved	A/D input	
3.	Reserved	Digital output		25	I2C_ADDR	A/D input	I2C address of PD69000
4.	SDA	Digital I/O	I2C data	26	Rmode	A/D input	N/A
5.	SCL	Digital input	I2C clock	27	xSystem_OK	Digital output	System validity indication
6.	Self_reset	Digital output	Internal self Reset	28	xHSWP	Digital I/O	N/A
7.	xLED_CS	Digital output	Chip select for LED stream	29	xDisable_ports	Digital input	Disable all PoE Ports
8.	xLED_Latch	Digital output	Latch for LED stream	30	VREFH	A/D ref. voltage	Reference high level
9.	Tx	Digital output	UART transmit	31	VREFL	A/D ref. voltage	Reference low level
10	Rx	Digital input	UART receive	32	xPoE_RESET	Digital output	Reset to PoE managers
11	Reserved	Digital output		33	xInt_Out	Digital output	Interrupt output indication
12	ESPI_xCS	Digital I/O	ESPI bus to PoE manager	34	Reserved	Digital I/O	
13	ESPI_MISO	Digital I/O	ESPI bus to PoE manager	35	Reserved	Digital I/O	
14	ESPI_MOSI	Digital I/O	ESPI bus to PoE manager	36	PG0	Digital input	Power Good #0
15	ESPI_SCK	Digital output	ESPI bus to PoE manager	37	PG1	Digital input	Power Good #1
16	VSS	Digital ground	Digital ground	38	PG2	Digital input	Power Good #2
17	VDD	Digital power	Main Supply 3.3v	39	PG3	Digital input	Power Good #3
18	Reserved	Digital I/O	Shorted to pin 20	40	VDDAD	Analog power	Main Supply 3.3v
19	xLED_OE	Digital I/O	Enable for status LED	41	VSSAD	Analog ground	Analog ground
20	Reserved	Digital I/O	Shorted to pin 18	42	BKGD	Digital I/O	BDM burn-in
21	LED0	Digital I/O		43	XTAL	Analog output	Oscillator output
22	Reserved	Digital I/O		44	EXTAL	Analog input	Oscillator input

Electrical Specification_____

Comment: For detailed electrical specification refer to the following datasheets (at: www.freescale.com)

- Manufacturer - Freescale Semiconductor
- Manufacturer part number - MC9S08GT60A

Main Features Description _____

Function	Description
Supports up to eight PoE devices, 96 ports	The PoE devices can be cascaded for up to eight PoE devices, that will fit into a 96 ports PoE system utilizing one PoE Controller (PD69000)
Power management	The system supports two power management modes: Class mode, Dynamic mode and static mode. See Technical Note 113, Cat. No. 06-0002-081 for more details.
Threshold configuration	Over-voltage and under-voltage thresholds configuration for disconnection purposes.
High Power ports	The PoE devices can be configured (both hardware and software) so as to enable higher current through ports (up to ~720mA)
Communication	Supports both I²C and UART interfaces with Host CPU.
Legacy (capacitor) detection	Allows detection and powering of pre-standard devices (PDs).
LED stream	Direct SPI interface to an external LED Stream circuitry. It allows the designer to implement a simple LED circuit that does not require a software code.
System OK indication	Digital output pin to the Host, indicating that voltage and temperature range are valid.
System and port measurements	Measurements of the following parameters: Current (mA), Power consumption (W), Vmain (V), Port voltage (V), Class of PD (0-4).
Detailed port status	Port statuses are received from PoE managers such as: port on, port off due to disconnection or due to overload
Interrupt pin	Interrupt out from the PoE Controller indicating events such as: Port On, Port Off, Port Fault, PoE device Fault, Voltage out of range and more. For a full list of interrupt events, refer to Serial Communication Protocol, Cat. No. 06-0032-056.
Port power limit	Configurable Port power limit; when a port exceeds power limit, it is automatically disconnected
Power matrix control	Allows the layout designer to connect all physical ports to the logical ports whenever desired.
'Power Good' interrupt from power supply	For systems comprising more than a single power supply, a fast port disconnection mechanism is executed in cases where one power supply fails, in order to maintain operation and prevent collapse of the other power supplies.

I²C Address Selection_____

I²C interface between the Host CPU and a specific PD69000 requires the setting of address for the device; this is done by applying a specific voltage level to pin#25 (I2C_ADDR) as shown below:

I2C_ADDR Voltage Level	I²C Address (hexadecimal)
0.00 to 0.21 V	UART
0.21 to 0.41 V	0x4
0.41 to 0.62 V	0x8
0.62 to 0.83 V	0xC
0.83 to 1.03 V	0x10
1.03 to 1.24 V	0x14
1.24 to 1.44 V	0x18
1.44 to 1.65 V	0x1C
1.65 to 1.86 V	0x20
1.86 to 2.06 V	0x24
2.06 to 2.27 V	0x28
2.27 to 2.48 V	0x2C
2.48 to 2.68 V	0x30
2.68 to 2.89 V	0x34
2.89 to 3.09 V	0x38
3.09 to 3.30 V	0x3C

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Revision History

Revision Level / Date	Para. Affected	Description
1.0 31/ August.08		Initial release
1.1 22/ January.09	P3	Comment added
1.1 27 Jul 10		Changing catalog numbers metrology

For support contact: sales_AMSG@microsemi.com
Visit our web site at: **www.microsemi.com**   **Cat. No. DS_PD69000**

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