

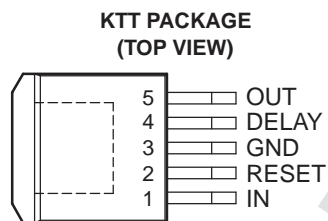
400-mA, 5-V OUTPUT, HIGH INPUT VOLTAGE LDO VOLTAGE REGULATOR

FEATURES

- Output Voltage 5 V \pm 2%
- Very Low over all Current Consumption
- Very low noise: 15.5 μ V
- Power-On and Undervoltage Reset
- Reset Low-Level Output Voltage < 1 V
- Very Low Dropout Voltage
- Short-Circuit Protection
- Reverse-Polarity Protection
- ESD (HBM) Protection > 6 kV

APPLICATIONS

- Industrial Systems
- Distributed Power Systems
- White Goods



DESCRIPTION

The TPS78405 is a very low-noise monolithic integrated low-dropout voltage regulator offered in a 5-pin TO (KTT) package. An input voltage up to 45 V is regulated to $V_{OUT} = 5$ V (typ). The device can drive loads up to 400 mA and is short-circuit proof. At overtemperature, the TPS78405 is turned off by the incorporated temperature protection. A reset signal is generated for an output voltage ($V_{OUT,rt}$) of 4.65 V (typ). The reset delay time can be programmed by the external delay capacitor.

The input capacitor, C_{IN} (1 μ F Tantalum), compensates for line fluctuation. Using a resistor of approximately 1 Ω , in series with C_{IN} , dampens the oscillation of input inductivity and input capacitance. The output capacitor, C_{OUT} , stabilizes the regulation circuit. Stability is specified at C_{OUT} (Tantalum) ≥ 22 μ F and ESR ≤ 5 Ω , within the operating temperature range.

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The device also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity
- Overvoltage shutdown

ORDERING INFORMATION⁽¹⁾

T _A	V _{OUT} (TYP)	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	5 V	TO-263 (KTT)	Reel of 500	TPS78405KTTR	TPS78405

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



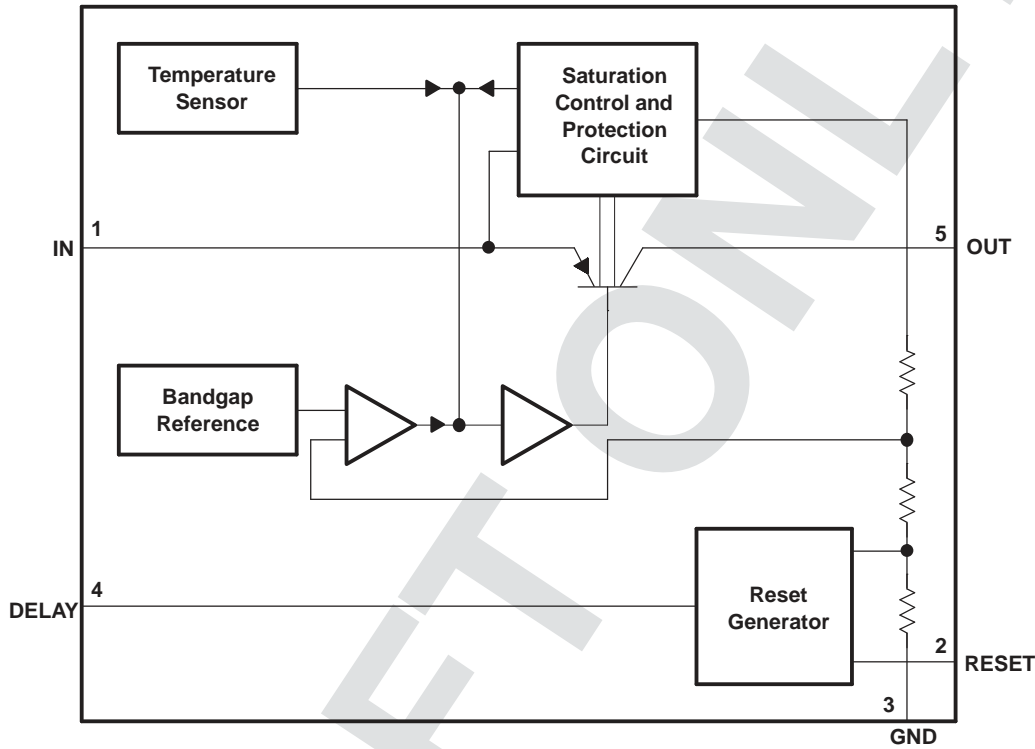
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	IN	Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than 1 inch away from the main input filter capacitor. In general, the output impedance of power supply rises with frequency, so it is advisable to include a bypass capacitor. A ceramic bypass capacitor in range of 1 μ F to 10 μ F is sufficient. The TPS78405 regulator is designed to withstand reverse voltage on IN with respect to ground. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input, so that no reverse current flow into the regulator and no reverse voltage appears at the load. The device protects both itself and the load.
2	RESET	Reset output. Open-collector output. When the output voltage drops below 4.65 V, the transistor is turned on. The maximum driving current is 5 mA, and maximum collector voltage is 13 V. RESET can be used to monitor the output voltage using an LED.
3	GND	Ground. This is the return of the circuit and is connected internally to the device heatsink.
4	DELAY	Reset delay. Used for setting the reset delay time using a capacitor to set the delay time (see Figure 2). DELAY charges the capacitor from 5.5- μ A current sources.
5	OUT	Output. Supplies power to the load. A minimum output capacitor (tantalum) of 22 μ F and ESR < 5 Ω is required to prevent oscillations. A larger output capacitor is required for applications with large transient loads to limit peak voltage transients.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

Input voltage range, $V_{IN}^{(2)}$	IN	–42 V to 45 V
	DELAY	–0.3 V to 7 V
Output voltage range, V_{OUT}	OUT	–1 V to 16 V
	RESET	–0.3 V to 25 V
Input current, I_{IN}	DELAY	±2 mA
Output current for RESET, I_{RO}	RESET	±5 mA
ESD rating	Human-Body Model (HBM)	8 kV
Package thermal impedance, junction to free air, $\theta_{JA}^{(3)(4)}$		21.5°C/W
Operating virtual-junction temperature range, T_J		–40°C to 150°C
Storage temperature range, T_{stg}		–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.
- (3) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	5.5	42	V
T_J	Junction temperature	–40	150	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $V_{IN} = 13.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 150°C (unless otherwise noted) (see [Figure 1](#))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	$I_{OUT} = 5\text{ mA to }400\text{ mA}$, $V_{IN} = 6\text{ V to }28\text{ V}$	4.9	5	5.1	V
		$I_{OUT} = 5\text{ mA to }200\text{ mA}$, $V_{IN} = 6\text{ V to }42\text{ V}$	4.9	5	5.1	
I_{OUT}	Output current limit	$V_{IN} = 6\text{ V}$, $-40^\circ\text{C} - 125^\circ\text{C}$	400	700		mA
I_{GND}	Current consumption $I_{GND} = I_{IN} - I_{OUT}$	$I_{OUT} = 1\text{ mA}$, $T_J = 25^\circ\text{C}$		150	200	μA
		$I_{OUT} = 1\text{ mA}$, $T_J \leq 85^\circ\text{C}$		150	220	
		$I_{OUT} = 250\text{ mA}$		5	8	mA
		$I_{OUT} = 400\text{ mA}$		12	16	
V_{DO}	Dropout voltage ⁽¹⁾	$I_{OUT} = 400\text{ mA}$, $V_{DO} = V_{IN} - V_{OUT}$, $T_J = 25^\circ\text{C}$		250	400	mV
		$I_{OUT} = 300\text{ mA}$,		200	400	
		$I_{OUT} = 300\text{ mA}$, $V_{DO} = V_{IN} - V_{OUT}$, $T_J = 25^\circ\text{C}$		200	300	
		$I_{OUT} = 100\text{ mA}$, $V_{DO} = V_{IN} - V_{OUT}$, $T_J = 25^\circ\text{C}$		80	100	
	Load regulation	$I_{OUT} = 5\text{ mA to }400\text{ mA}$		10	15	mV
	Line regulation	$\Delta V_{IN} = 8\text{ V to }32\text{ V}$, $I_{OUT} = 5\text{ mA}$		5	15	mV
$I_{OUT(MAX)}$	Short-circuit current	$V_{IN} = V_{OUT} + 1\text{ V}$, $T_J = 25^\circ\text{C}$			1.2	A
PSRR	Power-supply ripple rejection	frequency = 120 Hz , $V_r = 0.5\text{ V}_{pp}$		60		dB
$\frac{\Delta V_O}{\Delta T}$	Temperature output-voltage drift			0.5		mV/K
e_n	Output noise voltage (RMS)	BW = $100\text{ Hz to }50\text{ kHz}$, $C_{OUT} = 22\text{ }\mu\text{F}$, $I_{OUT} = 5\text{ mA}$		15.5		μV
$V_{OUT,rt}$	RESET switching threshold		4.5	4.65	4.8	V
V_{ROL}	RESET output low voltage	$R_{ext} \geq 5\text{ k}\Omega$, $V_{OUT} > 1\text{ V}$		0.2	0.4	V
I_{ROH}	RESET output leakage current	$V_{RO} = 5\text{ V}$		0	5	μA
$I_{D,c}$	RESET charging current	$V_D = 1\text{ V}$	3	5.5	9	μA
V_{DU}	RESET upper timing threshold		1.5	1.8	2.2	V
V_{DRL}	RESET lower timing threshold		0.2	0.4	0.7	V

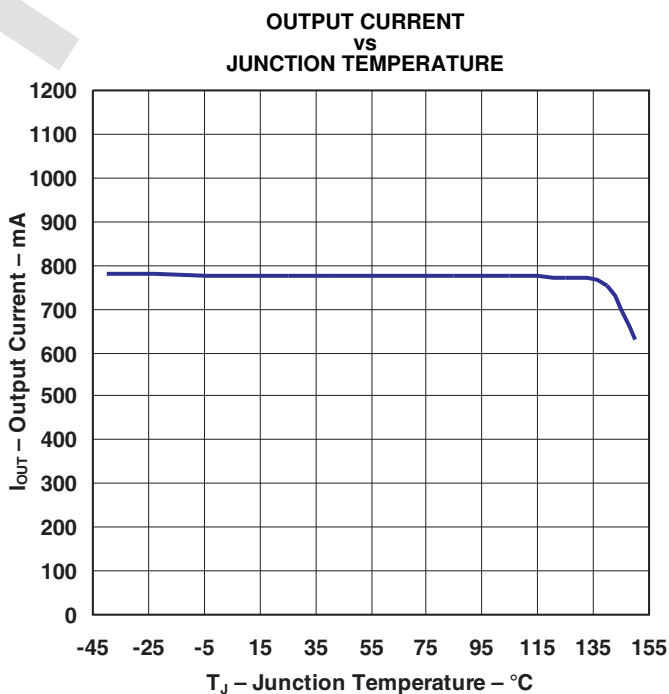
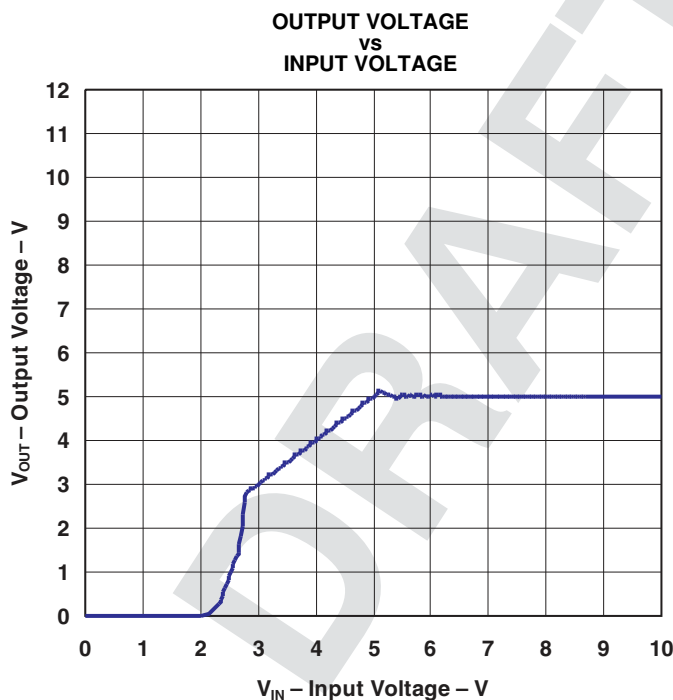
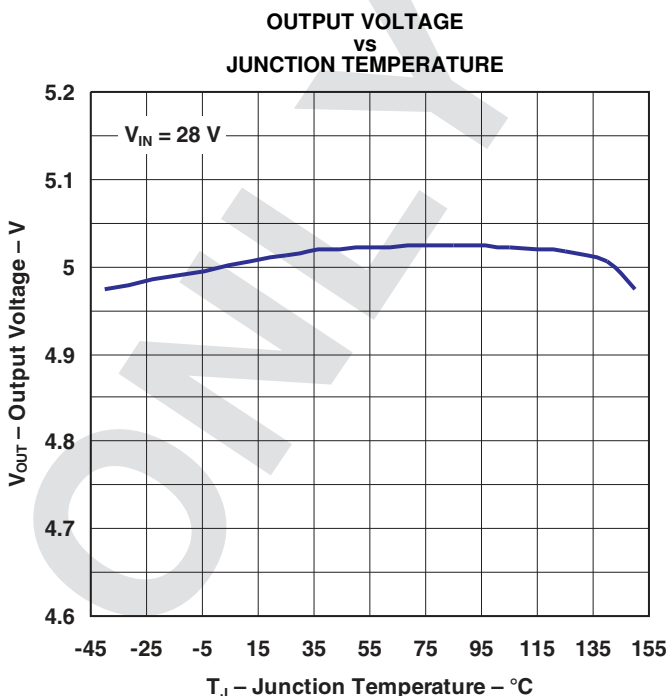
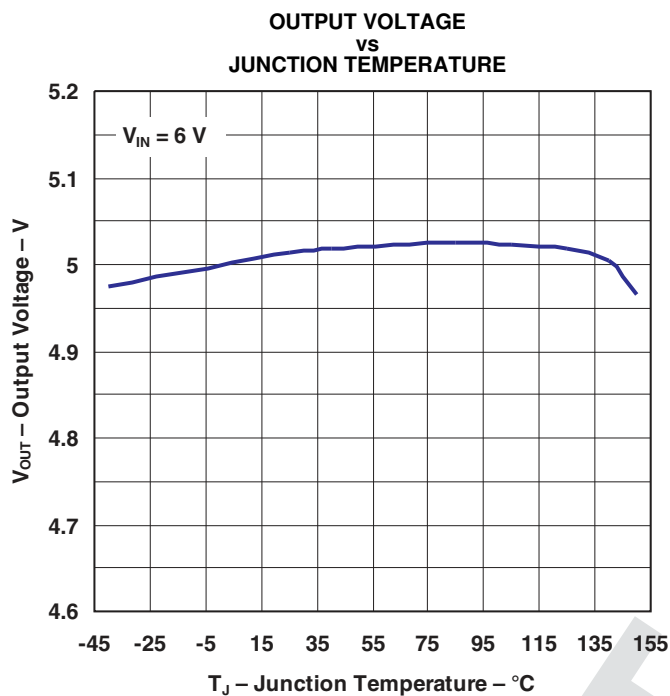
(1) Measured when the output voltage V_{OUT} has dropped 100 mV from the nominal value obtained at $V_{IN} = 13.5\text{ V}$.

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

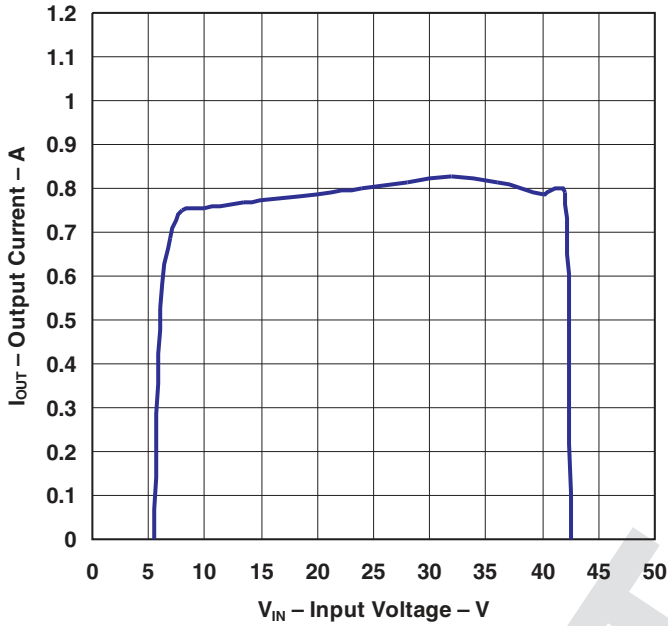
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rd}	RESET delay time	$C_D = 47\text{ nF}$	10	16	22	ms
t_{rr}	RESET reaction time	$C_D = 47\text{ nF}$		0.5	2	μs

TYPICAL CHARACTERISTICS

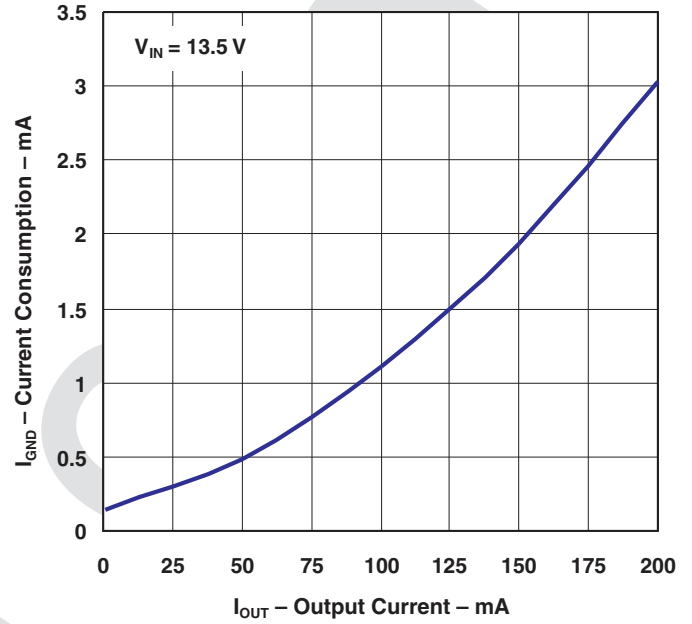


TYPICAL CHARACTERISTICS (continued)

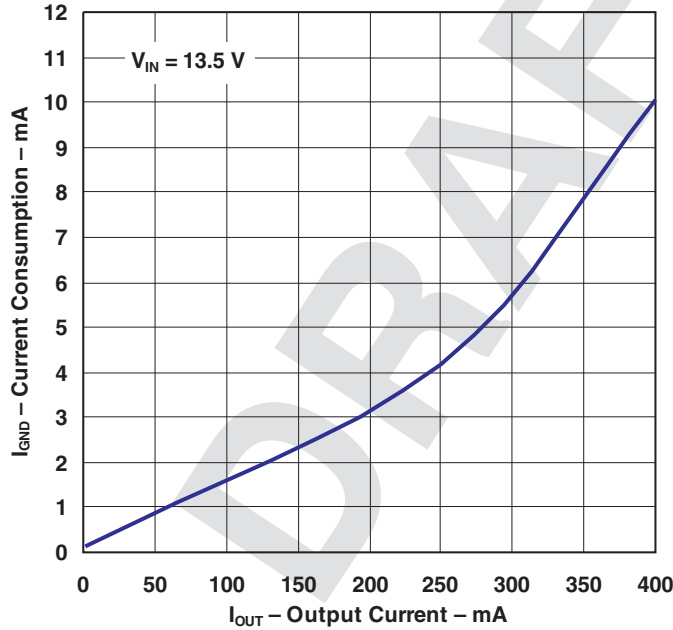
OUTPUT CURRENT
vs
INPUT VOLTAGE



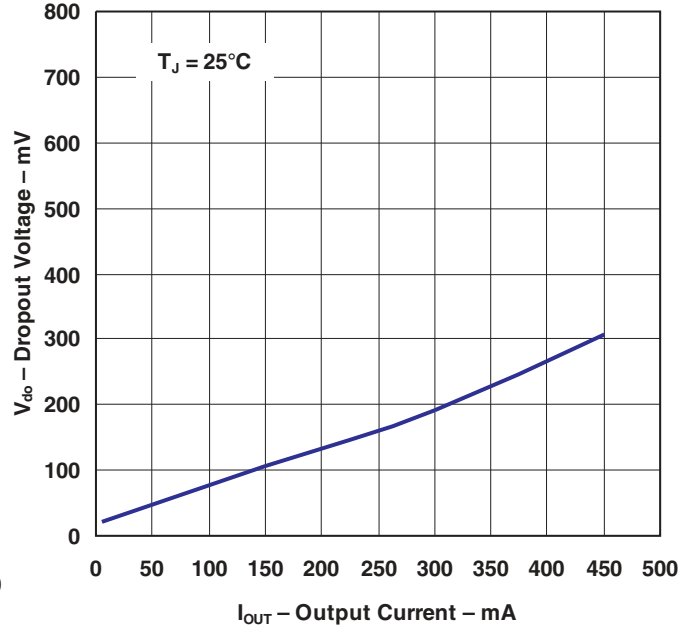
CURRENT CONSUMPTION
vs
OUTPUT CURRENT



CURRENT CONSUMPTION
vs
OUTPUT CURRENT

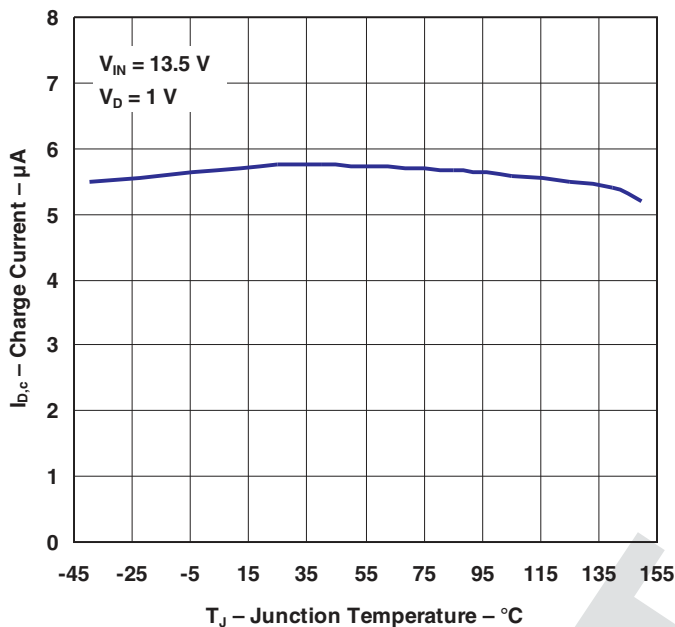


DROPOUT VOLTAGE
vs
OUTPUT CURRENT

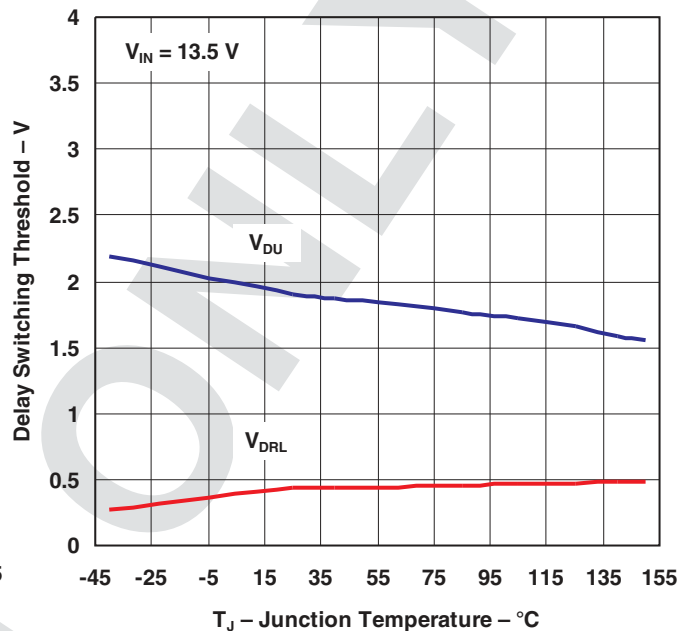


TYPICAL CHARACTERISTICS (continued)

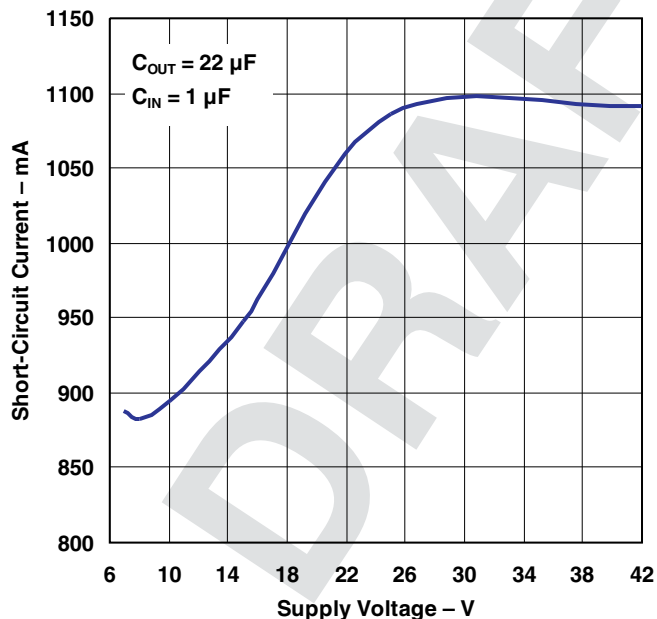
CHARGE CURRENT
vs
JUNCTION TEMPERATURE



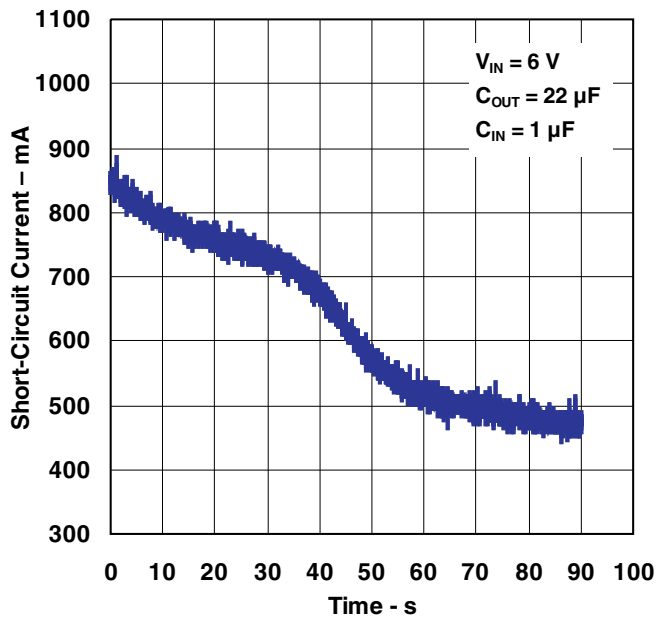
DELAY SWITCHING THRESHOLD
vs
JUNCTION TEMPERATURE



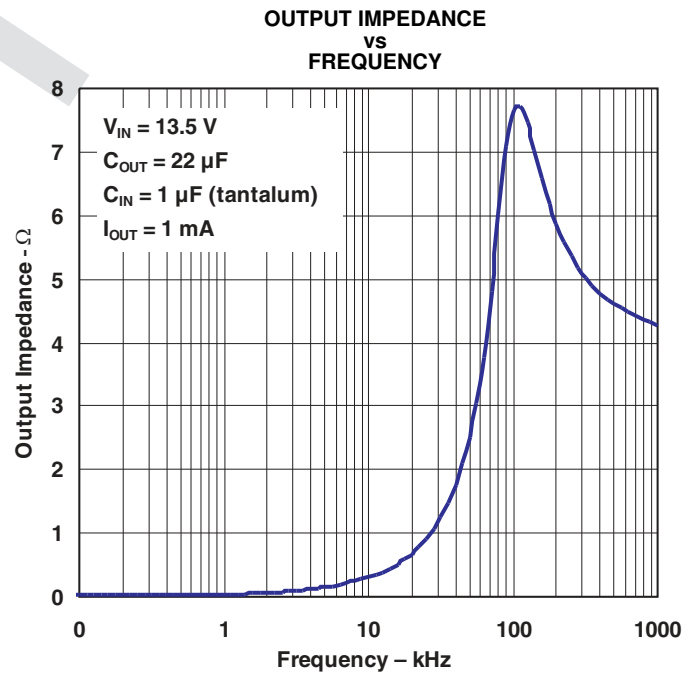
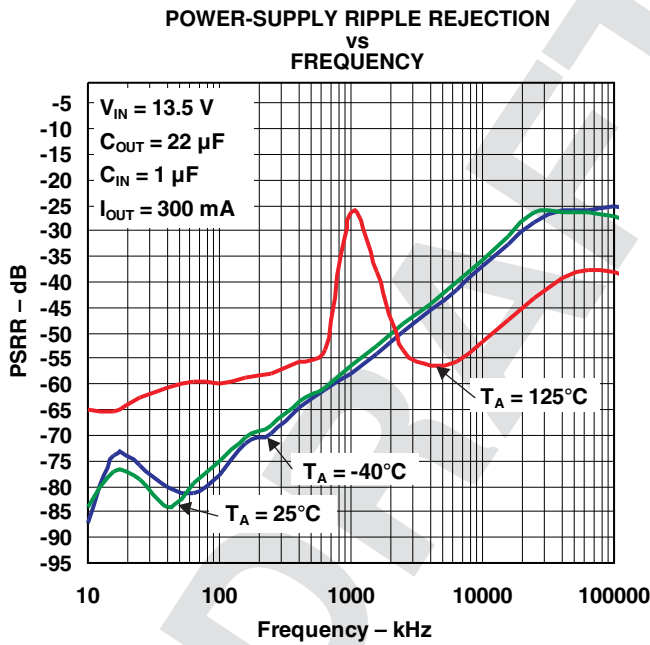
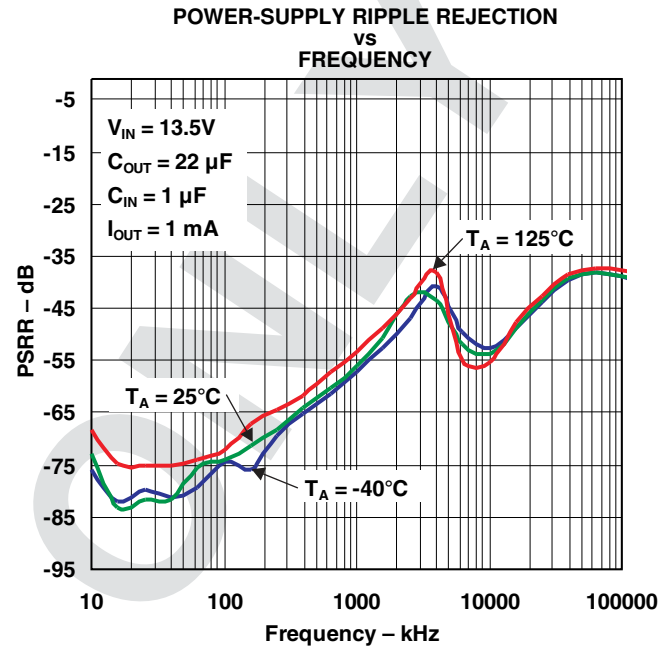
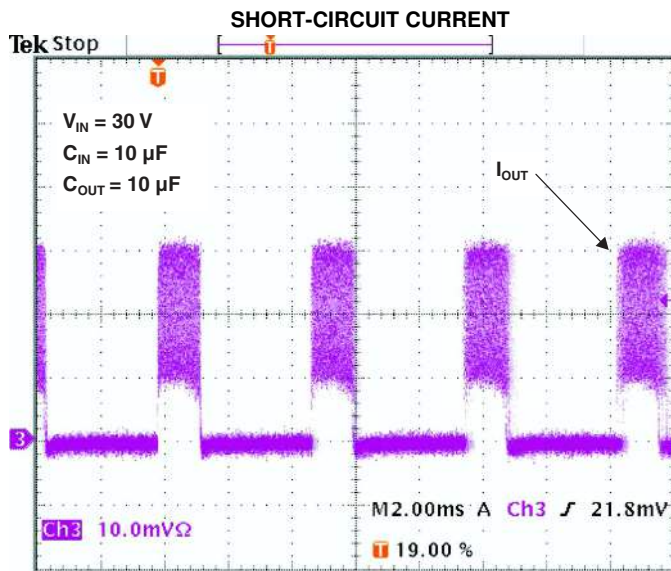
SHORT-CIRCUIT CURRENT
vs
SUPPLY VOLTAGE



SHORT-CIRCUIT CURRENT
vs
TIME

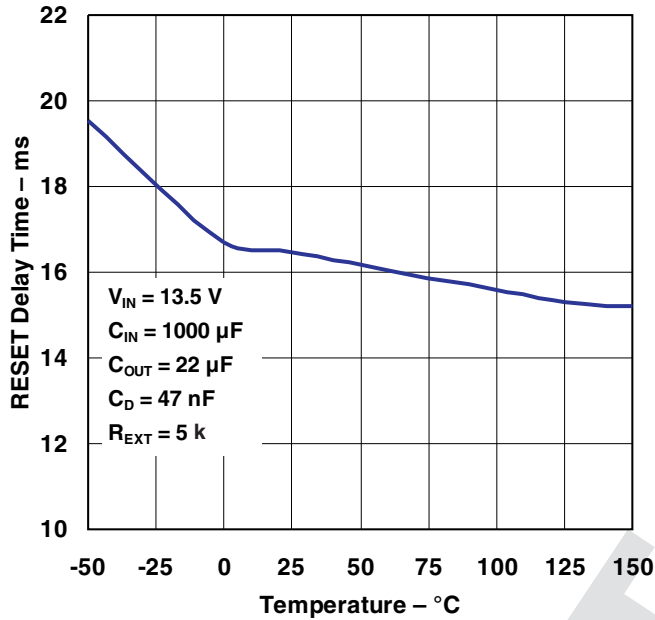


TYPICAL CHARACTERISTICS (continued)

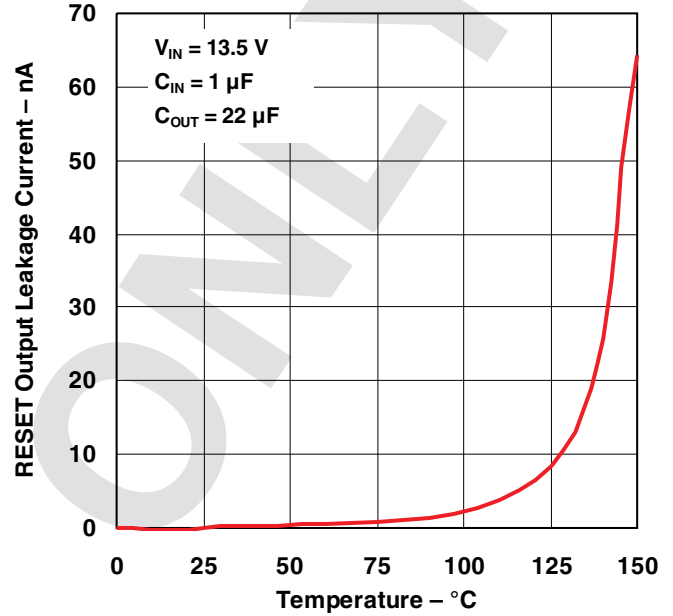


TYPICAL CHARACTERISTICS (continued)

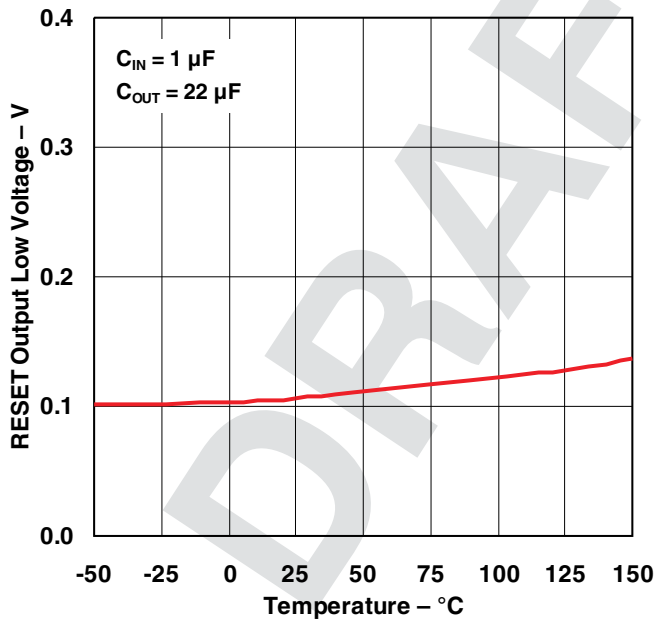
RESET DELAY TIME
vs
TEMPERATURE



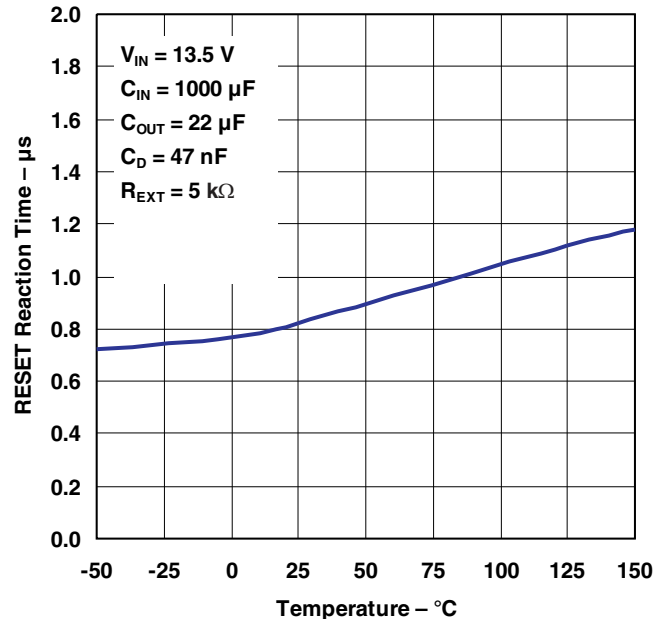
RESET OUTPUT LEAKAGE CURRENT
vs
TEMPERATURE



RESET OUTPUT LOW VOLTAGE
vs
TEMPERATURE

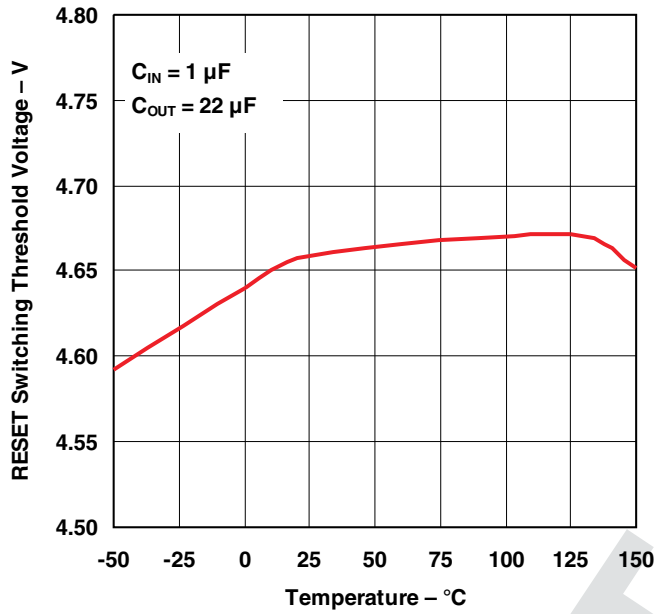


RESET REACTION TIME
vs
TEMPERATURE

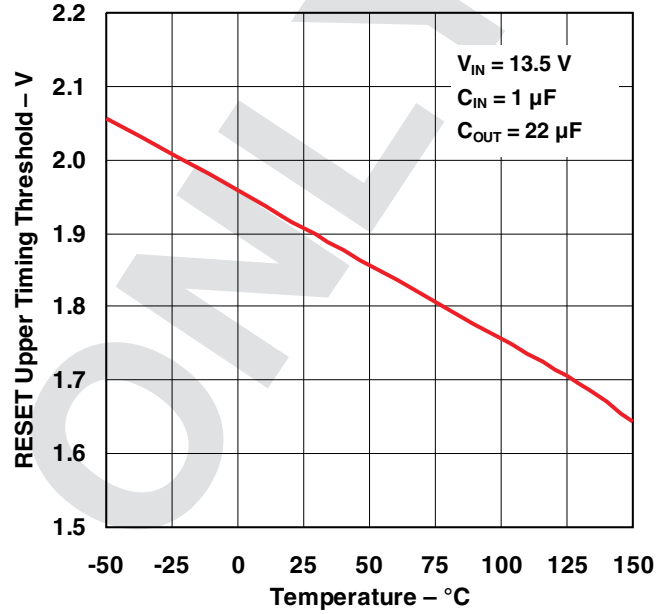


TYPICAL CHARACTERISTICS (continued)

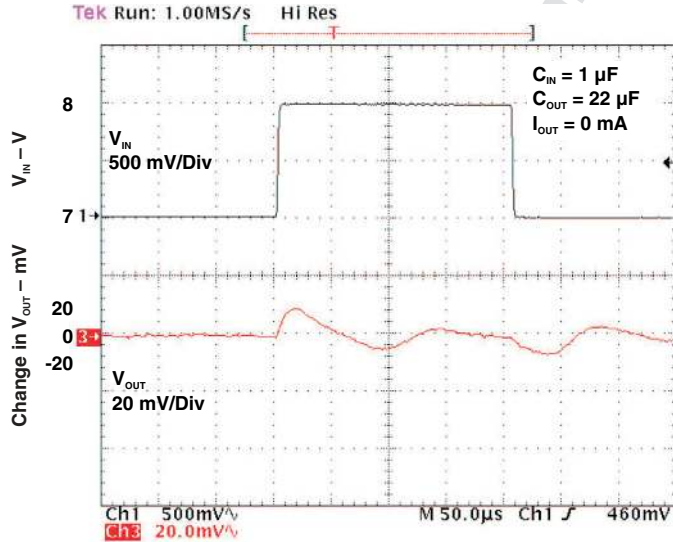
RESET SWITCHING THRESHOLD VOLTAGE vs TEMPERATURE



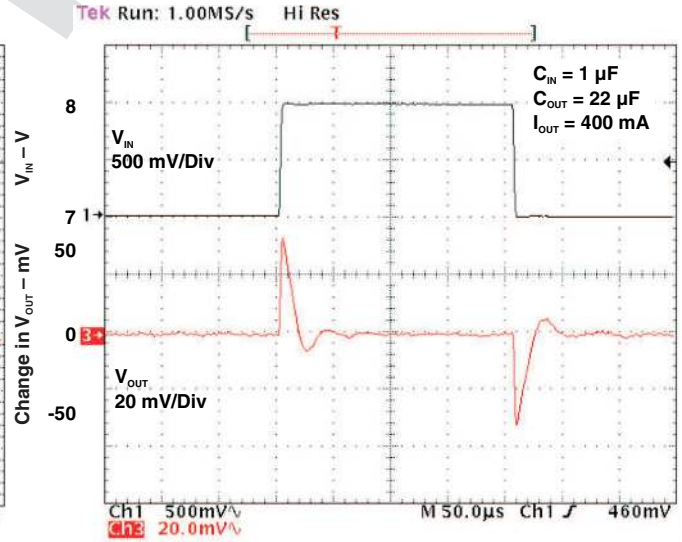
RESET UPPER TIMING THRESHOLD vs TEMPERATURE



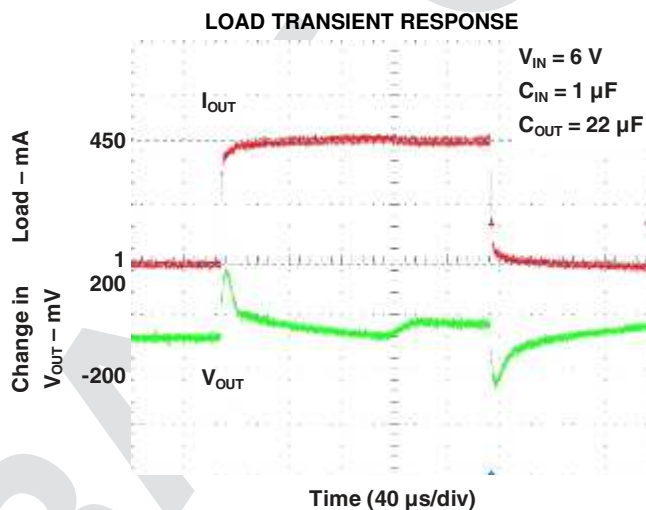
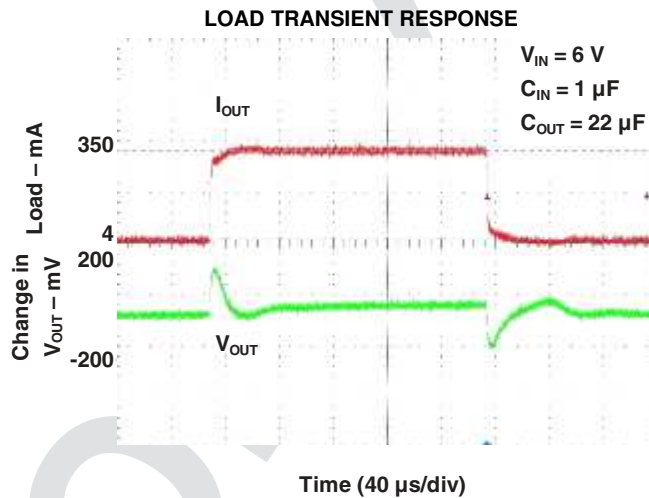
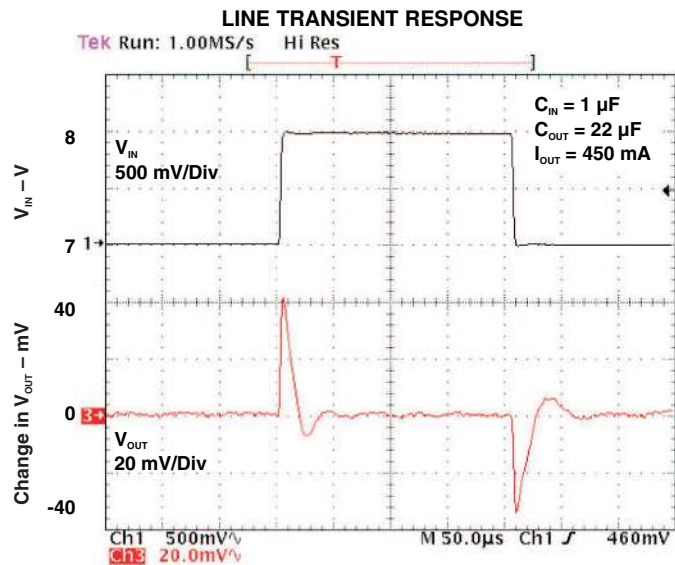
LINE TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE

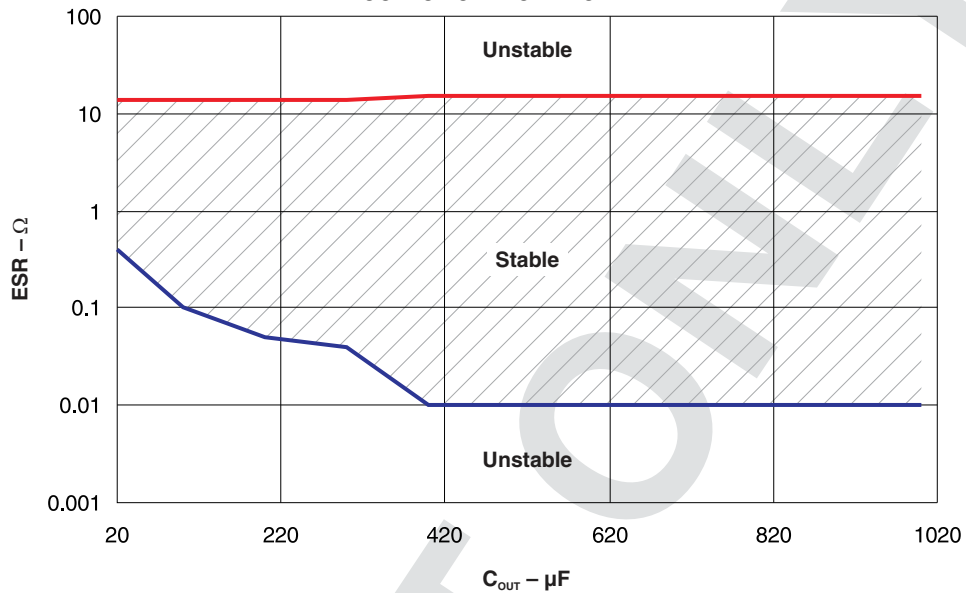


TYPICAL CHARACTERISTICS (continued)

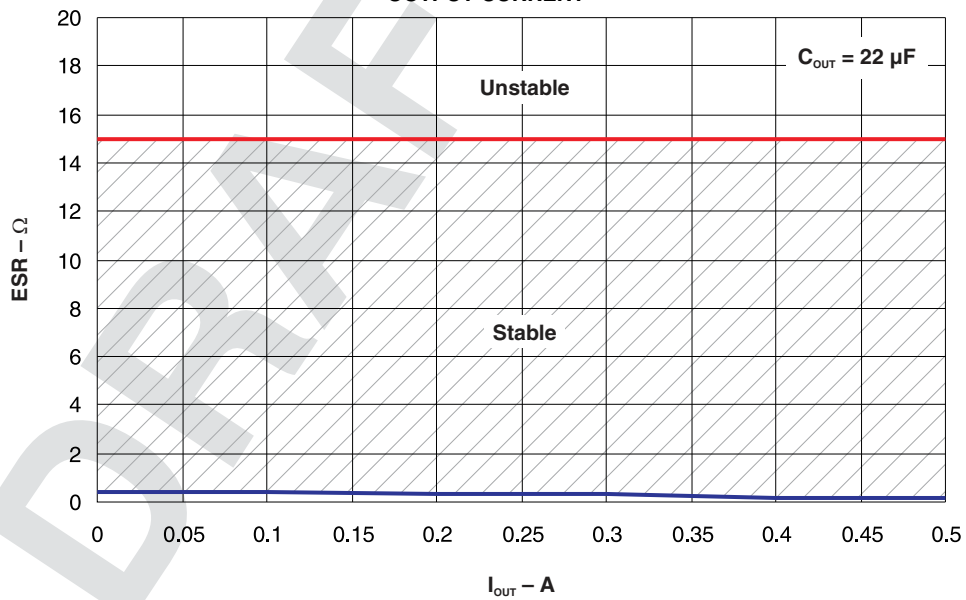


TYPICAL CHARACTERISTICS (continued)

REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
OUTPUT CAPACITANCE



REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE
vs
OUTPUT CURRENT



PARAMETER MEASUREMENT INFORMATION

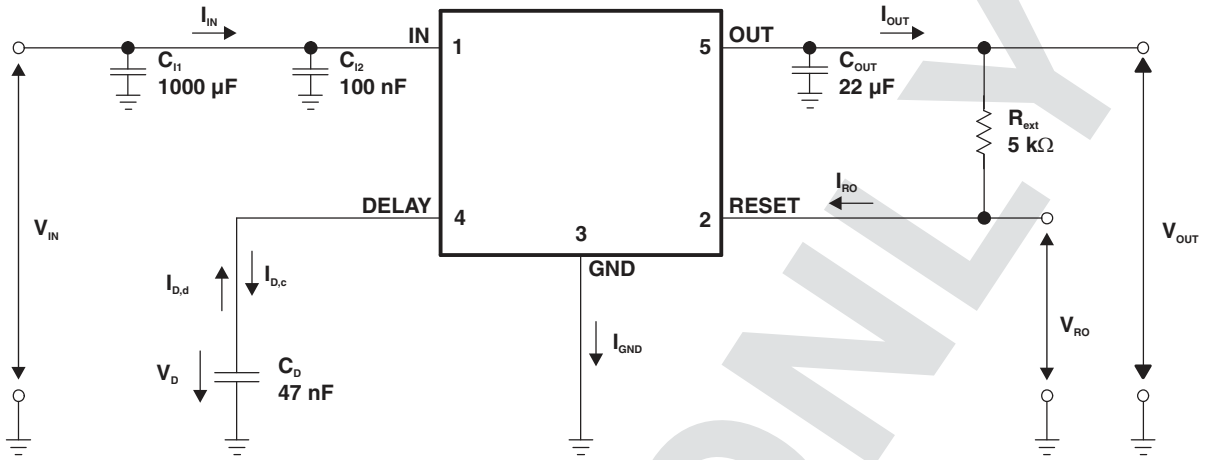


Figure 1. Test Circuit

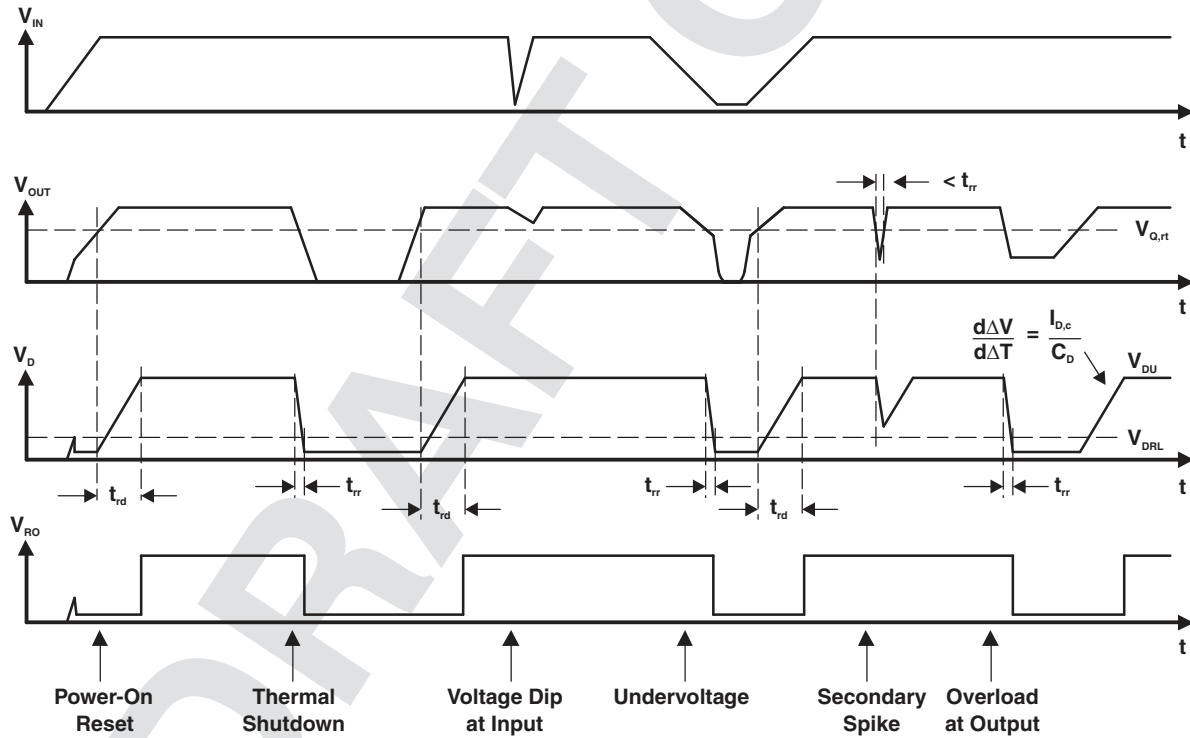


Figure 2. Reset Timing

APPLICATION INFORMATION

The TPS78405 is a monolithic integrated low-dropout voltage regulator in 5-pin KTT package. An input voltage up to 45 V is regulated down to 5 V. The output can drive load up to 450 mA and is short-circuit protected. In addition to short-circuit protection, the TPS78405 incorporates over-temperature and input-reverse protection. Figure 3 is typical application.

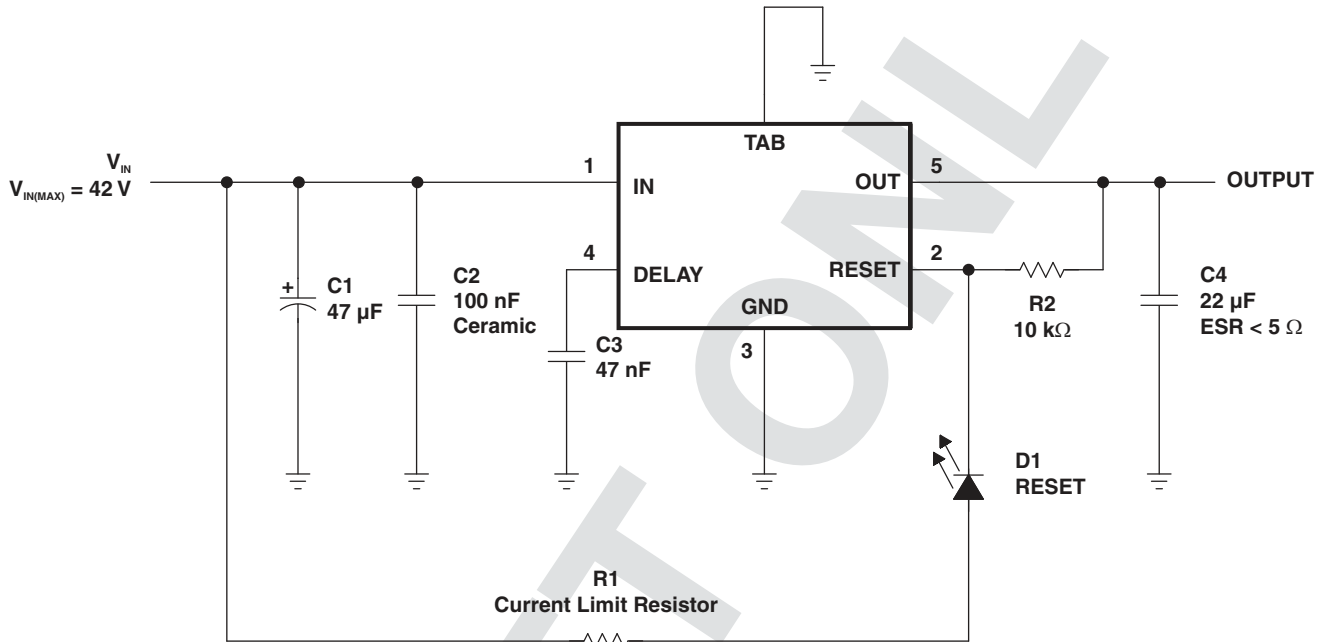


Figure 3. High Input Voltage, 450 mA, LDO Voltage Regulator

Output Capacitance

The TPS78405 regulator is designed to be stable with wide range of output capacitors. The ESR of the output capacitor affects stability. A minimum output capacitor of 22 µF with ESR < 5 Ω is recommended to prevent oscillations. A larger output capacitance value can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS78405, increase the effective output capacitor value.

Ceramic capacitors can be used by adding a small resistor in series (ESR) with the capacitor (see the Region of Stability graphs in *Typical Characteristics*).

Thermal Considerations

The power-handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of one component:

$$\text{Output current multiplied by the input/output voltage differential: } I_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}}).$$

The TPS78405 regulator has an internal thermal-limiting circuit to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient.