

SANYO Semiconductors **DATA SHEET**

An ON Semiconductor Company

LV5813TT — Step-down Switching Regulator

Overview

LV5813TT is 1ch step down switching regulator. 0.25Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current. Compact-package MSOP8 (150mil) employed. Current mode control type, with superior load current response and easy phase compensation. ON/OFF pin, allowing the standby mode with the current drain of 90μ A or less. Pulse-by-pulse over-current protection and overheat protection available for protection of load devices. Soft start pin to be provided with a capacitance for soft start.

Functions

• 1.5A 1ch step-down switching regulator

• Wide input dynamic range (4.75V to 18V)

• High efficiency : 90% ($V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 1A$)

• Compact package : MSOP8 (150mil)

• Standby mode

• Over-current protection

• Thermal shutdown

• Fixed frequency: 370kHz

• Soft start

• Reference voltage: 0.8V

Applications

• LCD TV

• Blu-ray Disc Player/Recorder

• Pre regulator

- PDP TV
- For χDSL power supply
- Amusement

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Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input V _{IN} voltage	V _{IN} max		20	V
BOOT pin maximum voltage	V _{BT} max		25	V
SW pin maximum voltage	V _{SW} max		V _{IN} max	V
BOOT pin-SW pin maximum voltage	V _{BS-SW} max		7	V
EN pin maximum voltage	V _{EN} max	*1	V _{IN} +0.3	V
FB, COMP, SS pin maximum voltage	Vfs max		7	V
Allowable power dissipation	Pd max	With specified substrate *2	0.85	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-40 to +150	°C

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V _{IN} pin voltage	V _{IN}		4.75 to 18	V
BOOT pin voltage	V _{BT}		-0.3 to 23	V
SW pin voltage	V _{SW}		-0.4 to V _{IN}	V
BOOT pin-SW pin maximum voltage	V _{BS-SW}		6.5	V
EN pin maximum voltage	V _{EN}		V _{IN} + 0.3	V
FB, COMP, SS pin voltage	V _{FSO}		6	٧

Electrical Characteristics at Ta = 25°C, $V_{IN} = 12$ V, unless otherwise specified.

ъ .	Symbol Conditions		Ratings			
Parameter		Conditions	min	typ	max	Unit
IC current drain at standby	I _{CC} 1	EN = 0V		90		μА
IC current drain in operation	I _{CC} 2	EN = 5V, FB = 1V		2		mA
Efficiency	Effcy	V _{IN} = 12V, I _{OUT} = 1A, V _O = 5V, Design target *3		90		%
Reference voltage	Vref	V _{IN} = 4.75V to 18V	-2%	0.8	+2%	V
FB pin bias current	Iref	FB = 0.8V		20	200	nA
High-side ON resistance	RonH	BOOT = 5V		0.25		Ω
Oscillation frequency	Fosc		296	370	444	kHz
Oscillation frequency during short-circuit protection	Foscs		85	115	145	kHz
EN high-threshold voltage	Venh		0.9	1.8	2.7	V
EN low-threshold voltage	Venl		0.7	1.35	2.0	V
Maximum ON DUTY	D max			85		%
Current limit peak value 1	lcl1	V _{IN} = 12V, V _{OUT} = 1.2V, L = 10μH	3.1		5.7	Α
Current limit peak value 2	lcl2	V _{IN} = 12V, V _{OUT} = 3.3V, L = 10μH	2.8		5.4	Α
Current limit peak value 3	lcl3	V _{IN} = 12V, V _{OUT} = 5V, L = 10μH	2.5		5.1	Α
Thermal shutdown temperature	Ttsd	Design guarantee *4		160		°C
Thermal shutdown temperature hysteresis	Dtsd	Design guarantee *4		40		°C
Soft start current	ISS	SS = 0V	3	5	7	μΑ

^{*3 :} Reference value (not tested before shipment)

 $^{*1:} V_{IN} + 0.3 < V_{IN} max$

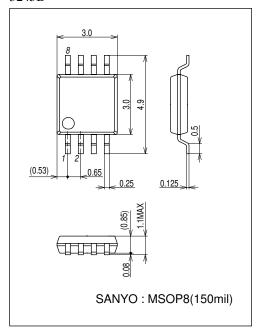
^{*2 :} Specified substrate : $46.4 \text{mm} \times 31.8 \text{mm} \times 1.7 \text{mm}$, glass epoxy substrate

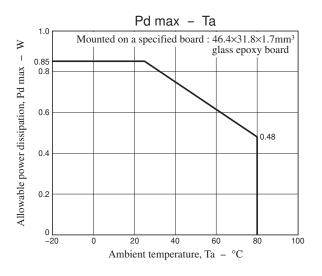
^{*4 :} Design guarantee (value guaranteed by design and not tested before shipment)

Package Dimensions

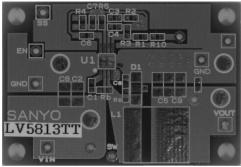
unit: mm (typ)

3245B

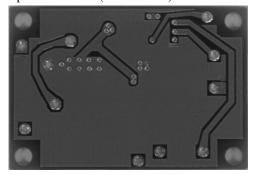




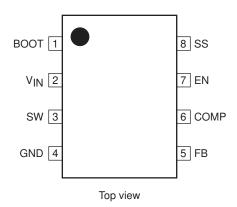
Specified Board (Top side)



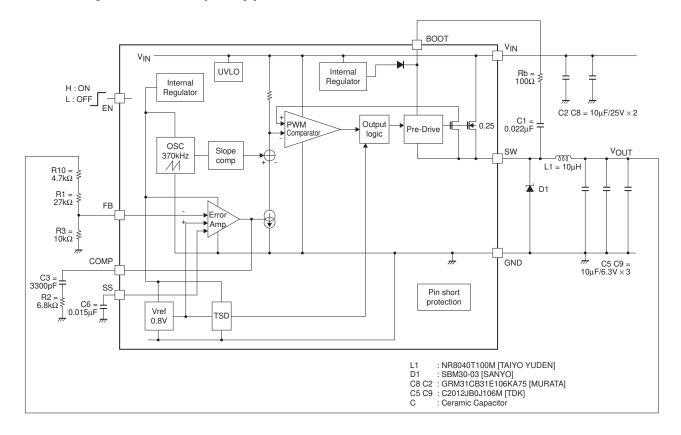
Specified Board (Bottom side)



Pin Assignment



Block Diagram and Sample Application Circuit (3.3V output)



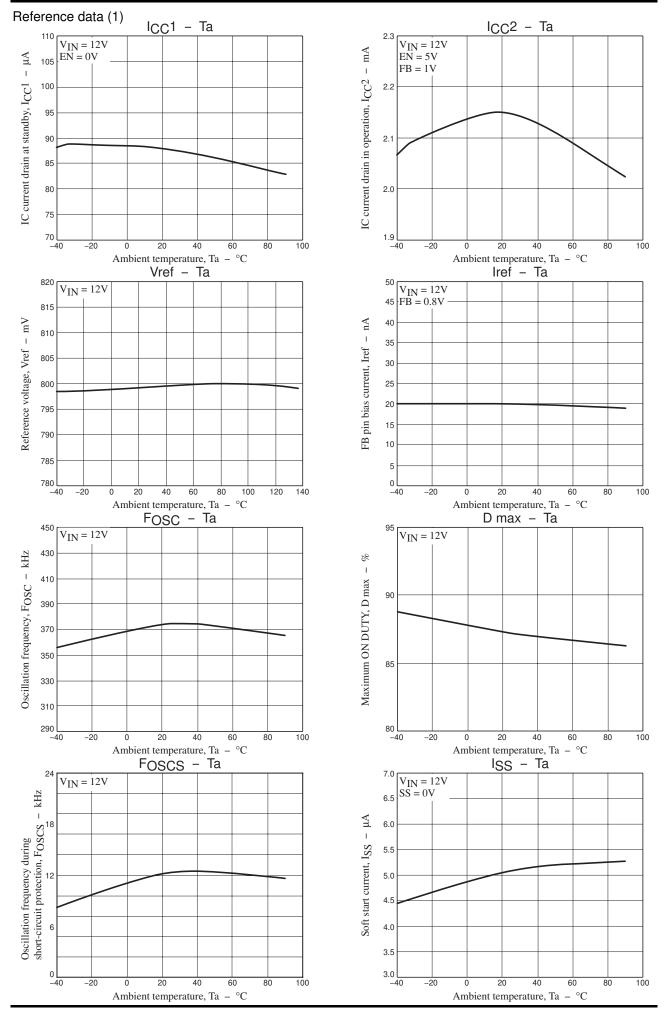
Pin Function

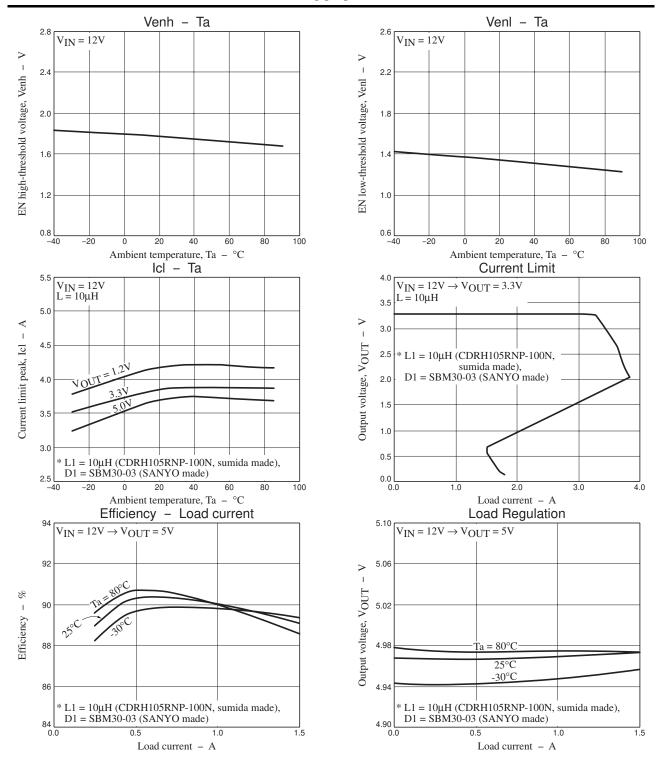
Pin No.	Pin name	Description	Equivalent Circuit
1	ВООТ	Upper MOS transistor boot strap capacitance connection pin Connect the boot capacitance of about $0.022\mu F$ between SW pins To protect the SW pin's absolute maximum rating, to ensure stable operation, and to eliminate noise, the boot capacitance serial resistance (about 100Ω) Rb proves effective.	Short protection circuit BOOT Output MOS SW
2	VIN	Input voltage pin. Connect substantially large (10µF 2 parameters or more) capacitance between this pin and GND.	See BOOT
3	SW	Power switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin.	See BOOT
4	GND	Ground pin.	

Continued on next page.

LV5813TT

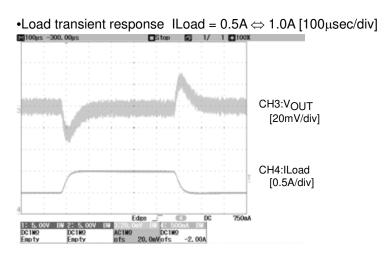
Pin No.	rom preceding pag Pin name	Description	Equivalent Circuit
5	FB	Feedback pin Sets the output voltage by means of split resistor in the section of the output voltage V_{OUT} - FB - GND. V_{OUT} setting is made as calculated below: $V_{OUT} = Vref \times \{1 + \frac{(R1 + R10)}{R3}\}$ $Vref = 0.8V$ Example: 3.3V output voltage (See block diagram and sample application circuit) $V_{OUT} = 0.8 \times \{1 + \frac{(27k + 4.3k)}{10k}\}$ $= 3.304V$	VIN Internal regulation sline SSS WREF 0.8V
6	COMP	Phase compensation pin Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	Short protection circuit COMP
7	EN	Enable pin Converter enabled when set to the HIGH voltage and disabled when connected to GND.	V _{IN}
8	SS	Soft start pin Set the soft start time by means of the built-in $5\mu A$ source voltage and external soft start capacity Css can be set as follows : $C6 = 5\mu A \times \frac{Tss}{Vref}$ Where, Tss is soft start time and Vref is the reference voltage. Example : 2.4ms soft start time achieved $Css = 5\mu A \times \frac{2.4 \text{ms}}{0.8 V} = 0.015 \mu F$	



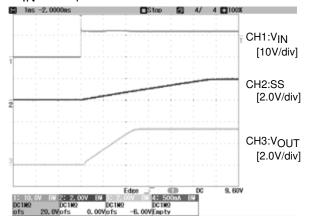


Reference data (2)

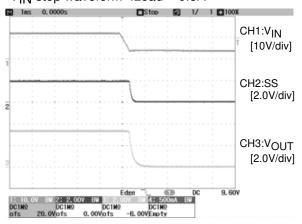
(* measurement circuit is shown in "8. Sample Application circuit", $V_{IN} = 12V \Rightarrow V_{OUT} = 3.3V$)

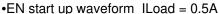


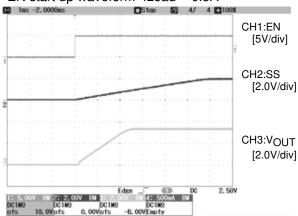




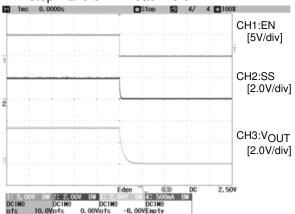
•V_{IN} stop waveform ILoad = 0.5A







•EN stop waveform ILoad = 0.5A



Considerations for the design

- During use with V_{IN} = 12V or less, the boot strap voltage may become deficient due to intermittent operation at no load, resulting in failure of normal operation. In this case, insert a resistance of about 500 Ω between V_{OUT} and GND and avoid the intermittent operation mode during use.
- Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. In such an event, do not insert beads as above described and, instead, remove noise by means of the BOOT resistance Rb.

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