IS32LT3180

DUAL INTENSITY, LINEAR CURRENT DRIVER FOR RCL

August 2022

GENERAL DESCRIPTION

The IS32LT3180 is an eight channel linear current regulator for automotive rear tail light applications such as RCL (Rear Combination Lamps) and CHMSL (Center High Mounted Stop Lamps). It is fully programmable with two LED brightness levels for the different intensity requirements of “stop” bright (DC mode) and “tail” dim (PWM mode).

A logic level at the PWM pin is used to select between the tail and stop output conditions. The stop condition provides the highest intensity output, while the tail condition utilizes an internally generated PWM signal to reduce the intensity of the LEDs’ light output.

The sink current at the OUTx pins is easily set with a single resistor at the STOP pin. A second resistor at the TAIL pin sets the duty cycle of the internal PWM oscillator for dimming (less bright) the LED output when operating in the tail condition.

An external FET controller is provided to maintain a constant headroom and power dissipation for the LED driver under wide varying supply voltages. For proper operation without Fault trigger, the use of external FET is recommended.

The IS32LT3180 is offered in an eTSSOP-16 package.

FEATURES

- Output current programmable from 10mA to 75mA
- Tail duty cycle programmable from 1% to 95%
- Linear voltage regulator to minimize consumption in the device
- Low dropout voltage of 0.8V@35mA
- Slew rate control on each output for better EMI performance
- PWM logic level input selects between full brightness and PWM dimming levels
- FAULT reporting
- LED open/short circuit detection
- Input overvoltage protection
- STOP pin overcurrent protection
- Thermal rollback of output current
- Withstand 50V load dump
- AEC-Q100 qualification
- RoHS & Halogen-Free compliant (Pb-free) package

APPLICATIONS

- Rear Combinational Lamp (RCL)
- Center High Mount Stop Light (CHMSL)
- Daytime running lamp
- Fog lamps
- Turn signal

TYPICAL APPLICATION CIRCUIT

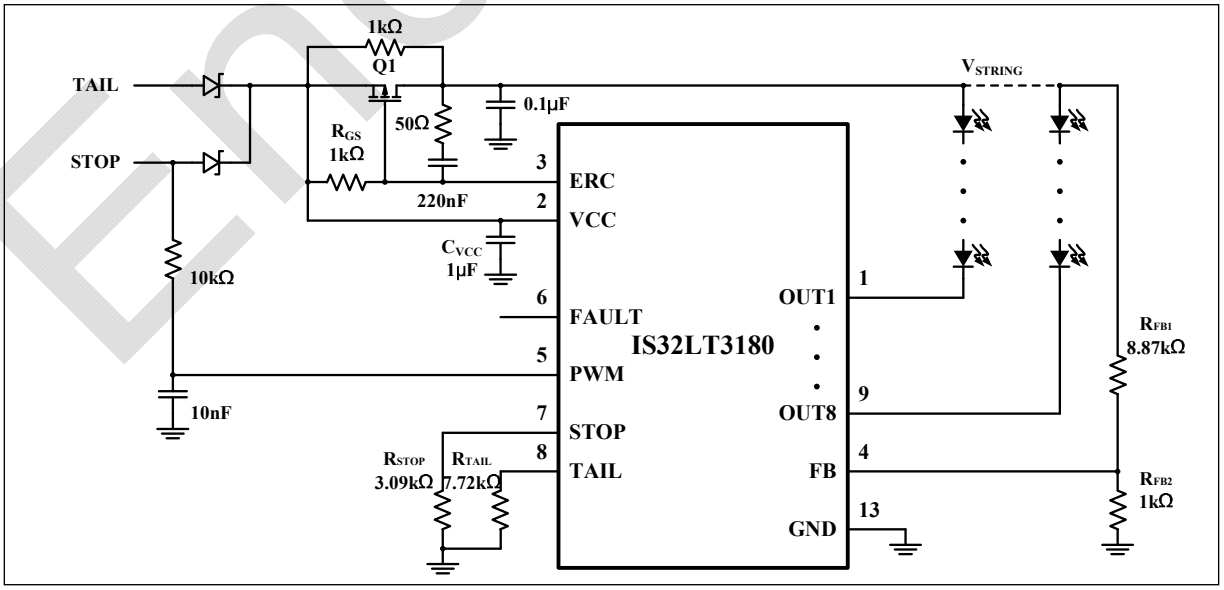
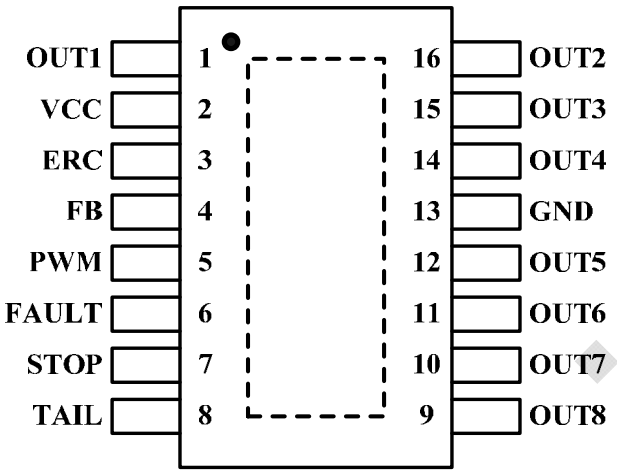


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top view)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	OUT1	Output current sink channel 1.
2	VCC	Power input for the IC.
3	ERC	External regulator control output. Connects to the gate of an external PMOS FET operated in linear mode.
4	FB	Reference input voltage for the external resistor divider (1.05V typical)
5	PWM	Digital logic input. Logic high to select full intensity (DC output current) and logic low (or floating) to select lower intensity (PWM output current).
6	FAULT	Open drain fault flag. High impedance status to indicate LED open/short, STOP pin over current, over voltage, thermal rolloff conditions.
7	STOP	Output current sink level setting pin.
8	TAIL	PWM duty cycle programming pin.
9~12	OUT8 ~OUT5	Output current sink channel 8~5.
13	GND	Ground connection for the IC.
14~16	OUT4 ~ OUT2	Output current sink channel 4~2.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Automotive Range: -40°C To +125°C

Order Part No.	Package	QTY/Reel
IS32LT3180-ZLA3-TR	eTSSOP-16, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

VCC, ERC, PWM, FAULT, OUTx, FB	-0.3 to 50V
TAIL, STOP	-0.3 to 5.5V
OUTx current	100mA
Operating junction temperature, T_J	150°C
Storage temperature range, T_{STG}	-55°C ~ +150°C
Operating ambient temperature range, $T_J = T_A$	-40°C ~ +150°C
Package thermal resistance (Junction to ambient), θ_{JA}	39.9°C/W
Power dissipation, $P_{D(MAX)}$ (Note 2)	2.5W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: Detail information please refers to package thermal de-rating curve on Page 12.

ELECTRICAL CHARACTERISTICS

T_J = -40°C ~+150°C, V_{CC} = 6V~16V, R_{STOP} =3.09kΩ, R_{TAIL} =7.72kΩ. (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{CC}	Input current	I_{OUTx} =35mA, V_{CC} =16V, 8 channels T_J = -40°C ~+125°C		6.0	8.0	mA
		T_J = +150°C (Note 5)		4.5		
I_{OUT_MAX}	Maximum sink current	T_J = -40°C ~+125°C, V_{OUTx} =1.2V	75			mA
		T_J = +150°C (Note 5, 6)		25		
I_{OUTACC}	Sink current accuracy	I_{OUTx} =35mA = (I_{OUT_MAX}+I_{OUT_MIN})/2 V_{OUTx} = 0.8V, T_J = -40°C ~+125°C (Note 4, 6)	-8	0	8	%
ΔI_{OUT}	Current matching	1-2×I_{OUT}/(I_{OUT_MAX}+I_{OUT_MIN}) I_{OUTx} =35mA, T_J = -40°C ~+125°C	-5	0	5	%
		T_J = +150°C (Note 5, 6)		±7		
I_L	Current leakage	V_{OUTx} =42V			1	μA
L_R	Line regulation	6V< V_{CC} <16V, 0.8V<V_{OUTx}<3V I_{OUTx} = 35mA, 8 channels T_J = -40°C ~+125°C (Note 6)		0.6	4	mA
V_{OVP}	Overvoltage setback threshold	@99%I_{OUTx} T_J = -40°C ~+125°C (Note 6)	16	18.7	23	V
I_{OSB}	Overvoltage setback current	V_{CC} =20V T_J = -40°C ~+125°C (Note 6)		95		%I_{OUT}
I_{FSB}	FAULT reporting of setback current	T_J = -40°C ~+125°C (Note 6)		80		%I_{OUT}
V_{OC}	Open LED detection threshold		0.3	0.4	0.5	V
V_{TH}	Output disable threshold			100	250	mV
V_{SCR}	Short LED detection threshold for reduced LED Current		3.2	3.6	4	V
R_{CS}	Current slew rate	I_{OUTx} = 35mA, 10%~90% T_J = -40°C ~+125°C (Note 5)		5	20	mA/μs
		T_J = +150°C (Note 5)		1		

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J = -40°C ~+150°C, V_{CC} = 6V~16V, R_{STOP} =3.09kΩ, R_{TAIL} =7.72kΩ. (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{RS}	Thermal rollback start temperature	I_{OUTx} >95% of maximum value (Note 5)		130		°C
T_{SD}	Thermal shutdown Threshold	I_{OUTx} has rolled off to 10% of maximum value (Note 5)	150	160		°C
T_{SD_HY}	Thermal hysteresis	(Note 5)		15		°C
I_{TFB}	FAULT reporting of thermal rollback	(Note 5)		50		%I_{OUT}
V_{FAULT}	FAULT pin voltage	Sink current = 5mA		0.1	0.2	V
I_{LF}	FAULT pin input leakage current	V_{FAULT} = 20V		0.1	1	μA
V_{PWM_H}	PWM high threshold			1.9	2.2	V
V_{PWM_L}	PWM minimum threshold		0.7	1.0		V
V_{FB}	FB regulation voltage		0.95	1.05	1.15	V
I_{ERC}	ERC drive current	V_{ERC} ≥ 3V	5	6		mA
V_{STOP}	STOP pin output voltage	T_J = -40°C ~+125°C (Note 4)	1.05	1.08	1.11	V
		T_J = +150°C (Note 5)		0.45		
	STOP pin current to I_{OUTx}	(Note 4)		100		A/A
V_{TAIL}	TAIL pin output current		90	100	110	μA
	PWM accuracy	Duty cycle set to 5%, V_{TAIL} = 0.6V T_J = -40°C ~+125°C (Note 6)	3.5	5	6.5	%
		Duty cycle set to 50%, V_{TAIL} = 2.4V T_J = -40°C ~+125°C (Note 6)	46	50	54	%
		Duty cycle set to 80%, V_{TAIL} = 3.6V T_J = -40°C ~+125°C (Note 6)	70	80	90	%
t_{ON}	Turn-on delay	V_{CC} =0V step to V_{CC} =12V, the delay between 0.9×V_{CC} with 0.9×I_{OUTx}		1	2	ms
t_{PWM}	PWM on delay	V_{CC} =12V V_{PWM} =12V step to V_{PWM} =0V		50	100	μs
f_{PWM}	PWM frequency	V_{PWM} = 0V		1		kHz

Note 3: All parts are production tested at T_J = -40°C ~ +150°C, unless otherwise noted. Other temperature limits are guaranteed by design.

Note 4: Accuracy of the STOP pin output voltage need not meet the specification so long as the output current accuracy specification over the full programmable current range can be guaranteed.

Note 5: Guaranteed by design.

Note 6: The output current please refers to Figure 9 at Page 7 when T_J is over 125°C.

TYPICAL PERFORMANCE CHARACTERISTICS

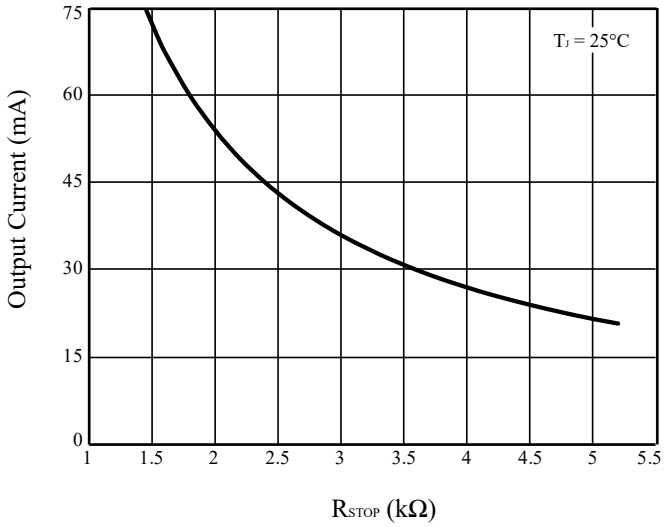


Figure 2 Output Current vs. R_{STOP}

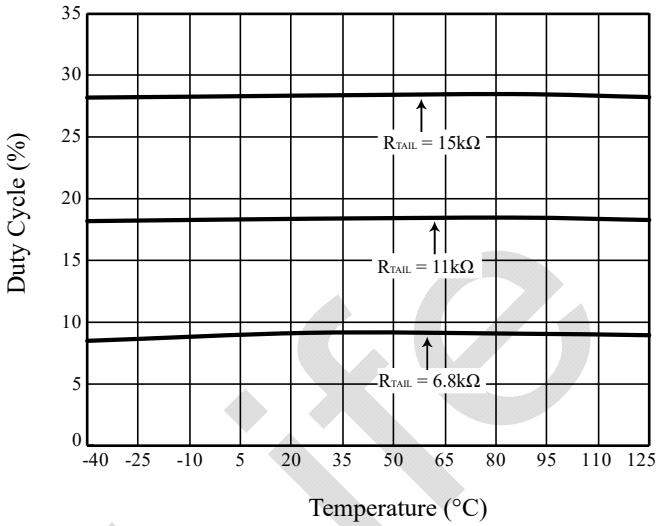


Figure 3 Duty Cycle vs. Temperature

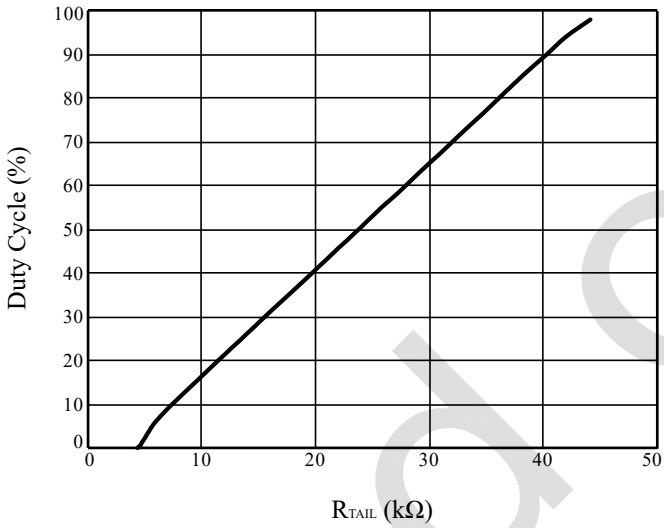


Figure 4 Duty Cycle vs. R_{TAIL}

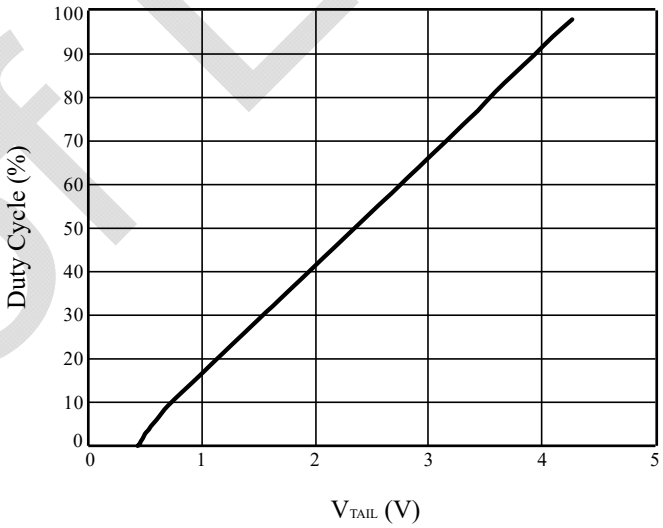


Figure 5 Duty Cycle vs. V_{TAIL}

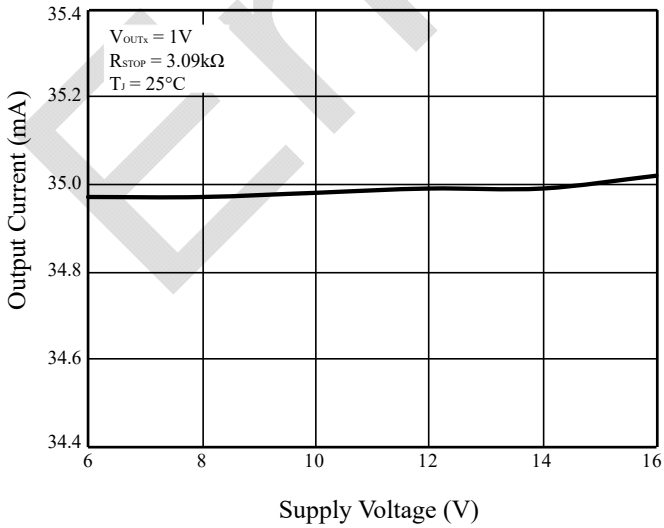


Figure 6 Line Regulation

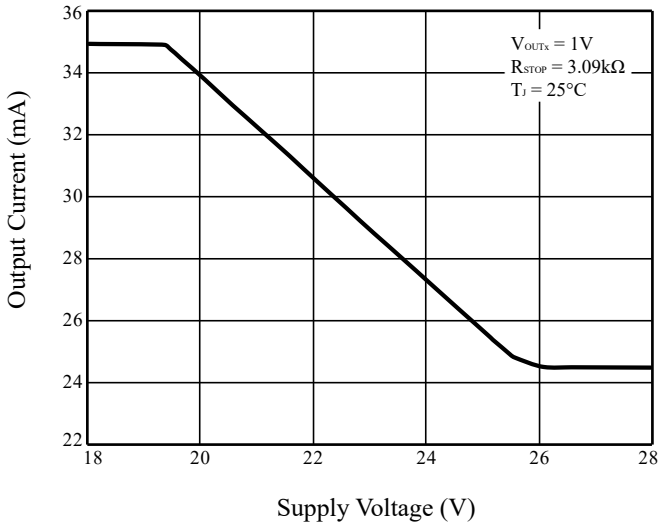


Figure 7 Input Overvoltage Protection

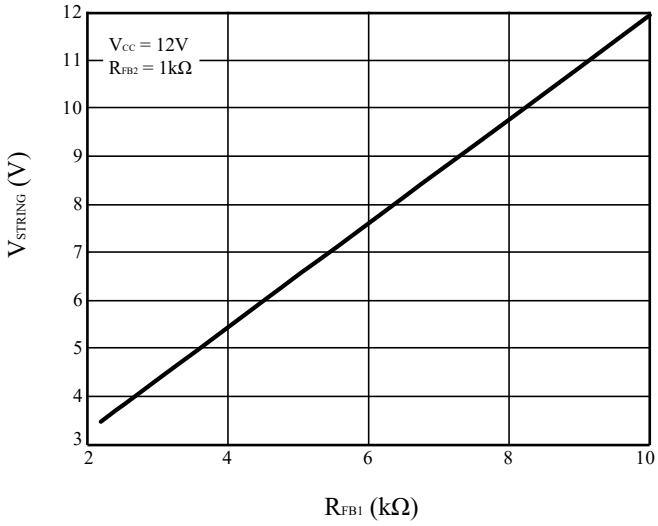


Figure 8 V_{STRING} vs. R_{FB1}

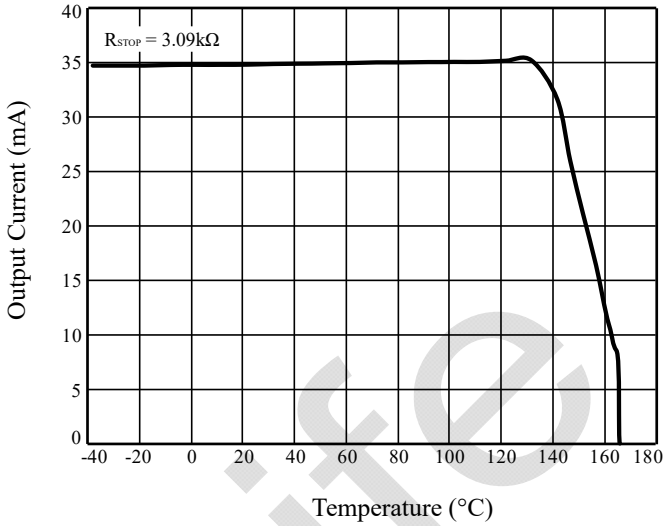


Figure 9 Output Current vs. Temperature

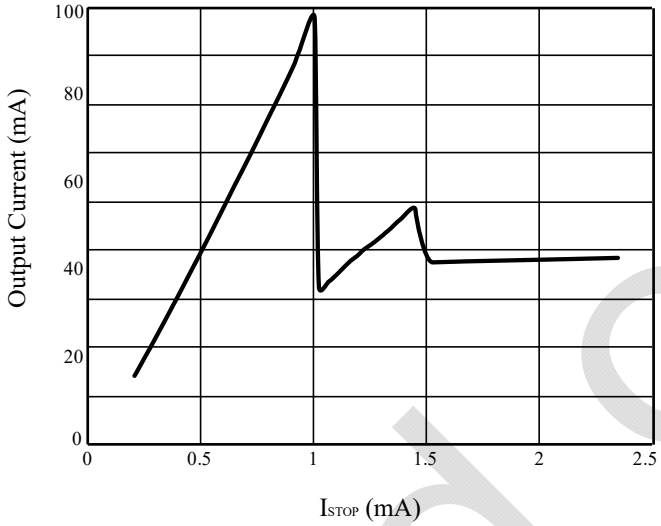


Figure 10 Output Current vs. I_{STOP}

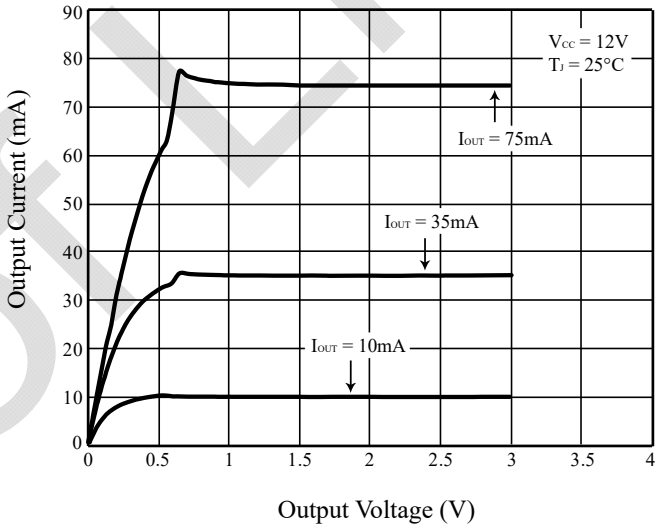


Figure 11 Output Current vs. Output Voltage

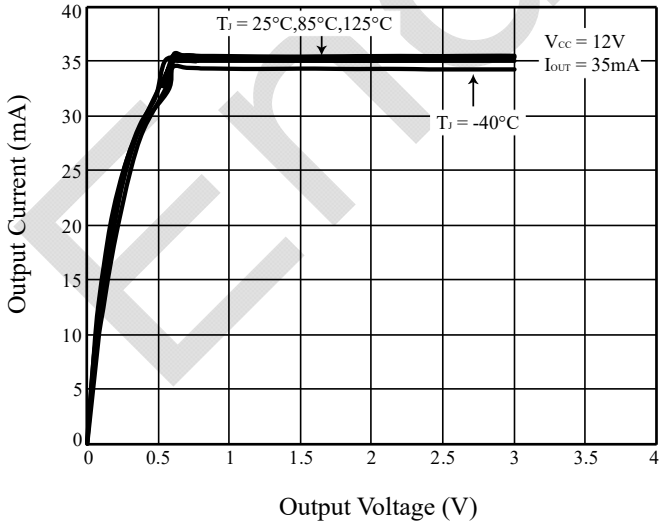
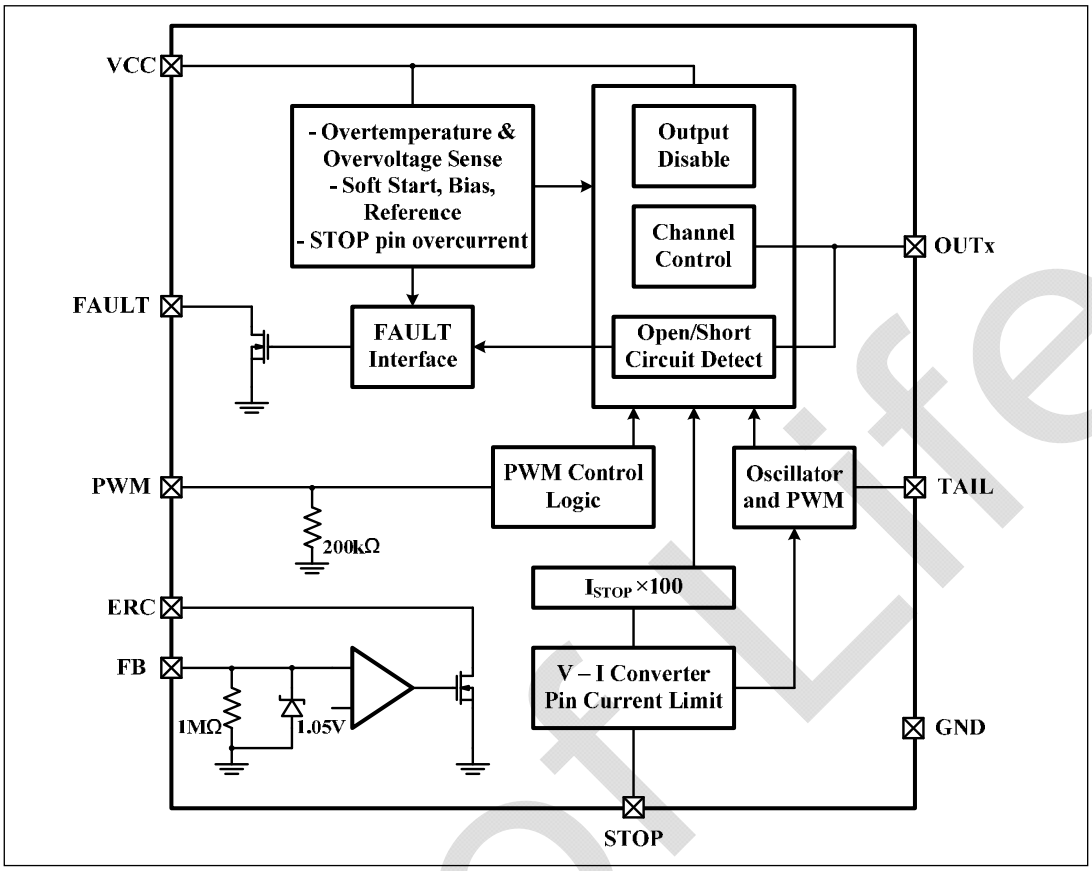


Figure 12 Output Current vs. Output Voltage

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3180 is an 8-channel linear current driver optimized to drive Rear Combination Lamp for automotive applications. A single input is used to select between two fully programmable intensity levels, one for the 'STOP' condition, and the other for the 'TAIL' condition. The full intensity 'STOP' condition is easily set using an external resistor, R_{STOP}. The lower intensity 'TAIL" condition is realized via a PWM of the output current, the duty cycle of which is easily programmed using an external resistor, R_{TAIL}.

IS32LT3180 also includes an integrated drive circuit for an external PMOS FET linear regulator for the case where the voltage across the LED loads must be accurately maintained to control power dissipation.

The ERC pin current (I_{ERC}) flows through 1kΩ resistor (R_{GS}) and generates a voltage across gate and source of PMOS FET. IS32LT3180 regulates this ERC current by sensing feedback reference voltage (V_{FB}) to controls the R_{DS_ON} of PMOS FET and get the expected V_{STRING}, which is set by resistor divider R_{FB1} and R_{FB2}.

The integrated feedback reference is trimmed to be 9% accuracy, while the ERC pin current (I_{ERC}) for the external regulator control can drive up to 6mA.

PROGRAMMING THE OUTPUT CURRENT

A single programming resistor (R_{STOP}) controls the maximum sink current for each LED channel. The STOP pin provides a reference voltage of 1.08V (Typ.). The programming resistor may be computed using the following Equation (1):

$$I_{OUT} = 100 \times \frac{1.08}{R_{STOP}} \qquad (1)$$

The current which is drawn from the STOP pin is internally mirrored to each of the 8 outputs with a multiplication factor of 100A/A. Thus, an output current of 50mA would require a current to be drawn from STOP of 500μA, corresponding to an external programming resistance of 2.16kΩ.

OVER CURRENT PROTECTION

A 1mA current limiting on STOP pin limits the current which can be referenced from the STOP pin. Exceeding the STOP current limit will reduce the output current. This helps limit output current (brightness and power) for this fault. The current rolls off per the diagram (Figure 10) to prevent unexpected excessive power dissipation. When the current of STOP pin reaches 1mA, the FAULT pin will assert.

PROGRAMMING THE PWM DUTY CYCLE

The PWM duty cycle which determines the lower intensity TAIL condition, is also easily programmed using a single external resistor. The PWM duty cycle (DC) is set by the following Equation (2):

$$DC = \left(\frac{100\mu A \times R_{TAIL}}{4V} - 0.1 \right) \times 100\% \qquad (2)$$

However, contrary to the STOP pin, and the TAIL pin supplies a constant current of 100μA. Internally, a sawtooth waveform with a peak value of 4.4V and a minimum value of 0.4V is compared to the voltage of the TAIL pin. The frequency of the sawtooth waveform is 1kHz resulting in a PWM signal of 1kHz at the programmed duty cycle. Thus, for example, a 50% duty cycle would require the reference voltage at TAIL to be 2.4V, corresponding to an external resistance value of 24kΩ.

The voltage comparison operation of the PWM duty cycle provides an alternative method of programming the duty cycle of the output current during a TAIL condition. Providing a DC input voltage to the TAIL pin from 0.4V to 4.4V programs the output duty cycle linearly from 0% to 100% duty cycle.

THERMAL ROLLBACK OF OUTPUT CURRENT

To protect the IC from damage due to high power dissipation, the temperature of the die is monitored. When the temperature of the die is below the thermal rollback start threshold of 130°C (Typ.), the output current maximum is the value set by the selection of R_{STOP}. When the die temperature is between the thermal rollback start threshold 130°C (Typ.) and the over temperature shutdown threshold 160°C (Typ.), the output current decreases linearly from the peak value to a target value of 10% of the maximum current occurring at the thermal shutdown temperature. During the rollback, the FAULT pin will assert this fault when the output current reaches 50%×I_{OUT}.

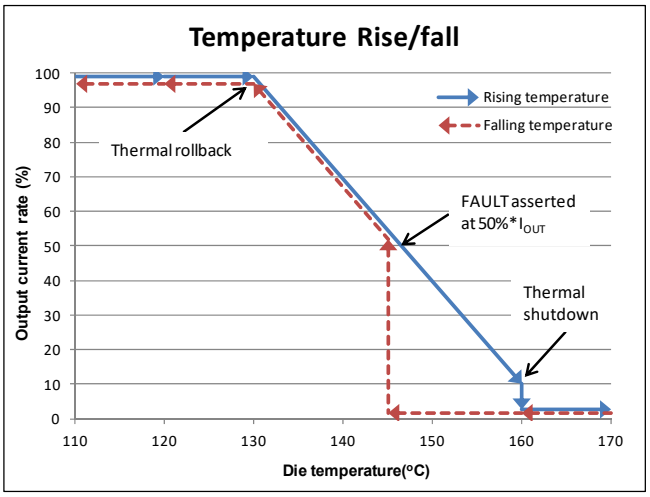


Figure 13 Temperature Rise/Fall

THERMAL SHUTDOWN

If the die temperature exceeds the thermal shutdown temperature of 160°C (Typ.) then the device is shutdown, and the sink current is shut off for all channels. After a thermal shutdown event, the die will not try to restart until the temperature of the die has reduced to less than 145°C (Typ.).

INPUT VOLTAGE OVER VOLTAGE DETECTION

Automotive battery systems have wide variations in line supply voltage; depending on battery charge status. Low dropout is a key attribute for providing consistent LED light output at low line voltage. Unlike adjustable regulator based constant current source schemes where the set point resistor resides in the load path, the IS32LT3180's set point resistor lies outside the LED load path, and aids in the low dropout capability.

Current limit is employed during high voltage. During a current limit event, the drive current is linearly reduced to 70%×I_{OUT} resulting in lower power dissipation on the IC. This occurs during high battery voltage (V_{CC} > 16V). In this way the IS32LT3180 can operate in extreme conditions and still provide a controlled level of light output. The overvoltage condition is asserted on the FAULT pin as the drive current reaches 80%×I_{OUT}. Reference Figure 14 and 15 for power limiting behavior.

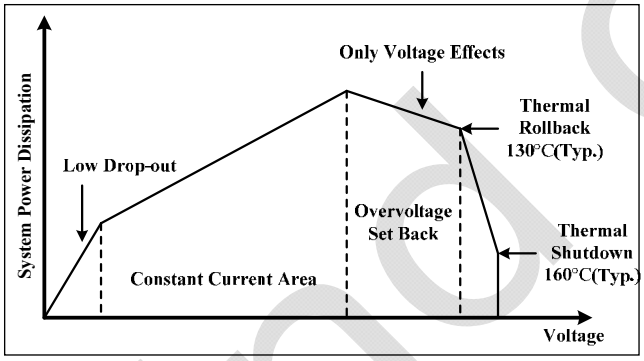


Figure 14 System Power

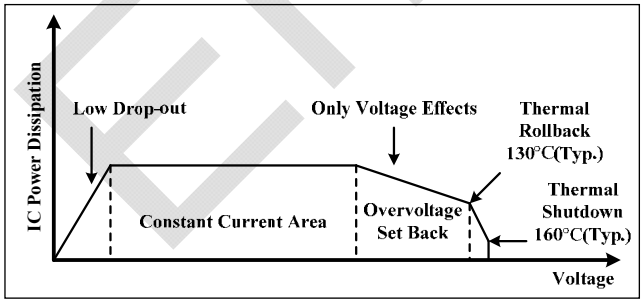


Figure 15 IC Power

OUTPUT CURRENT SLEW RATE CONTROL

To minimize the effects of EMI, the output current rise and fall time is controlled. The slew rate control circuitry is designed to control the rise time, 10% to 90% and fall time 90% to 10% at 5mA/μs (Typ.).

OPEN LED DETECTION

Each of the outputs of the IS32LT3180 is monitored for an output voltage of less than 400mV (Typ.). If any of the output voltages drops below the threshold voltage, the fault register is triggered and the FAULT pin is asserted.

During normal operation, it is possible that current may still be flowing in the output LED string even if the output voltage of the IC falls below the open LED detect threshold (V_{OC})– for example, if the LED string remains intact, but the supply voltage dips momentarily. In this case, the FAULT pin would assert then de-assert when the output voltage returns to the nominal value.

OUTPUT DISABLE DETECTION

As IS32LT3180 powers up, the device will check OUTx pin of each channel to see if it is connected to GND. If any channel is connected to GND (disable typical threshold is 100mV), the fault diagnostic function will ignore the fault of this channel. To prevent a trigger fault assertion, when less than 8 channels are used, the unused OUTx pins must be connected to GND to disable these channels.

SHORT LED DETECTION

If there is a condition where some or all of the LEDs on a channel become short circuited, the voltage on the channel output can reach the supply voltage, and therefore the power dissipation of that channel will arise due to V×I thermal dissipation. In this case, the device will automatically try to protect itself by quickly lowering the current of the channel(s), whose voltage on the channel output pin(s) rises above 3.6V, to 30%×I_{OUT}. The FAULT pin will assert. If the voltage returns to the lower region, the current in the output driver will return to the set value and FAULT pin de-asserts.

Note: to avoid the false short LED protection, the external PFET architecture is essential for the automotive application, due to its wide varying battery supply voltage.

Table 1 I_{OUT} and FAULT State at Different PWM

6V< V_{CC} <16V			
PWM Pin	**LED String**	**I_{OUT}**	**FAULT**
> 2.2V	Normal	$100\times\frac{1.08}{R_{STOP}}$	De-asserted
	Open	0A	Asserted
	Short	$100\times\frac{1.08}{R_{STOP}}\times 30\%$	Asserted
< 0.7V	Normal	$100\times\frac{1.08}{R_{STOP}}\times DC$	De-asserted
	Open	0A	Asserted
	Short	$100\times\frac{1.08}{R_{STOP}}\times 30\%\times DC$	Asserted

DC = Duty cycle of PWM as set by R_{TAIL}.

EXTERNAL REGULATOR CONTROL PIN

An external PMOS can be used to protect the IS32LT3180 from damage due to large voltage variation from the input voltage, or the LED string forward voltage. The external PMOS FET is used as a linear voltage regulator to help minimize the power dissipated in the OUTx channels.

The operation can be selected by connecting a resistive voltage divider to the FB pin (as shown in the Figure 1 typical operating schematic). This enables the ERC pin output to linearly drive the PMOS FET and regulate the V_{STRING} voltage so the FB voltage is maintained at 1.05V (Typ.).

FEEDBACK VOLTAGE SETTING

V_{STRING} should be set to a level to allow proper operation of the IC without detecting an open LED (0.5V max on OUTx) and to keep power to the IC at reduced levels below the 130°C (Typ.) thermal rollback temperature threshold limit. Reducing die temperature will depend on printed circuit board composition, PCB size, thermal via number and placement, module component placement, and air flow.

V_{STRING} can only be adjusted with an external PMOS FET and it is set using resistors R_{FB1} and R_{FB2} (refer to Figure 1) as following Equation (3):

$$V_{STRING}=V_{FB}\times\left(\frac{R_{FB1}}{R_{FB2}}+1\right) \qquad (3)$$

This simplifies to an equation for R_{FB1}.

$$R_{FB1}=\frac{R_{FB2}\left(V_{STRING}-V_{FB}\right)}{V_{FB}} \qquad (4)$$

And, $$V_{STRING}=V_{OUTx}+V_{LED} \qquad (5)$$

The recommended R_{FB2} is 1kΩ. V_{LED} is the total V_F. It should remain sufficient V_{OUTx} to insure the current sink operation. Please refer to Figure 11 and 12 to set a proper V_{OUTx}.

FAULT OUTPUT OPERATION

Any channel which encounters an open or short LED condition will be asserted by the FAULT pin. Typically this condition is encountered during a STOP or TAIL condition then the fault condition will be detected and the fault signal asserted. When the RCL is in neither STOP nor TAIL condition, the circuit is powered down, and thus the signal is cleared. Upon re-entering either the STOP or TAIL condition, the fault signal will reassert if the fault condition still exists, or, if the fault condition has been cleared, FAULT pin will not re-assert.

Exceeding the STOP pin current limiting 1mA will reduce the output current to 30mA and the FAULT pin will assert (refer to Figure 10).

In overvoltage detection, when the line supply voltage exceeds the overvoltage setback threshold (minimum is 16V), the drive current will be linearly decreased to 70%×I_{OUT}, which is proportional to supply voltage. The FAULT pin asserts as the drive current reach 80%×I_{OUT} and de-assert as return above 80%×I_{OUT}.

FAULT assertion due to the die temperature exceeding that of the thermal rollback start threshold is not latched. When the die temperature exceeds the thermal rollback threshold 130°C (Typ.) and output current linearly decreases to 50%×I_{OUT}, the FAULT signal will be asserted, and remain asserted until the output current returns above 50%×I_{OUT}, at which time, the FAULT pin will de-assert.

In all cases, if the device is powered down during the time when the FAULT signal is asserted, the FAULT pin is reset. Reapplying power to the circuit after this has occurred will cause the FAULT pin to operate as normal in accordance with the conditions described above.

Table 2 Fault Assertion

Fault Type	Asserted Condition	Output Driver Action	FAULT Pin	Fault Recovering
Open LED	Any of the OUTx pin voltages drops below than open LED voltage threshold 400mV (Typ.).	All channels keep on state.	High impedance status	The FAULTB pin pulls low when V_{OUTx} returns above the open LED detect threshold.
Short LED	The voltage on any channel OUTx pin rises above the short LED detect threshold 3.6V (Typ.).	The current of the channel(s), whose voltage on the channel output pin(s) rises above 3.6V, will be decreased to 30%×I_{OUT}.	High impedance status	The FAULTB pin pulls low when V_{OUTx} returns below the short LED detect threshold.
Short STOP pin	STOP pin current exceeds 1mA (Typ.).	The output current of all channels rolls off per the diagram (Figure 10).	High impedance status	The FAULTB pin pulls low when STOP pin current is lower than 1mA (Typ.).
Overvoltage VCC pin	VCC voltage exceeds overvoltage setback threshold 18.7V (Typ.).	The output current of all channels is linearly reduced to 70%×I_{OUT}.	High impedance status as the output current reaches 80%×I_{OUT}.	The FAULTB pin pulls low when the output current returns above 80%×I_{OUT}.
Thermal Rollback	The die temperature exceeds the thermal rollback threshold 130°C (Typ.).	The output current of all channels linearly decreases to 10%×I_{OUT} per the die temperature.	High impedance status as the output current reaches 50%×I_{OUT}.	The FAULTB pin pulls low when the output current returns above 50%×I_{OUT}.

THERMAL DISSIPATION

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3180, P_{3180}, and the package thermal resistance, θ_{JA}, as in Equation (6):

$$P_{3180} = V_{CC} \times I_{CC} + \sum_{x=1}^{8} V_{OUTx} \times I_{OUTx} \qquad (6)$$

and,

$$T_J = T_A + \Delta T = T_A + P_{3180} \times \theta_{JA} \qquad (7)$$

Where, V_{CC} is the supply voltage, V_{OUTx} is the voltage across OUTx pin to GND, I_{OUTx} is the sink current of each LED string and T_A is the ambient temperature.

When operating the device at high ambient temperatures, or when driving high load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (8):

$$P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \qquad (8)$$

So, $$P_{D(MAX)} = \frac{125°C - 25°C}{39.9°C/W} \approx 2.5W \qquad (9)$$

Figure 16, shows the power derating of the IS32LT3180 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

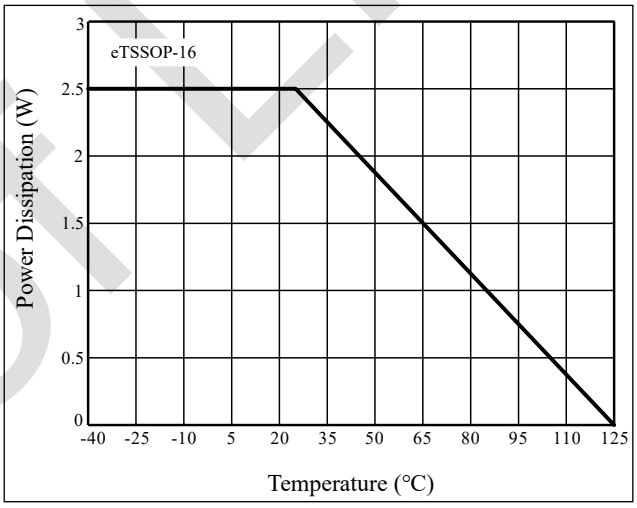


Figure 16 Dissipation Curve

With the linear voltage regulator, IS32LT3180 will regulate the PMOS FET to keep V_{STRING} voltage constant, that can be set by resistor divider R_{FB1} and R_{FB2}. So even though the supply voltage V_{CC} has some variation, the power dissipation on IS32LT3180 will be constant.

$$V_{OUTx} = V_{STRING} - V_{LEDSx} \qquad (10)$$

And, $$P_{3180} = V_{CC} \times I_{CC} + \sum_{x=1}^{8} V_{OUTx} \times I_{OUTx} \qquad (11)$$

Where, V_{LEDSx} is the total forward voltage of each LED string.

The power dissipation on the external PFET MOS can be calculated by the following Equation (12):

$$P_{FET} = \sum_{x=1}^{8} (V_{CC} - V_{STRING}) \times I_{OUTx} \qquad (12)$$

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a copper area of a few square millimeters on each side of the board directly under the IS32LT3180 (eTSSOP-16 package) and PMOS FET must be used. Multiple thermal vias, as shown in Figure 17, will help to conduct heat from the exposed pad of the IS32LT3180 and PMOS FET to the copper on each side of the board. The thermal resistance can be further reduced by using a metal substrate or by adding a heat sink.

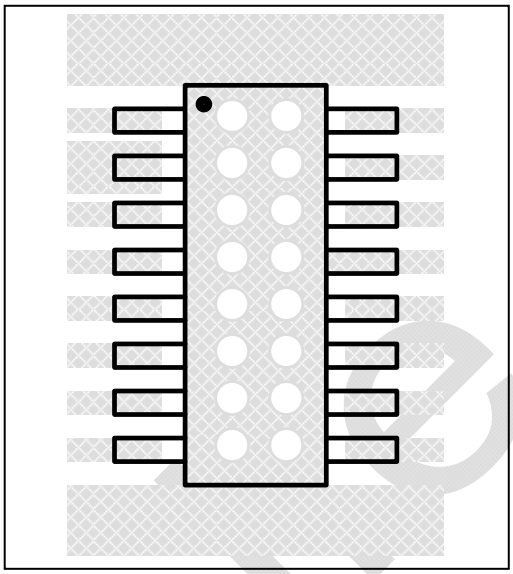


Figure 17 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

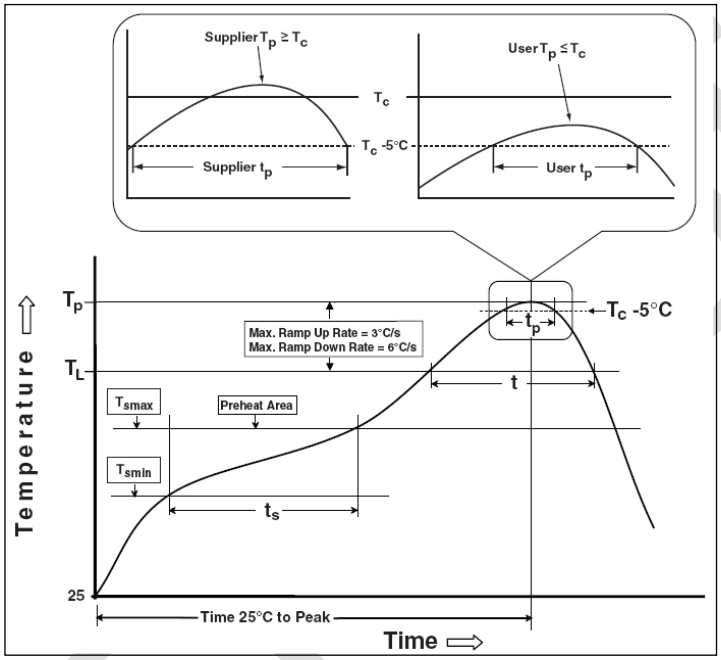
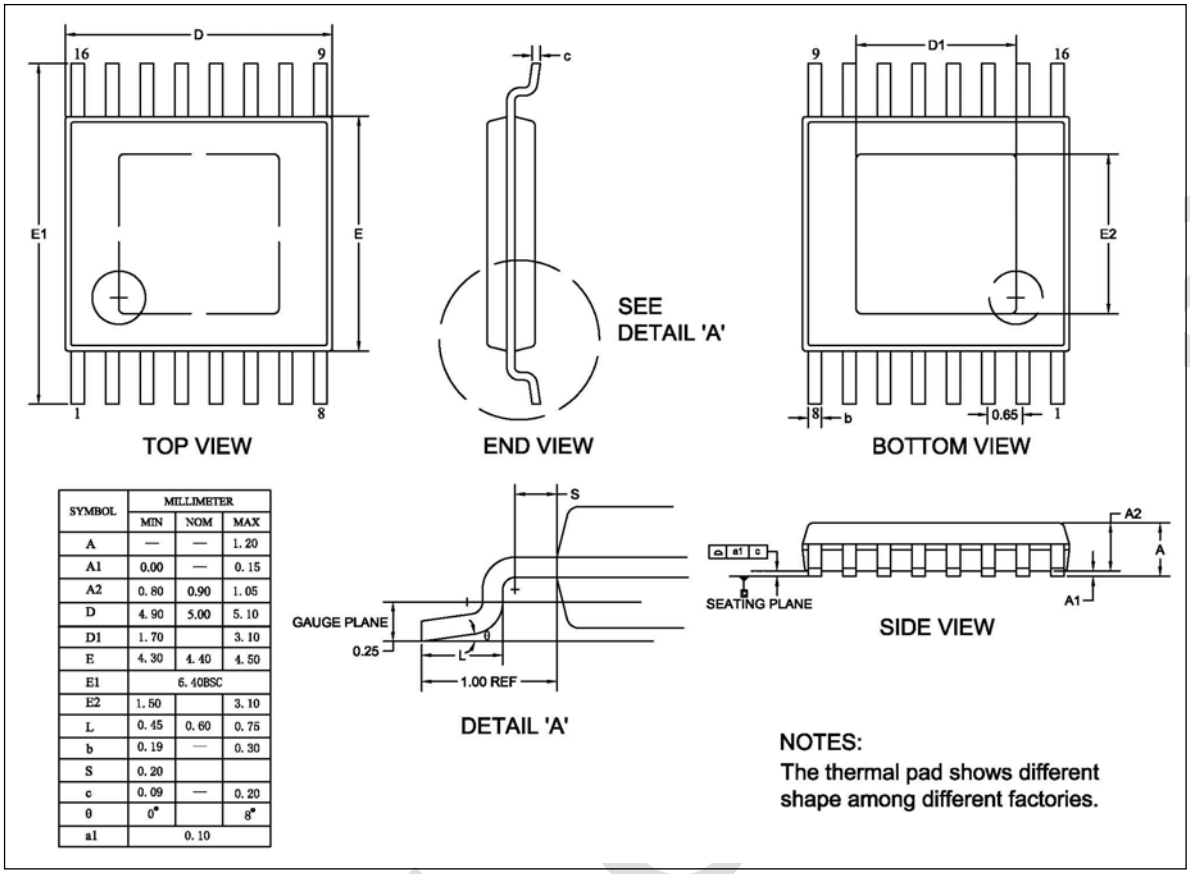


Figure 18 Classification Profile

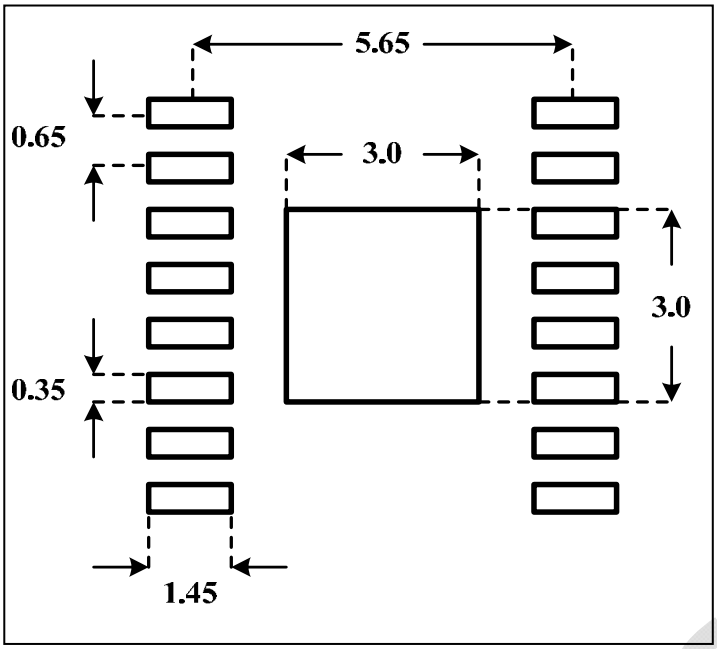
PACKAGE INFORMATION

eTSSOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70		3.10
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50		3.10
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2015.12.01
B	1. Remove Figure 2 2. Add a statement and note description	2016.01.01
C	Add NRND watermark	2022.06.14
D	Change watermark to EOL	2022.08.26