











SN74HC04-Q1

SCLS583B-MAY 2004-REVISED APRIL 2020

SN74HC04-Q1 Automotive Hex Inverters

Features

- AEC-Q100 Qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C, T_A
- **Buffered inputs**
- Positive and negative input clamp diodes
- Wide operating voltage range: 2 V to 6 V
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

Applications

- Synchronize inverted clock inputs
- Invert a digital signal

Description

This device contains six independent inverters. Each gate performs the Boolean function $Y = \overline{A}$ in positive logic.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC04IPWRG4Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional pinout of the SN74HC04-Q1

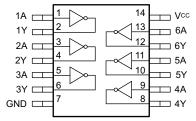




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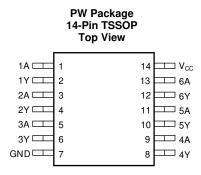
4 Revision HistoryNOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	Changes from Revision A (April 2008) to Revision B	Page
•	Updated to new data sheet standards	1
•	Deleted Q version of device from Electrical Specifications as it is no longer available	4
•	Changed R _{0JA} for PW package from 113 °C/W to 151.7 °C/W	4

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5 Pin Configuration and Functions



Pin Functions

	PIN			
NAME	NO.	I/O	DESCRIPTION	
1A	1	Input	Channel 1, Input A	
1Y	2	Output	Channel 1, Output Y	
2A	3	Input	Channel 2, Input A	
2Y	4	Output	Channel 2, Output Y	
ЗА	5	Input	Channel 3, Input A	
3Y	6	Output	Channel 3, Output Y	
GND	7	_	Ground	
4Y	8	Output	Channel 4, Output Y	
4A	9	Input	Channel 4, Input A	
5Y	10	Output	Channel 5, Output Y	
5A	11	Input	Channel 5, Input A	
6Y	12	Output	Channel 6, Output Y	
6A	13	Input	Channel 6, Input A	
V _{CC}	14	_	Positive Supply	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	TINU
V_{CC}	Supply voltage		-0.5	7	٧
I_{IK}	Input clamp current ⁽²⁾	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I _{OK}	Output clamp current ⁽²⁾	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T_J	Junction temperature (3)			150	ô
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(3) Guaranteed by design.

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



6.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Electrostatio discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2		V
	Electrostatic discharge	Charged device model (CDM), per AEC Q100- 011 CDM ESD Classification Level C6	±1000	V

⁽¹⁾ AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		2	5	6	V
		V _{CC} = 2 V	1.5			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			V
		V _{CC} = 6 V	4.2			
V _{IL} Low-level input voltage	V _{CC} = 2 V			0.5		
	Low-level input voltage	V _{CC} = 4.5 V			1.35	V
		V _{CC} = 6 V			1.8	
VI	Input voltage		0		V _{CC}	V
Vo	Output voltage		0		V _{CC}	V
		V _{CC} = 2 V			1000	
Δt/Δv Input	Input transition rise and fall rate	V _{CC} = 4.5 V			500	ns
		V _{CC} = 6 V			400	
T _A	Operating free-air temperature	SN74HC04I-Q1	-40		85	°C

6.4 Thermal Information

		SN74HC04-Q1	
	THERMAL METRIC	PW (TSSOP)	UNIT
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W



6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25$ °C (unless otherwise noted).

					0	perating	free-air	temperat	ure (T _A)			
F	PARAMETER	TEST CONDITIONS		V _{cc}	25°C			-40°C to 85°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
				2 V	1.9	1.998		1.9				
			$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4				
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}		6 V	5.9	5.999		5.9			V	
	Voltago		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.84				
			$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.34				
		V _I = V _{IH} or V _{IL}			2 V		0.002	0.1			0.1	
			$I_{OL} = 20 \mu A$	4.5 V		0.001	0.1			0.1		
V_{OL}	Low-level output voltage		$V_I = V_{IH} \text{ or } V_{IL}$		6 V		0.001	0.1			0.1	V
	voitage		I _{OL} = 4 mA	4.5 V		0.17	0.26			0.33		
			I _{OL} = 5.2 mA	6 V		0.15	0.26			0.33		
II	Input leakage current	V _I = V _{CC} or 0		6 V		±0.1	±100			±1000	nA	
I _{CC}	Supply current	$V_I = V_{CC}$ or 0	I _O = 0	6 V			2			20	μΑ	
C _i	Input capacitance			2 V to 6 V		3	10			10	pF	

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

					Op	erating	free-air	tempera	ture (T _A)		
	PARAMETER	FROM	то	V _{CC}		25°C		-40°	C to 85	°C	UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
				2 V		45	95			120		
t _{pd}	Propagation delay	A or B	A or B	Υ	4.5 V		9	19			24	ns
				6 V		8	16			20		
				2 V		38	75			95		
t _t	t _t Transition-time	Y	4.5 V		8	15			19	ns		
			6 V		6	13			16			

6.7 Operating Characteristics

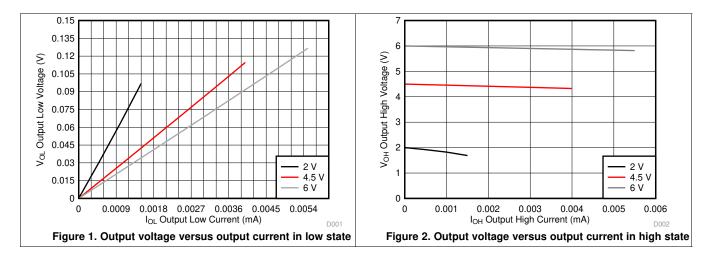
over operating free-air temperature range; typical values measured at $T_A = 25$ °C (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{pd}	Power dissipation capacitance per gate	No load		20		pF

TEXAS INSTRUMENTS

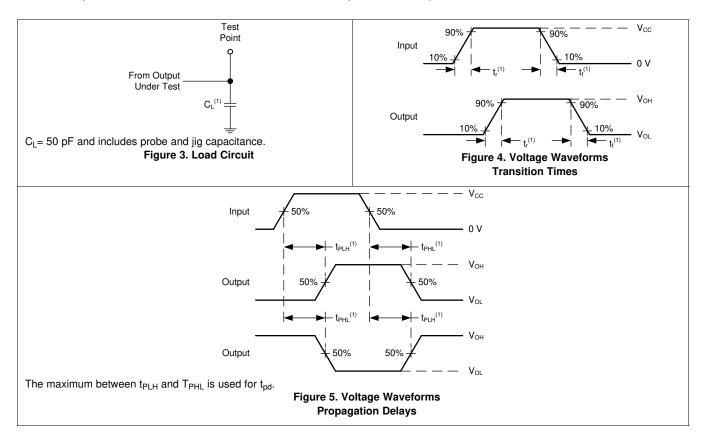
6.8 Typical Characteristics

 $T_A = 25^{\circ}C$



7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
- · The outputs are measured one at a time, with one input transition per measurement.



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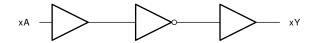


8 Detailed Description

8.1 Overview

This device contains six independent inverters. Each gate performs the Boolean function $Y = \overline{A}$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74HC04-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a highimpedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the Absolute Maximum Ratings.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the Electrical Characteristics. The worst case resistance is calculated with the maximum input voltage, given in the Absolute Maximum Ratings, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law $(R = V \div I)$.

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in the Recommended Operating Conditions to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

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Feature Description (continued)

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 6.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

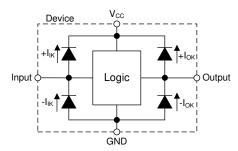


Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1. Function Table

INPUT	OUTPUT
Α	Υ
L	Н
Н	L

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HC04-Q1 can be used to add an additional stage to a counter with an external flip-flop. Because counters use a negative edge trigger, the flip-flop's clock input must be inverted to provide this function. This function only requires one of the six available inverters in the SN74HC04-Q1 device, so the remaining channels can be used for other applications needing an inverted signal or improved signal integrity. Unused inputs must be terminated at $V_{\rm CC}$ or GND. Unused outputs can be left floating.

9.2 Typical Application

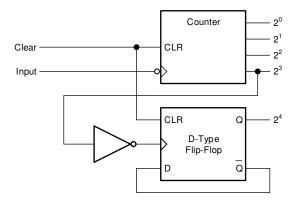


Figure 7. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC04-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{od} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, $T_J(max)$ listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

Typical Application (continued)

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC04-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HC04-Q1 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to the Feature Description for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to Feature Description for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

- 1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout*.
- 2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC04-Q1 to the receiving device.
- 3. Ensure the resistive load at the output is larger than $(V_{CC} / I_O(max)) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
- Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

9.2.3 Application Curves

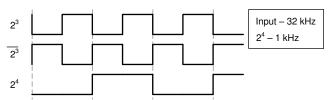


Figure 8. Application timing diagram



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 9*.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

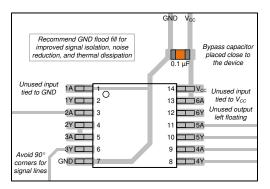


Figure 9. Example layout for the SN74HC04-Q1

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

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12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
SN74HC04IPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC04I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74HC04-Q1:



PACKAGE OPTION ADDENDUM

10-Dec-2020

• Catalog: SN74HC04

• Military: SN54HC04

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 3-Jun-2022

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC04IPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 3-Jun-2022



*All dimensions are nominal

Ì	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	SN74HC04IPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0	

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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