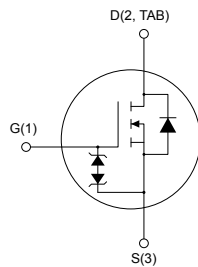
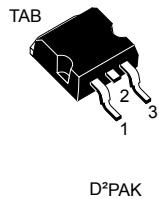


## N-channel 900 V, 280 mΩ typ., 15 A MDmesh K5 Power MOSFET in a D<sup>2</sup>PAK package



AM01475V1


**Product status link**
[STB16N90K5](#)
**Product summary**

<b>Order code</b>	STB16N90K5
<b>Marking</b>	16N90K5
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB16N90K5	900 V	330 mΩ	15 A

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	9	A
$I_D^{(1)}$	Drain current (pulsed)	60	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_j$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 15\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 450\text{ V}$ .
3.  $V_{DS} \leq 720\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.66	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	$^\circ\text{C}/\text{W}$

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	380	mJ

## 2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified

**Table 4. On/off state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	900			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 7.5\text{ A}$		280	330	m $\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1027	-	pF
$C_{oss}$	Output capacitance		-	106	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	1.6	-	pF
$C_{o(er)}$ <sup>(1)</sup>	Equivalent capacitance energy related	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }720\text{ V}$	-	51	-	pF
$C_{o(tr)}$ <sup>(2)</sup>	Equivalent capacitance time related				141	-
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	1	4.9	9	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 720\text{ V}$ , $I_D = 15\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	29.7	-	nC
$Q_{gs}$	Gate-source charge		-	7.3	-	nC
$Q_{gd}$	Gate-drain charge		-	17.7	-	nC

1.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}$ , $I_D = 7.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	28.8	-	ns
$t_r$	Rise time		-	36	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	46	-	ns
$t_f$	Fall time		-	9.8	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15\text{ A}, V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 15\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	458		ns
$Q_{rr}$	Reverse recovery charge		-	8.13		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	35.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 15\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V},$ $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	546		ns
$Q_{rr}$	Reverse recovery charge		-	9.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	33.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}, I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

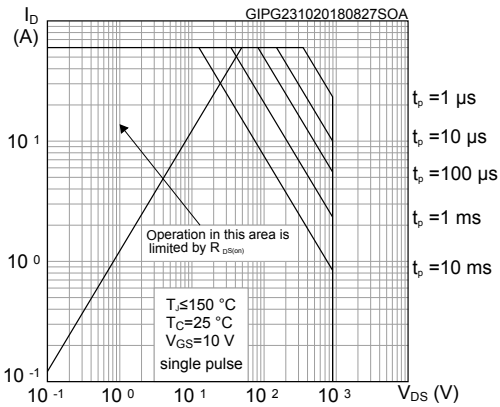


Figure 2. Normalized transient thermal impedance

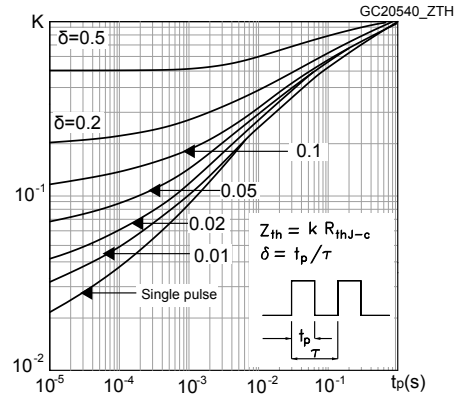


Figure 3. Typical output characteristics

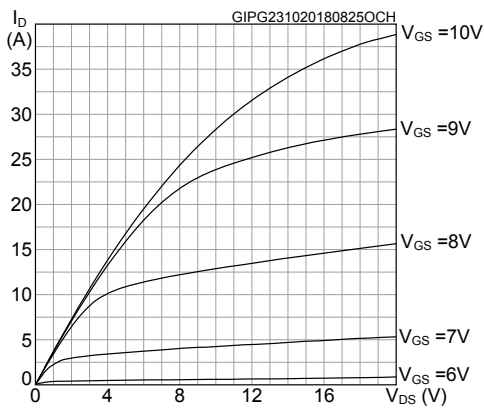


Figure 4. Typical transfer characteristics

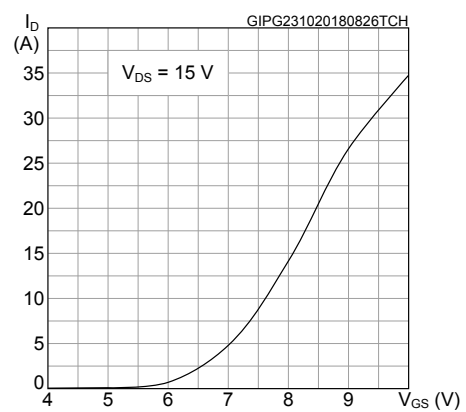


Figure 5. Normalized breakdown voltage vs temperature

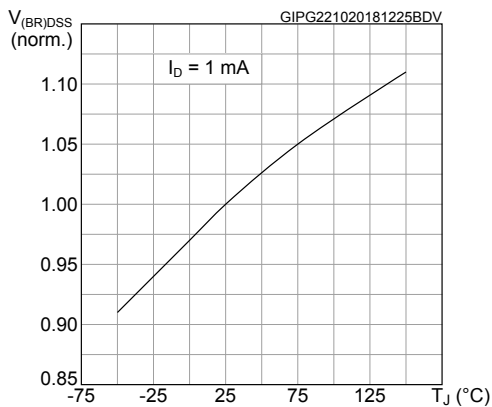
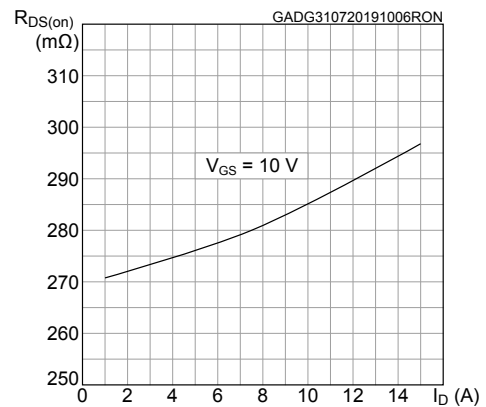
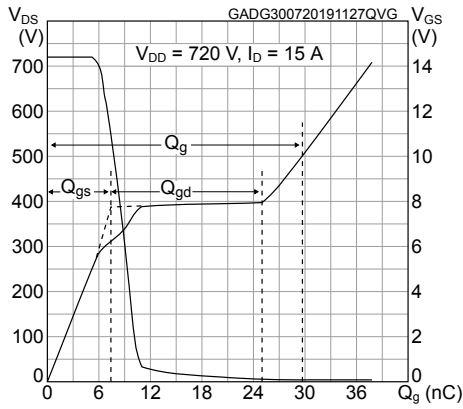


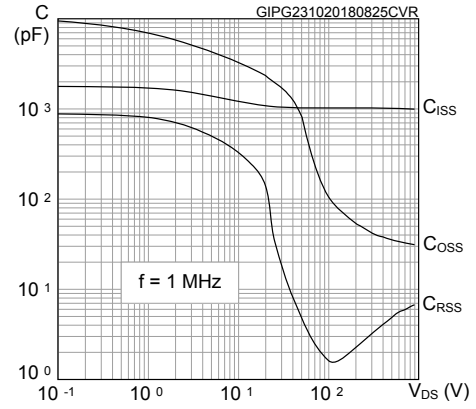
Figure 6. Typical drain-source on-resistance



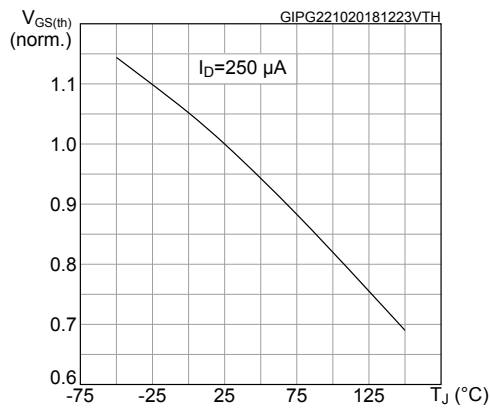
**Figure 7. Typical gate charge characteristics**



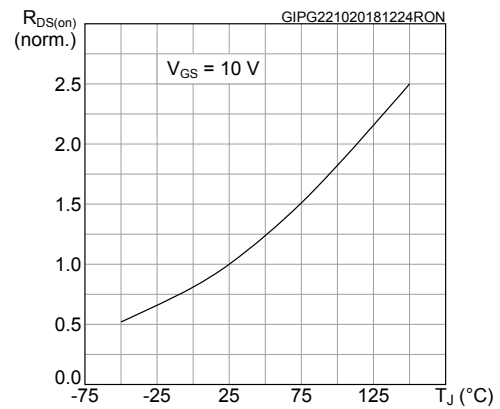
**Figure 8. Typical capacitances vs voltage**



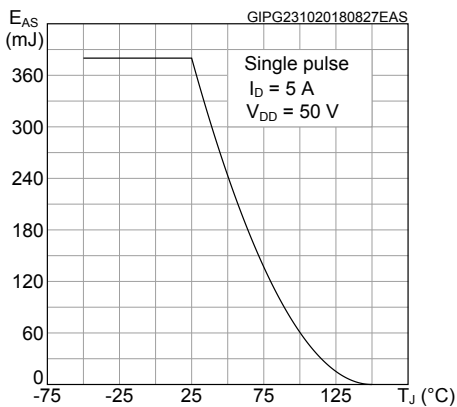
**Figure 9. Normalized threshold voltage vs temperature**



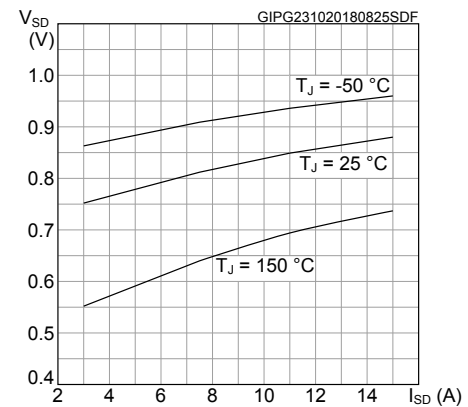
**Figure 10. Normalized on-resistance vs temperature**



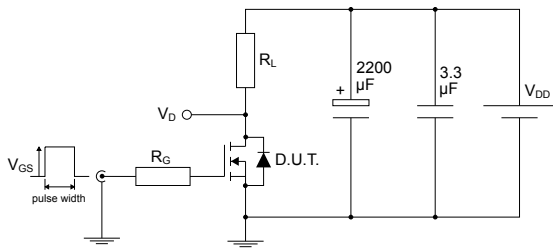
**Figure 11. Maximum avalanche energy vs temperature**



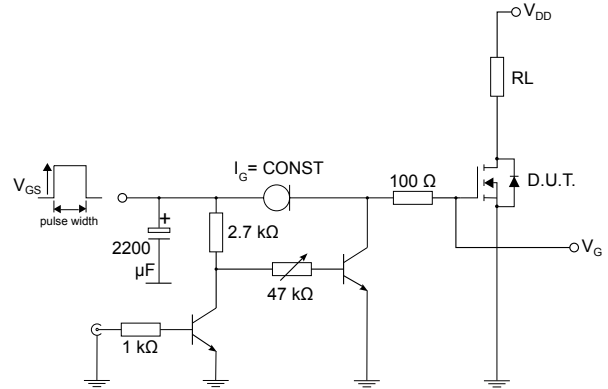
**Figure 12. Typical source-drain diode characteristics**



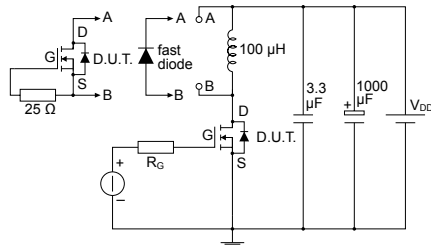
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


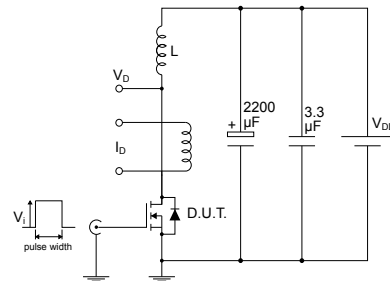
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**Figure 14. Test circuit for gate charge behavior**


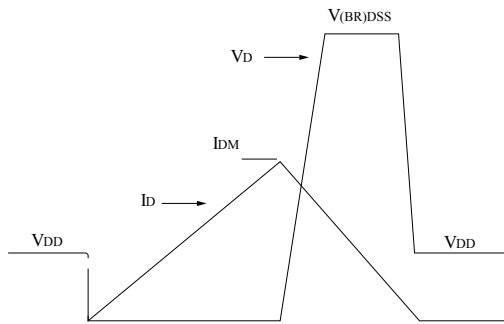
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


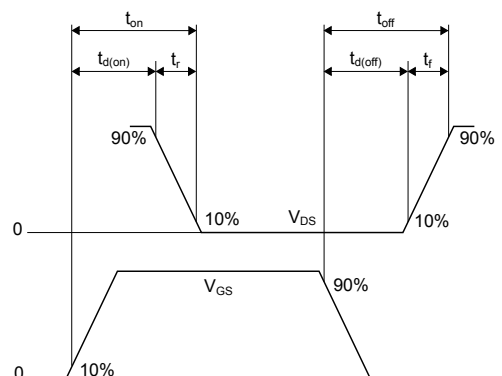
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**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

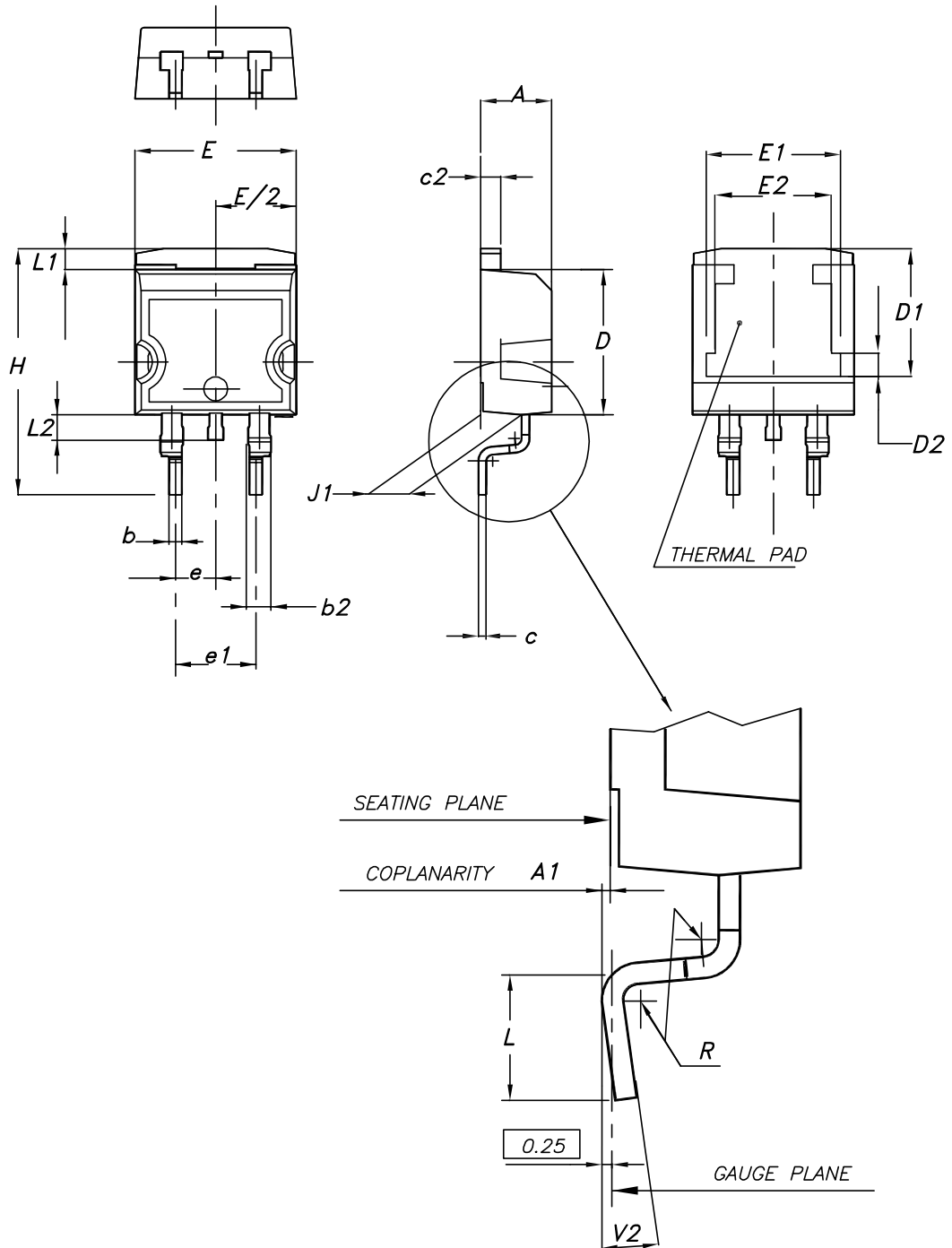
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



### 4.1 D<sup>2</sup>PAK (TO-263) package information

Figure 19. D<sup>2</sup>PAK (TO-263) type A package outline

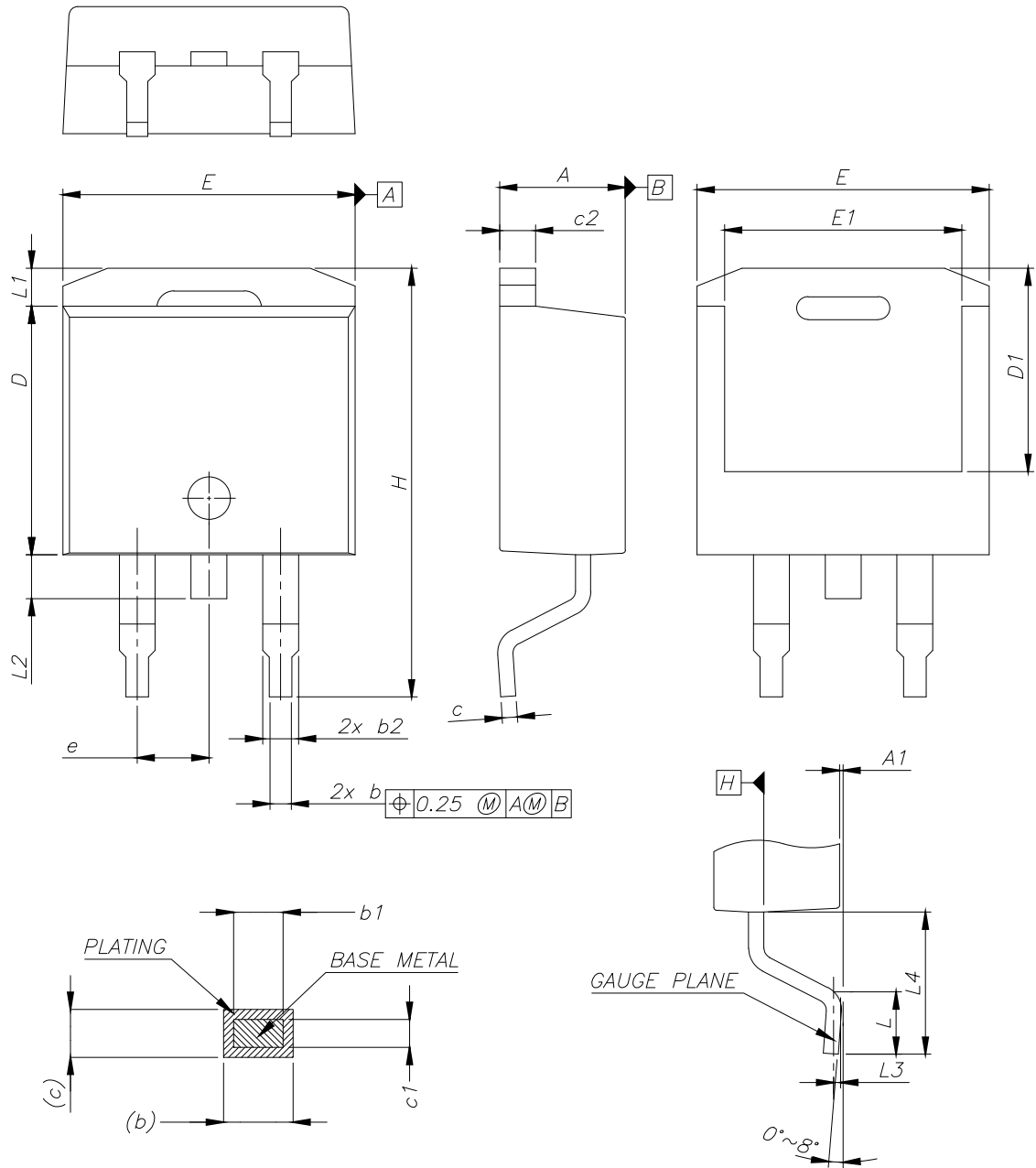


0079457\_26

**Table 9. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 20. D<sup>2</sup>PAK (TO-263) type B package outline

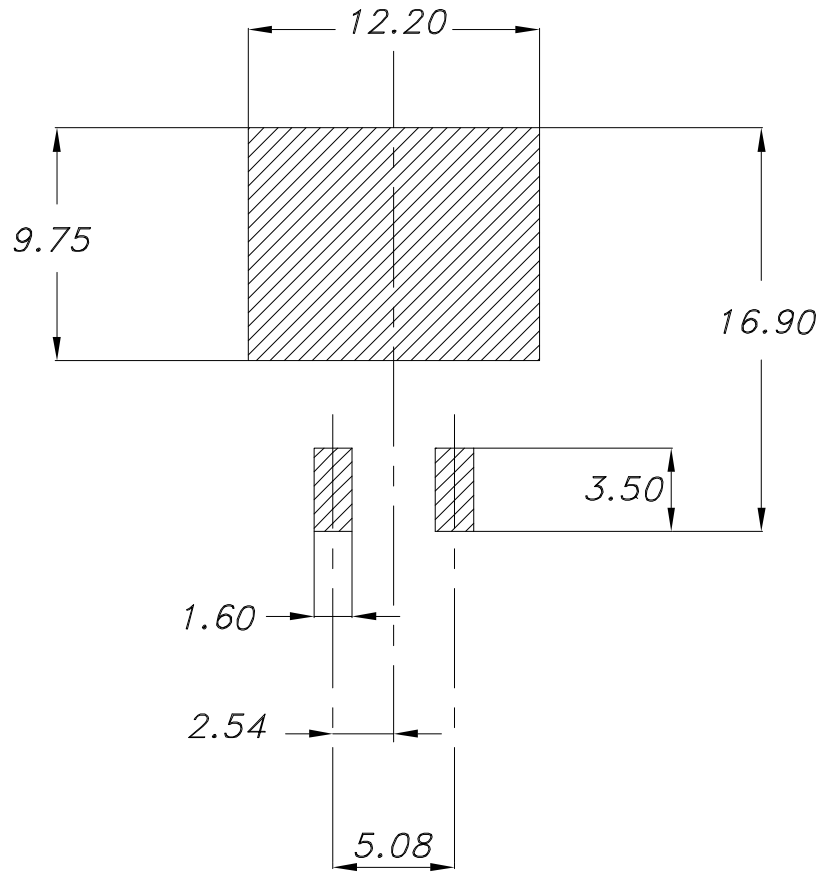


0079457\_26\_B

**Table 10. D<sup>2</sup>PAK (TO-263) type B mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

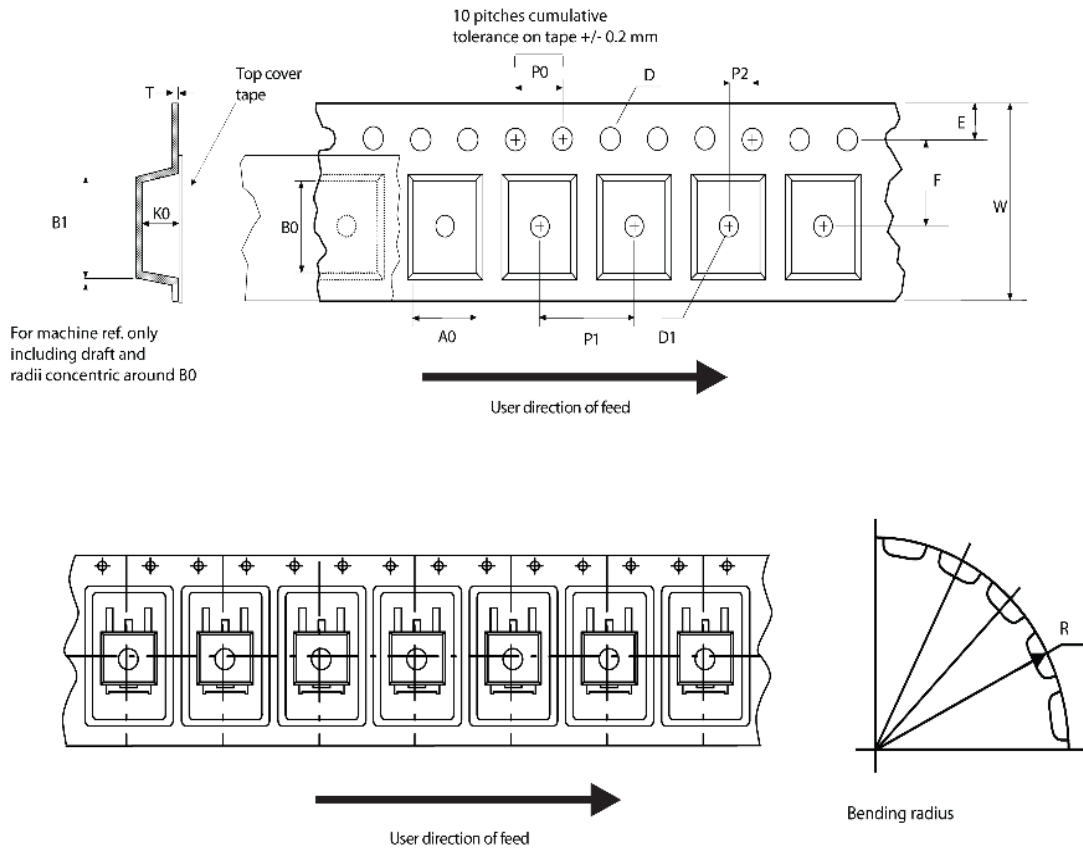
Figure 21. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



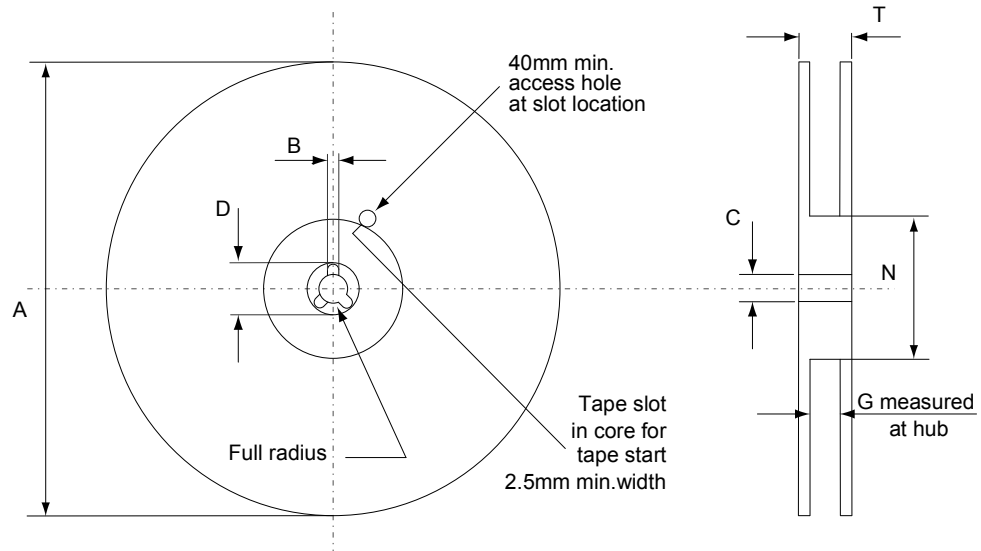
Footprint\_26

## 4.2 D<sup>2</sup>PAK packing information

Figure 22. D<sup>2</sup>PAK tape outline



AM08852v1

**Figure 23. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 11. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel			
Dim.	mm		Dim.	mm		
	Min.	Max.		Min.	Max.	
A0	10.5	10.7	A		330	
B0	15.7	15.9	B	1.5		
D	1.5	1.6	C	12.8	13.2	
D1	1.59	1.61	D	20.2		
E	1.65	1.85	G	24.4	26.4	
F	11.4	11.6	N	100		
K0	4.8	5.0	T		30.4	
P0	3.9	4.1	Base quantity Bulk quantity			
P1	11.9	12.1				1000
P2	1.9	2.1				1000
R	50					
T	0.25	0.35				
W	23.7	24.3				

### 4.3 D<sup>2</sup>PAK type B packing information

Figure 24. D<sup>2</sup>PAK type B tape outline

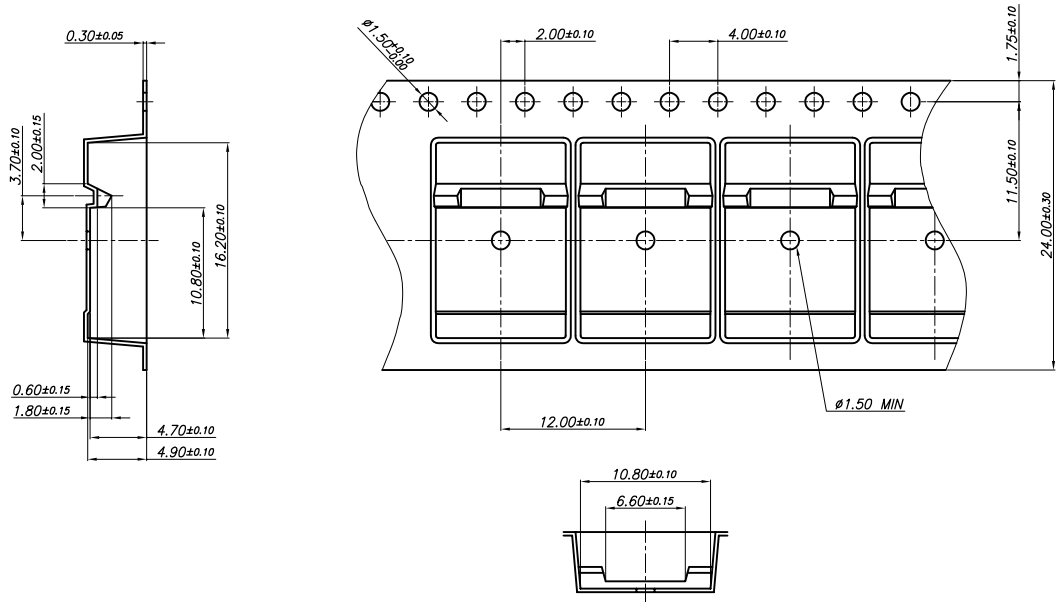
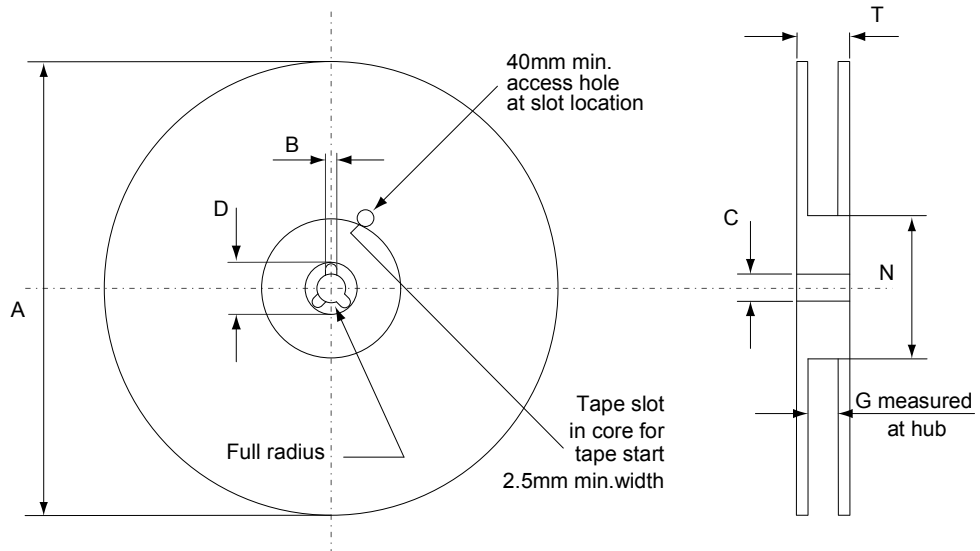


Figure 25. D<sup>2</sup>PAK type B reel outline



AM06038v1



**Table 12. D<sup>2</sup>PAK type B reel mechanical data**

Dim.	mm	
	Min.	Max.
A		330
B	1.5	
C	12.8	13.2
D	20.2	
G	24.4	26.4
N	100	
T		30.4

## Revision history

**Table 13. Document revision history**

Date	Revision	Changes
23-Oct-2018	1	Initial release.
05-Aug-2019	2	Updated <a href="#">Section 2.1 Electrical characteristics (curves)</a> . Minor text changes.

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