EPC9158: 48 V/54 V Input to 12 V, 50 A Output Dual Phase Synchronous Buck Converter Evaluation Board Quick Start Guide

Revision 2.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC9158 is a 48 V/54 V to 12 V synchronous buck converter and can deliver 25 A per phase or 50 A total when configured for a single output. EPC9158 features **EPC2218** enhancement mode eGaN® FET and LTC7890 two phase analog buck controller with integrated eGaN drivers. The board features:

- High efficiency: 96.5% with 48 V input and 12 V output configuration
- Switching frequency: 500 kHz
- Current mode control
- Reconfigurable light load operating mode and adjustable dead time
- Operating modes and other functions:
  - o UVLO
  - o Overcurrent protection
  - o Power good
  - o External synchronization

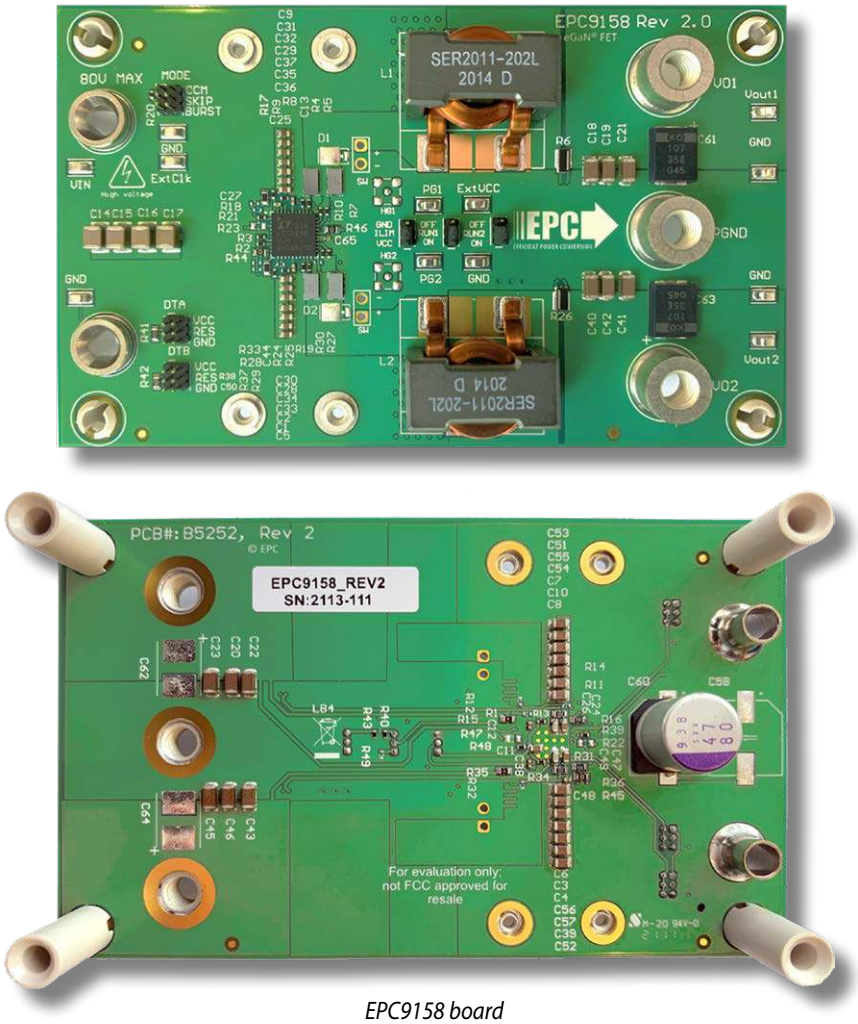
REGULATORY INFORMATION

This power module is for evaluation purposes only. It is not a full-featured power module and cannot be used in final products. No EMI test was conducted. It is not FCC approved.

Table 1: Electrical Characteristics (T_a = 25)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage	f_S = 500 kHz	14	48	54	V
$V_{IN,on}$	Input UVLO turn on voltage	Run1 tied to Vin		4		
V_{OUT}	Output Voltage			12		V
V_{OUT_RIP}	Output Voltage Ripple	Peak to peak		100		mV
I_{OUT}	Output Current	Dual phase, 400 LFM air flow			50 [1]	A
f_S	Switching Frequency	Mode=CCM		500		kHz

[1] The maximum current capability is dependent on thermal conditions. The FET temperature should be monitored to ensure the maximum temperature does not exceed the rating in the datasheet. Especially when the input voltage is higher than 54 V, the maximum output current is reduced.



EPC9158 board

QUICK START PROCEDURE

The demonstration board EPC9158 is easy to set up to evaluate the performance of the EPC2218 eGaN FETs and directly drive from the controller IC. Refer to figure 1 for proper connect and measurement setup and follow the procedure below:

1. Check that the jumpers are set to their default locations as shown in figure 1.
2. With power off, connect the input power supply between V_{IN} (J9) and GND (J10) banana jacks as shown. A shunt can be inserted to measure input current in the positive line only.
3. With power off, connect a load as needed between V_{OUT1} and V_{OUT2} (J4 and J8) and GND (J18) as shown in figure 1.
   Note: V_{OUT2} must be connected to V_{OUT1} in this configuration.
4. Make sure the load is off before turning on the supply voltage. The applied voltage should not exceed 80 V under any conditions.
5. Check the output voltage is regulated to 12 V to make sure the board is functional and operating at no-load. If 12 V is not observed, please carefully re-examine the circuit connections.
6. Activate the load and set to the desired current ensuring the current does not exceed the maximum ratings.
7. Once operational, adjust the input voltage and load current within the allowed operating range and observe the output switching behavior, efficiency and other parameters as desired. For measuring switch node waveforms, please use probe sockets provided without a probe ground lead. **Please note polarity.**
8. For shutdown, please follow steps in reverse of step 1–5. For custom configuration please refer the optional configuration section.

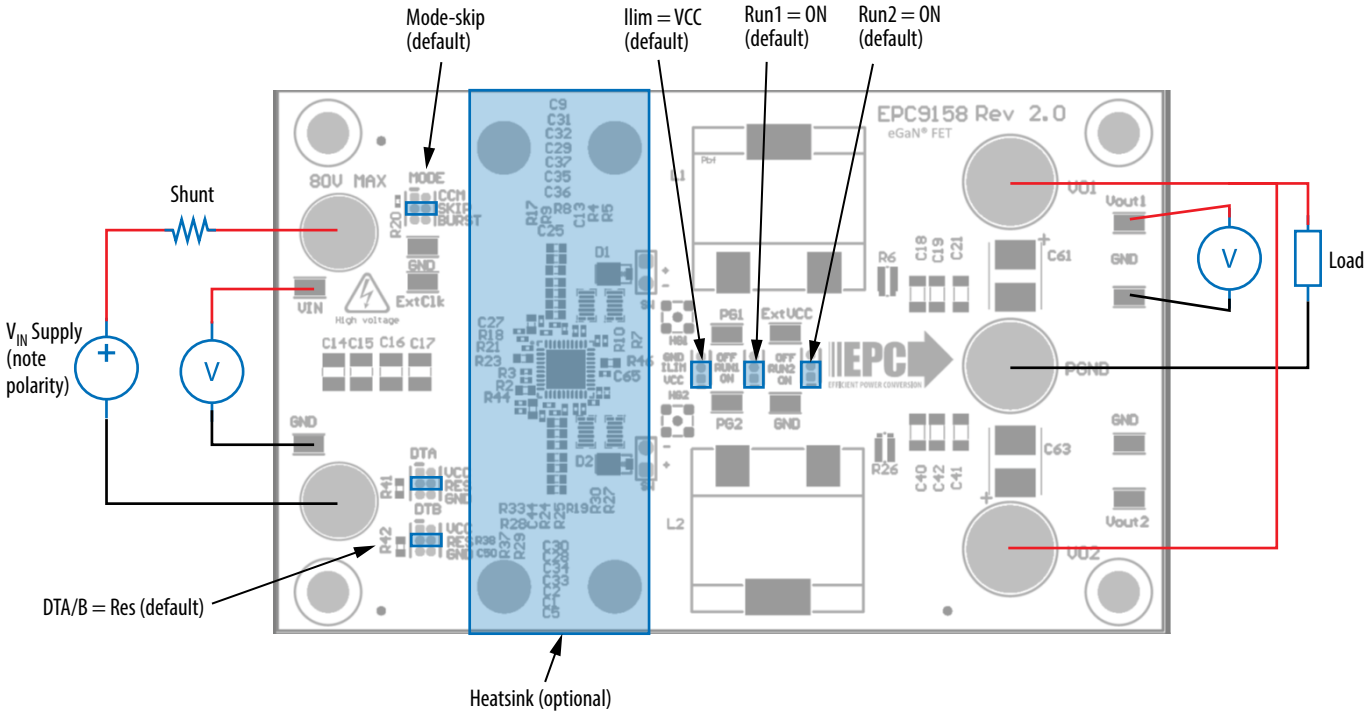


Figure 1: Proper connection set up and default jumper positions

EXPERIMENTAL RESULTS

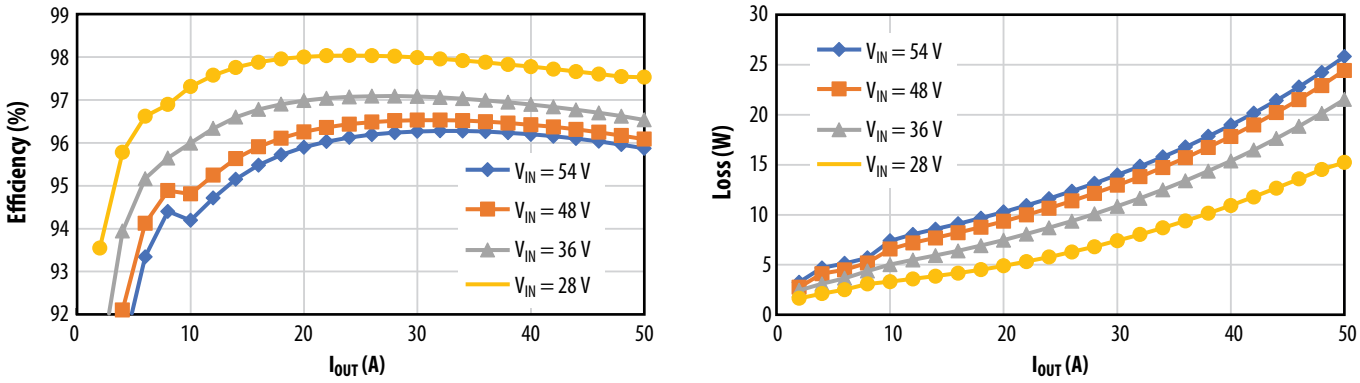


Figure 2: Typical efficiency and power losses (mode = skip, DTA/B = Res)

Typical output voltage ripple

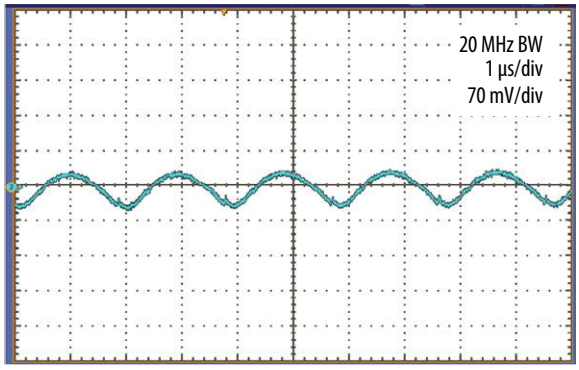


Figure 3: V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 50 A

Typical transient response

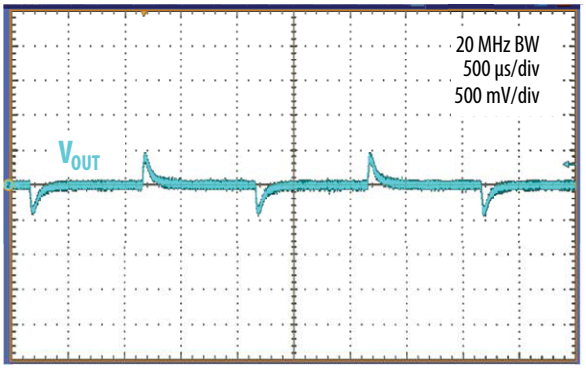


Figure 4: V_{IN} = 48 V, V_{OUT} = 12 V, output 50% (25 A) to 100% (50 A), 500 Hz transitions, di/dt =2 A/us

Startup waveform

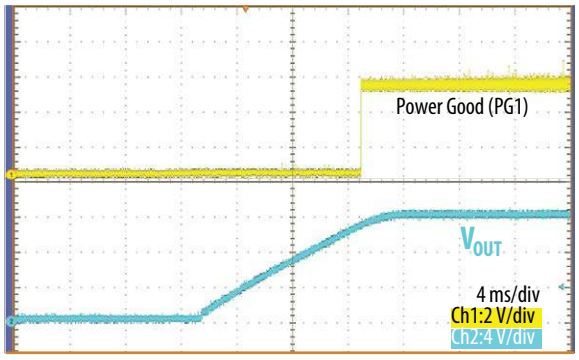


Figure 5: V_{IN} = 48 V, V_{OUT} = 12 V (Ilim = VCC)

Typical load regulation

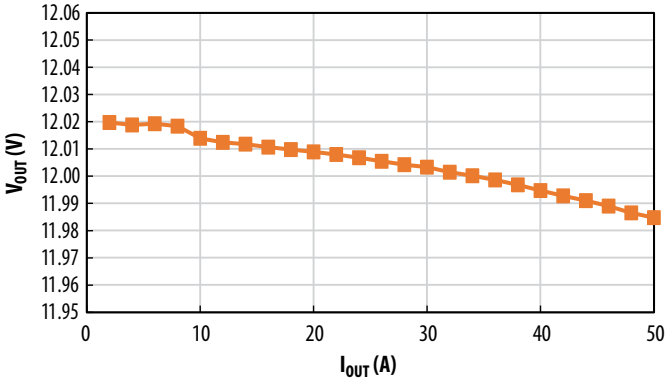
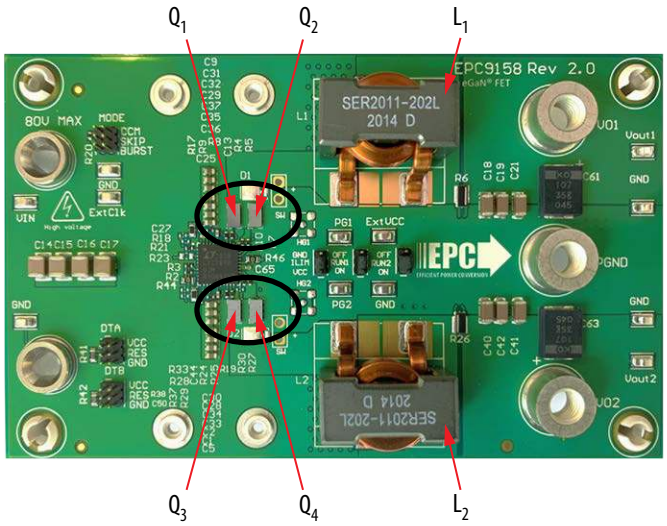


Figure 6: V_{IN} = 48 V, V_{OUT} = 12 V

Thermal performance



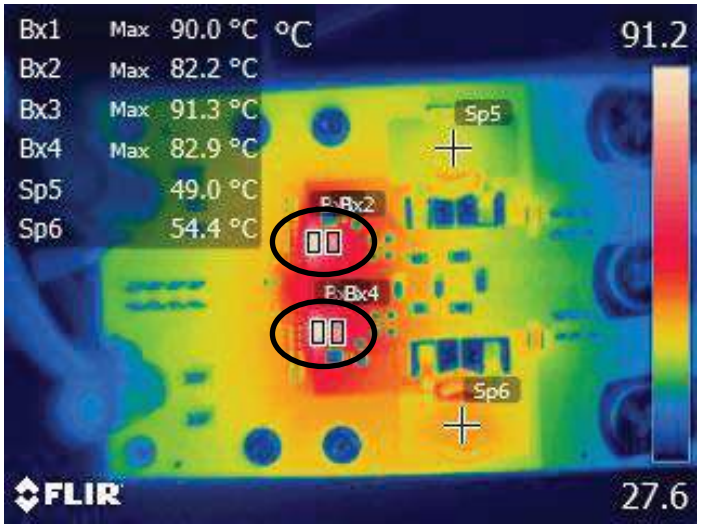


Figure 7: V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 50 A, 400 LFM air flow

CUSTOM CIRCUIT CONFIGURATIONS

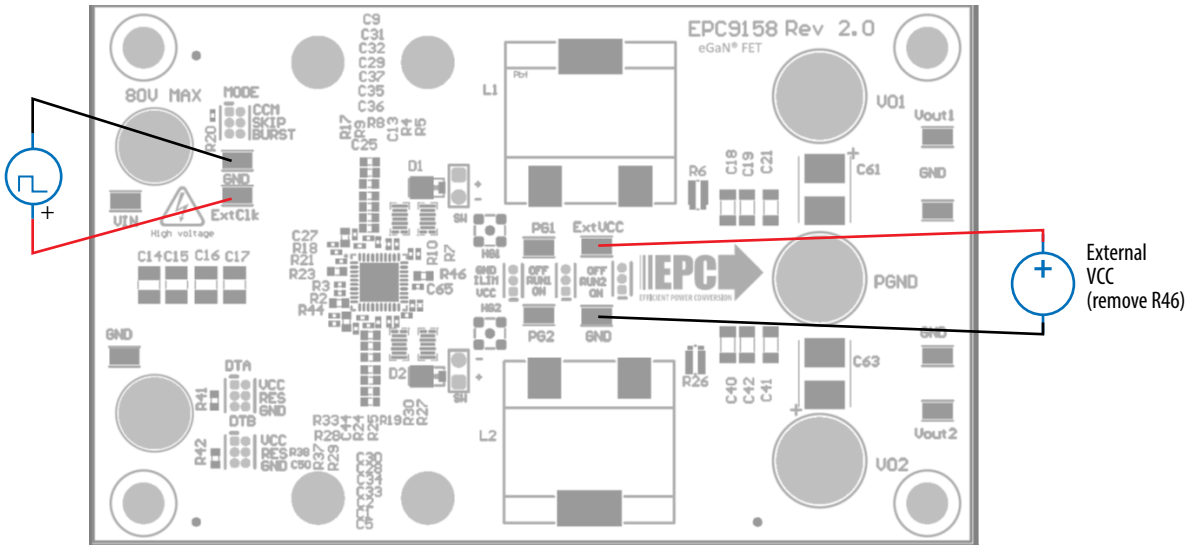


Figure 8: An example custom circuit connection with external VCC and clock

Single /Dual phase operation

By default, Dual phase operation is enabled. For single phase operation, please use Run2 jumper in the off position to disable phase 2.

Phase 1 cannot be disabled because the output of phase 1 is used to power the controller IC.

This board can also be configured as two independent single phase buck converters. To do so, remove R44 and R45 and adjust the feedback network to set the output voltages of each phase. Please refer to LTC7890 datasheet for more information.

Input UVLO adjustment

The V_{IN} UVLO threshold voltage can be set by R48 and R49. By default, R48 is shorted while R49 is open, the UVLO threshold is determined by the controller IC (around 4V). If needed, a new UVLO voltage can be set by changing R48 and R49: Please refer to LTC7890 datasheet for more information.

$$UVLO\ rising = 1.2\ V\left(1+\frac{R48}{R49}\right)$$

$$UVLO\ falling = 1.1\ V\left(1+\frac{R48}{R49}\right)$$

Switching frequency adjustment

If needed, switching frequency can be modified by changing the value of R21. Please refer to LTC7890 datasheet for more information.

$$f_S\,(MHz) \approx \frac{37\,(MHz)}{R21\,(k\Omega)}$$

External VCC

While the chip can be solely powered by the main power supply V_{IN}, the losses may be high for high input voltage. There are solutions which can reduce the power dissipation in the controller. By default, Ext VCC is connected to phase 1 output (R46 = 0 Ω). The light load efficiency can be further improved if connect an external low voltage power supply (for e.g. 5V) to Ext VCC (TP6) and GND as shown in figure 9. Please remove R46 before doing so. Please refer to LTC7890 datasheet for more information.

External clock synchronization

Some systems require power supplies be synchronized. An external clock can be connected to synchronize the PWM to an external clock as shown in figure 9. Please refer to the datasheet of LTC7890 for any limitations.

Deadtime adjustment

Dead time control is important for eGaN FETs, especially for high frequencies and high current applications. The dead time is controlled by the resistance values of R41 and R42 for rising and falling edges respectively. Additionally, Jumper J21 and J13 can be used to enable adaptive and fixed dead time control as supported by the LTC7890 controller. Please refer to LTC7890 datasheet for more information.

MECHANICAL DRAWING

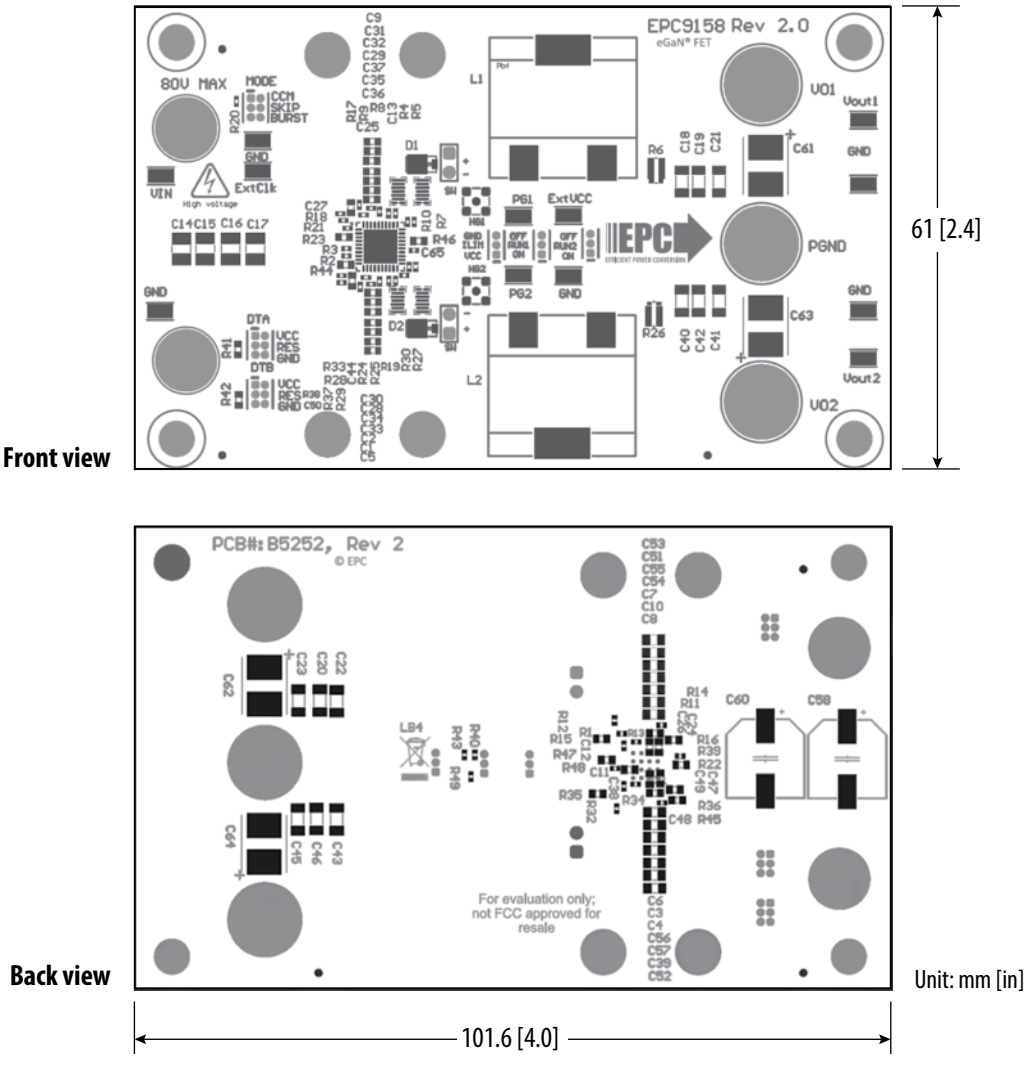


Figure 9: Mechanical dimensions

THERMAL MANAGEMENT (optional)

The EPC9158 is intended for bench evaluation at room temperature with forced air convection cooling. A heatsink is not required but will significantly improve convective heat dissipation from the topside of the FET and increase the current capacity of these devices.

The EPC9158 board is equipped with four mechanical SMD spacers that can be used to easily attach a standard eighth-brick converter heatsink using standard M2 screws (See Figure 10). Thermal interface material (TIM) pads (2x) are required for good thermal conductance between the FETs and the heatsink bottom surface. See Figure 10 for minimum required TIM pad size.

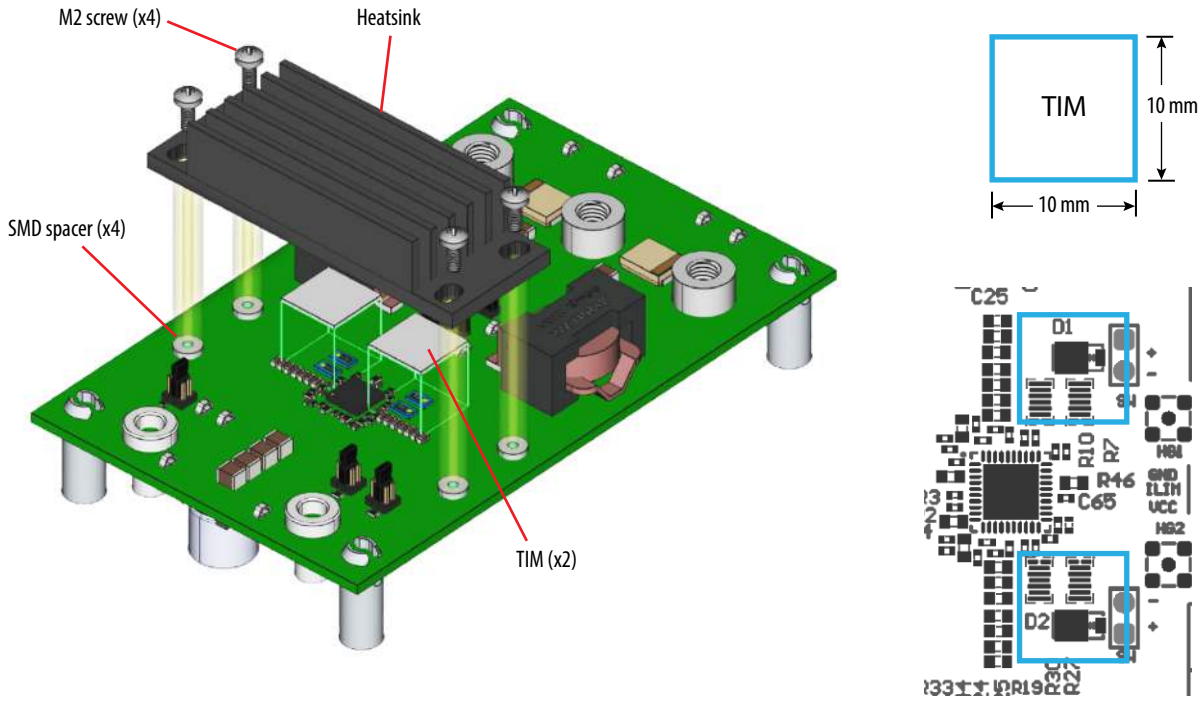


Figure 10: Exploded 3D assembly of heat sink installment and locations of TIM material

The following heat sink is recommended for EPC9158:

- **Wakefield** P/N : 567-45AB

A TIM is required between the FETs and the heatsink. The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface

EPC recommends the following thermal interface materials (TIM) for EPC9158:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m·K)
- **t-Global** P/N: TG-A6200 X 0.5 mm (moderate conductivity of 6.2 W/m·K)

NOTE. The EPC9158 development board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult: D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC9158 landing page at: https://epc-co.com/epc/Products/DemoBoards/EPC9158.aspx

For More Information:

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