User's Guide

TPS563231 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS563231 as well as support documentation for the TPS563231EVM-032 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS563231EVM-032.

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Trademarks

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1 Introduction

The TPS563231 is a single, adaptive on-time, D-CAP3™ mode, synchronous buck converter requiring a very low external component count. The D-CAP3 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 600 kHz and enters Advanced Eco-mode in light load conditions. The high-side and low-side switching MOSFETs are incorporated inside the TPS563231 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS563231 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS563231 dc/dc synchronous converter is designed to provide up to a 3-A output from an input voltage source of 4.5 V to 17 V. The output voltage range is from 0.6 V to 7 V. Rated input voltage and output current ranges for the evaluation module are given in Table 1-1.

The TPS563231EVM-032 evaluation module (EVM) is a single, synchronous buck converter providing 3.3 V at 3 A from 4.5-V to 17-V input. This user's guide describes the TPS563231EVM-032 performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS563231EVM-032	V_{IN} = 4.5 V to 17 V	0 A to 3 A

2 Performance Specification Summary

A summary of the TPS563231EVM-032 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 3.3 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS563231EVM-032 Performance Specifications Summary

SPECIFICATIONS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range (V_{IN})			4.5	12	17	V
CH1	Output voltage			3.3		V
	Operating frequency	V_{IN} = 12 V, I_O = 3 A		600		kHz
	Output current range		0		3	A
	Over current limit	V_{IN} = 12 V, L_O = 3.3 µH				A
	Output ripple voltage	V_{IN} = 12 V, I_O = 3 A		15		mV_{PP}

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS563231. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R5. Changing the value of R5 can change the output voltage above 0.6 V. The value of R5 for a specific output voltage can be calculated using Equation 1.

$$R_5 = \frac{R_6 \times (V_{OUT} - 0.6\,V)}{0.6\,V} \quad (1)$$

Table 3-1 lists the R5 values for some common output voltages. Note that the values given in Table 3-1 are standard values and not the exact value calculated using Table 3-1.

Table 3-1. Output Voltages

OUTPUT VOLTAGE (V)	R5 (kΩ)	R6 (kΩ)	L1 (µH)			C5 + C6 +C7 (µF)
			Min	Typ	Max	
1.0	6.65	10.0	1	1.5	4.7	20 - 68
1.05	7.5	10.0	1	1.5	4.7	20 - 68
1.2	10	10.0	1	1.5	4.7	20 - 68
1.5	15	10.0	1.5	2.2	4.7	20 - 68
1.8	20	10.0	1.5	2.2	4.7	20 - 68
2.5	31.6	10.0	2.2	3.3	4.7	20 - 68
3.3	45.3	10.0	2.2	3.3	4.7	20 - 68
5.0	73.2	10.0	3.3	4.7	4.7	20 - 68
6.5	98.3	10.0	3.3	4.7	4.7	20 - 68

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS563231EVM-032. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

The TPS563231EVM-032 is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability is 3 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP3 provides a place to monitor the V_{IN} input voltages with TP4 providing a convenient ground reference. TP9 is used to monitor the output voltage with TP5 as the ground reference.

Table 4-1. Connection and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 3.3 V at 3-A maximum
JP1	EN control. Shunt EN to GND to disable
TP1	V_{IN} positive power point
TP2,TP11	GND power point
TP3	V_{IN} positive monitor point
TP4,TP5,TP12,TP13	GND monitor test point
TP6	EN test point
TP7	Switch node test point
TP8	Test point for loop response measurements
TP9	V_{OUT} positive monitor point
TP10	V_{OUT} positive power point

4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) pins 1 and 2 are covered to shunt EN to GND, disabling the output.
2. Apply appropriate V_{IN} voltage to VI (J1-2) and GND (J1-1).
3. Move the jumper at JP1 (Enable control) pins 1 and 2 (EN and GND) to enable the output.

4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS563231EVM-032 at an ambient temperature of 25°C.

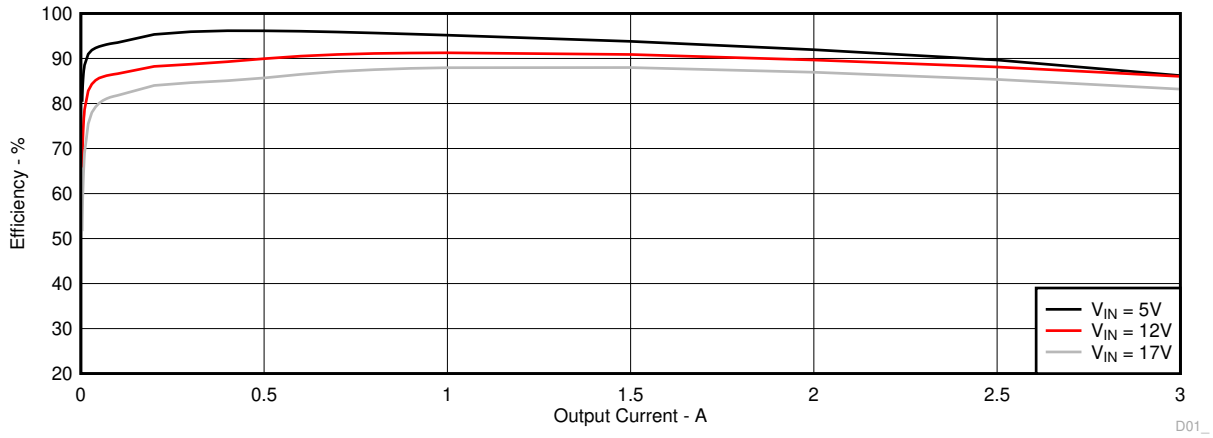

Figure 4-1. TPS563231EVM-032 Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS563231EVM-032 at an ambient temperature of 25°C.

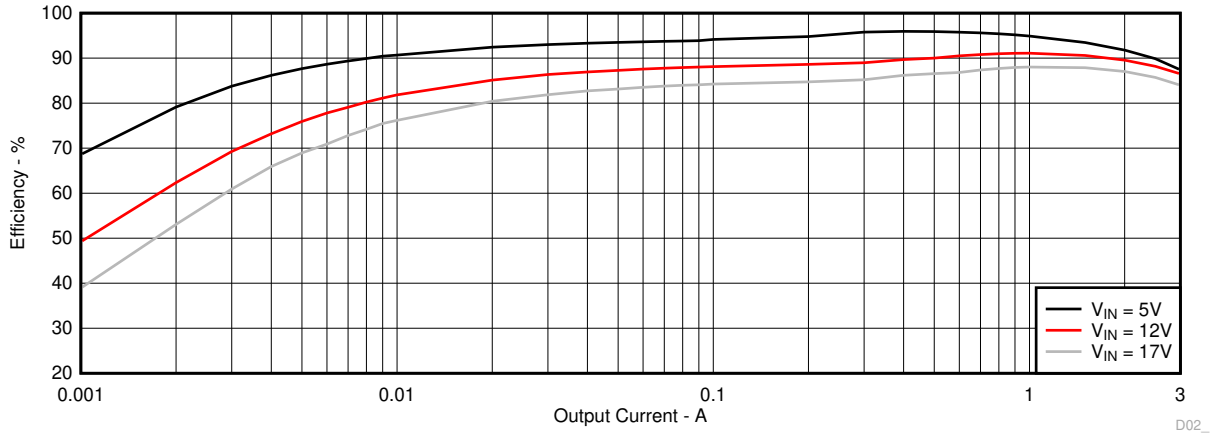

Figure 4-2. TPS563231EVM-032 Light Load Efficiency

4.4 Load Regulation

The load regulation for the TPS563231EVM-032 is shown in Figure 4-3.

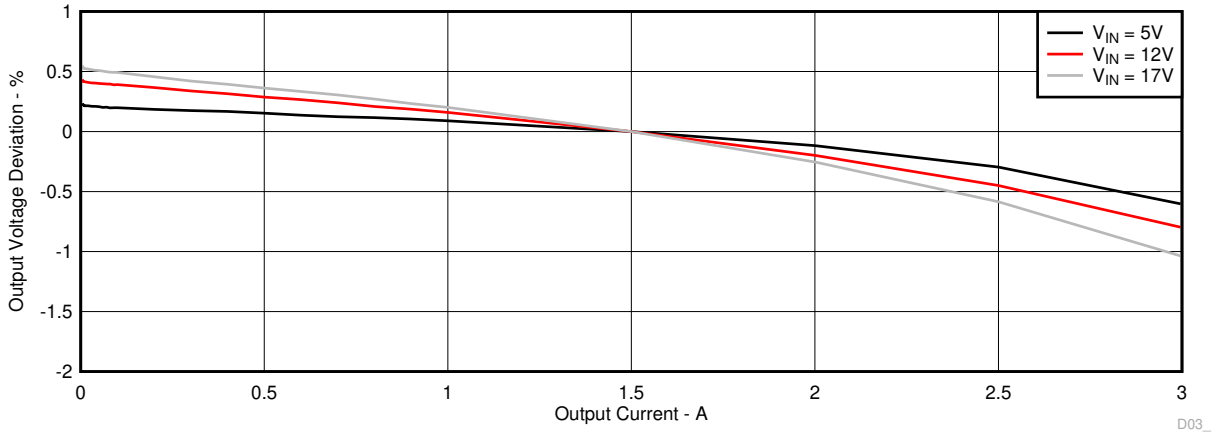

Figure 4-3. TPS563231EVM-032 Load Regulation

4.5 Line Regulation

The line regulation for the TPS563231EVM-032 is shown in Figure 4-4.

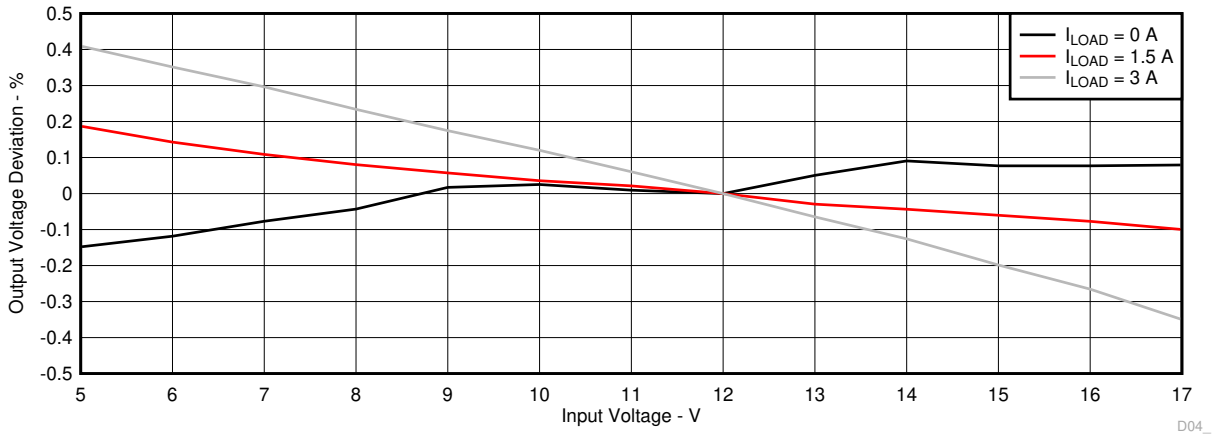

Figure 4-4. TPS563231EVM-032 Line Regulation

4.6 Load Transient Response

The TPS563231EVM-032 response to load transient is shown in Figure 4-5. The current steps and slew rates are indicated in the figures. Total peak-to-peak voltage variation is as shown.

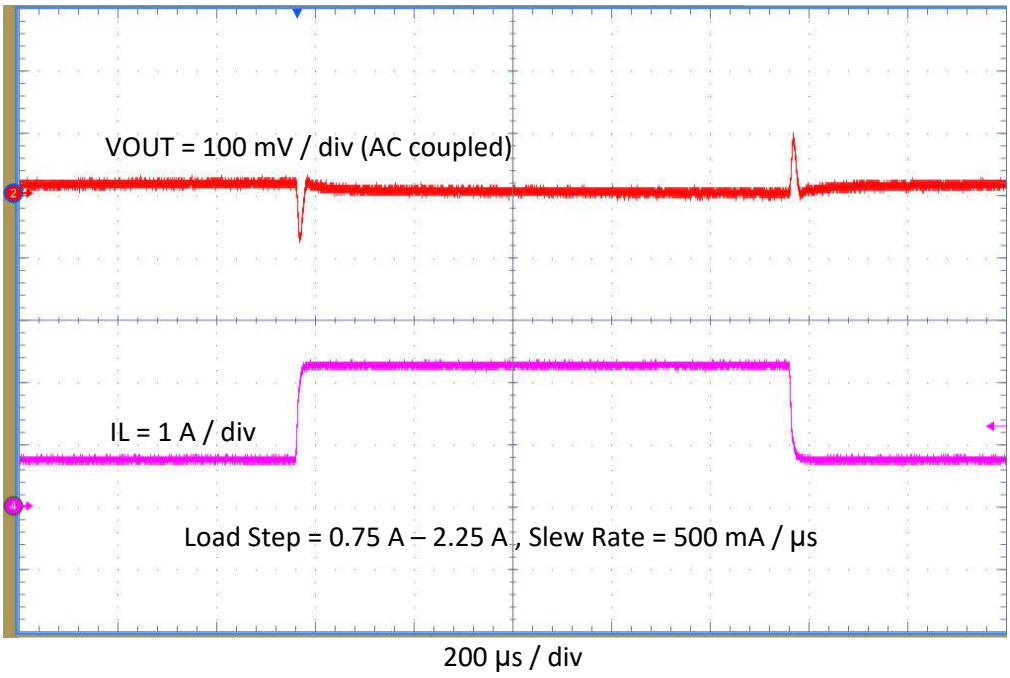

Figure 4-5. TPS563231EVM-032 Load Transient Response, 25% to 75% Load Step

4.7 Output Voltage Ripple

The TPS563231EVM-032 output voltage ripple is shown in Figure 4-6, Figure 4-7, and Figure 4-8. The output currents are as indicated.

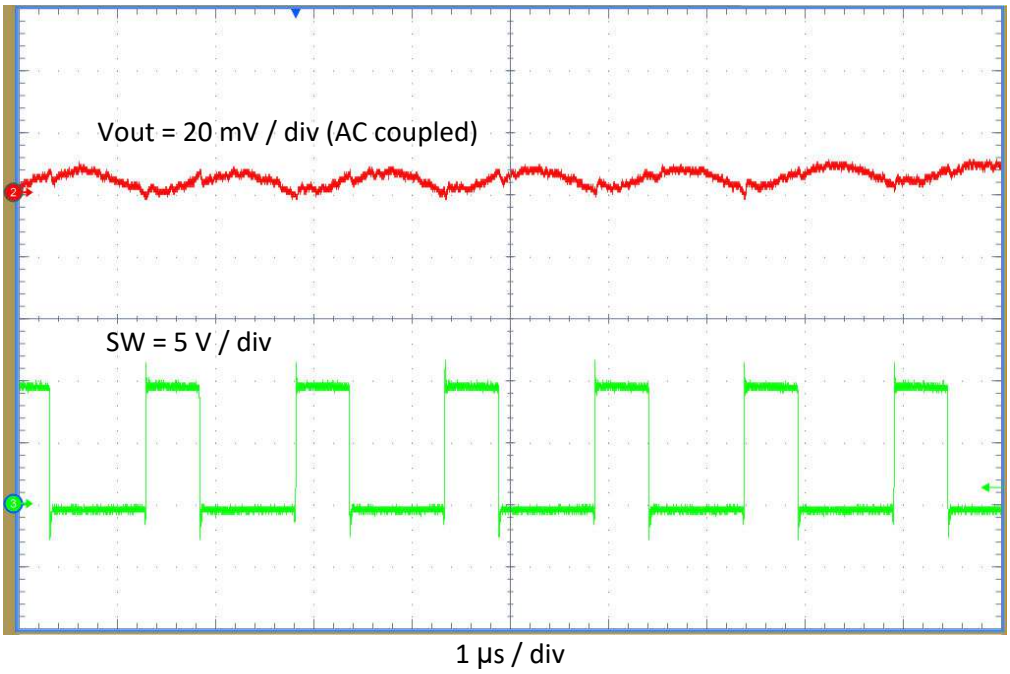

Figure 4-6. TPS563231EVM-032 Output Voltage Ripple, I_{OUT} = 3 A

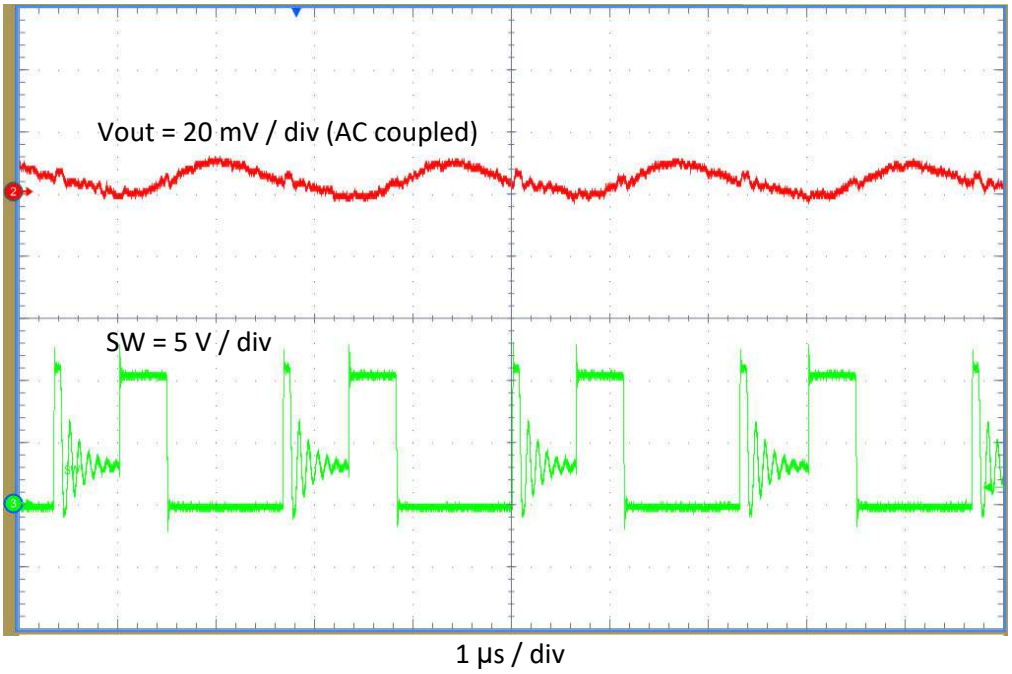

Figure 4-7. TPS563231EVM-032 Output Voltage Ripple, I_{OUT} = 300 mA

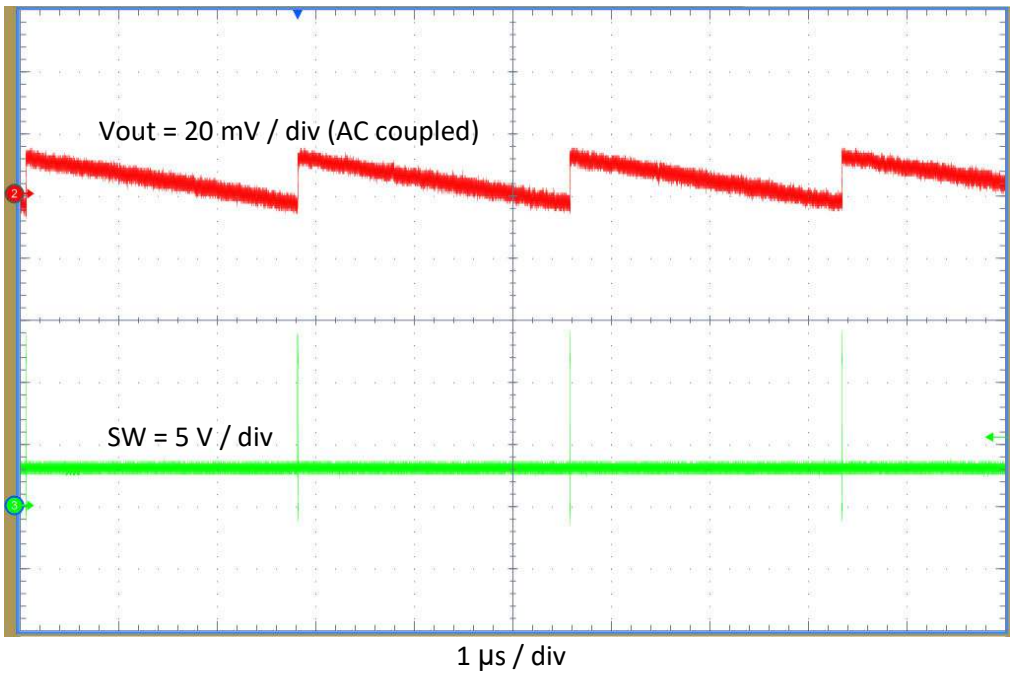

Figure 4-8. TPS563231EVM-032 Output Voltage Ripple, I_{OUT} = 0 mA

4.8 Input Voltage Ripple

The TPS563231EVM-032 input voltage ripple is shown in Figure 4-9. The output current is as indicated.

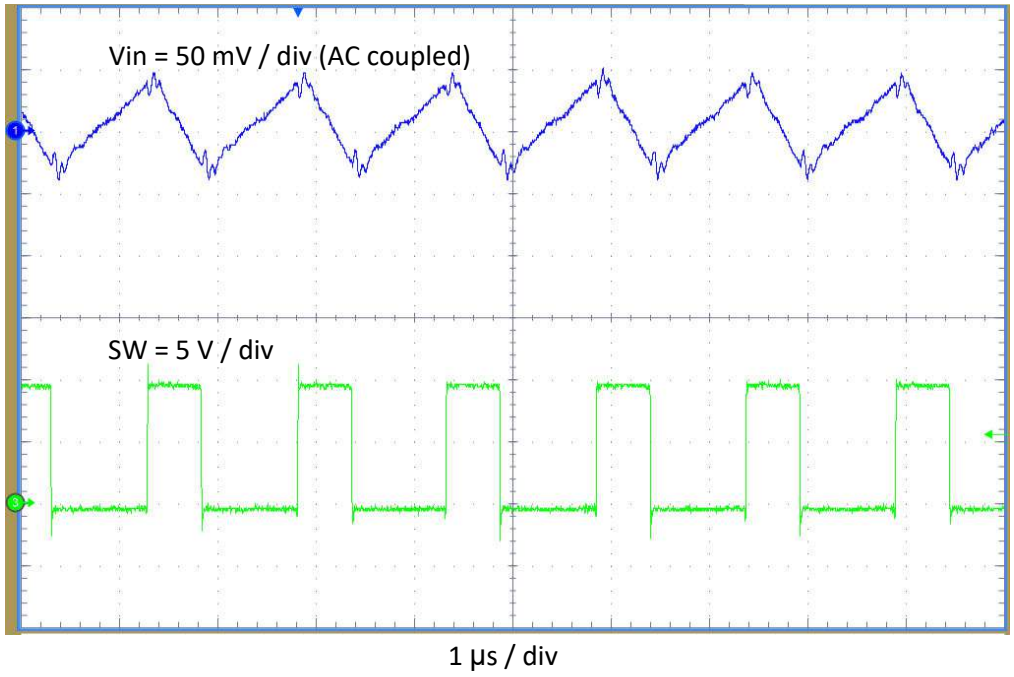

Figure 4-9. TPS563231EVM-032 Input Voltage Ripple, I_{OUT} = 3 A

4.9 Start-Up

The TPS563231EVM-032 start-up waveform relative to V_{IN} is shown in Figure 4-10. Load = 2 Ω resistive.

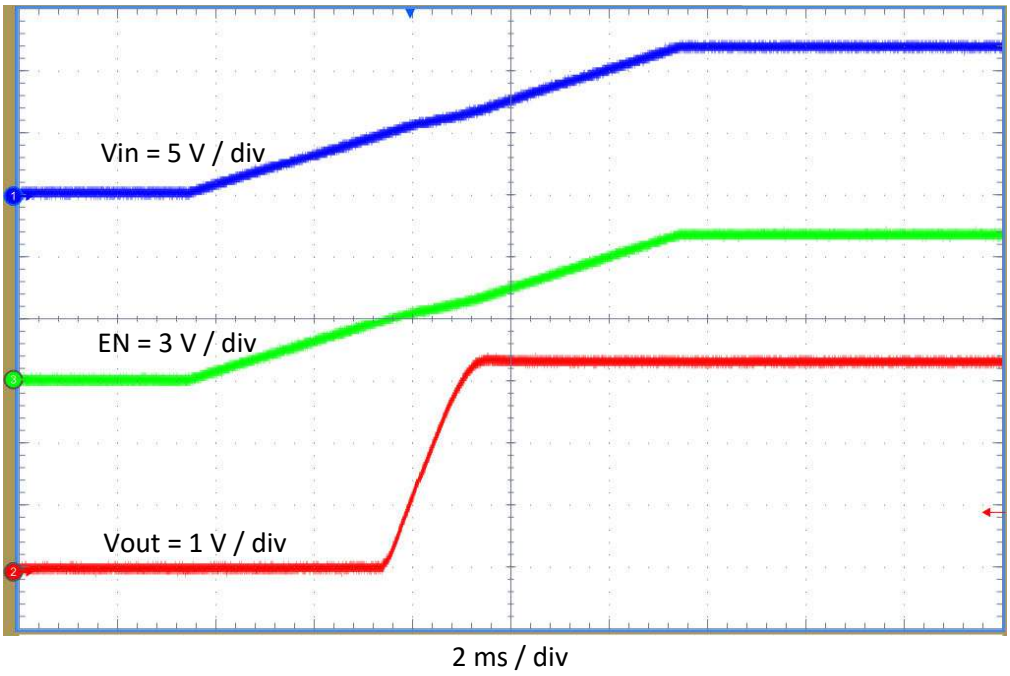

Figure 4-10. TPS563231EVM-032 Start-Up Relative to V_{IN}

The TPS563231EVM-032 start-up waveform relative to enable (EN) is shown in Figure 4-11. Load = 2 Ω resistive.

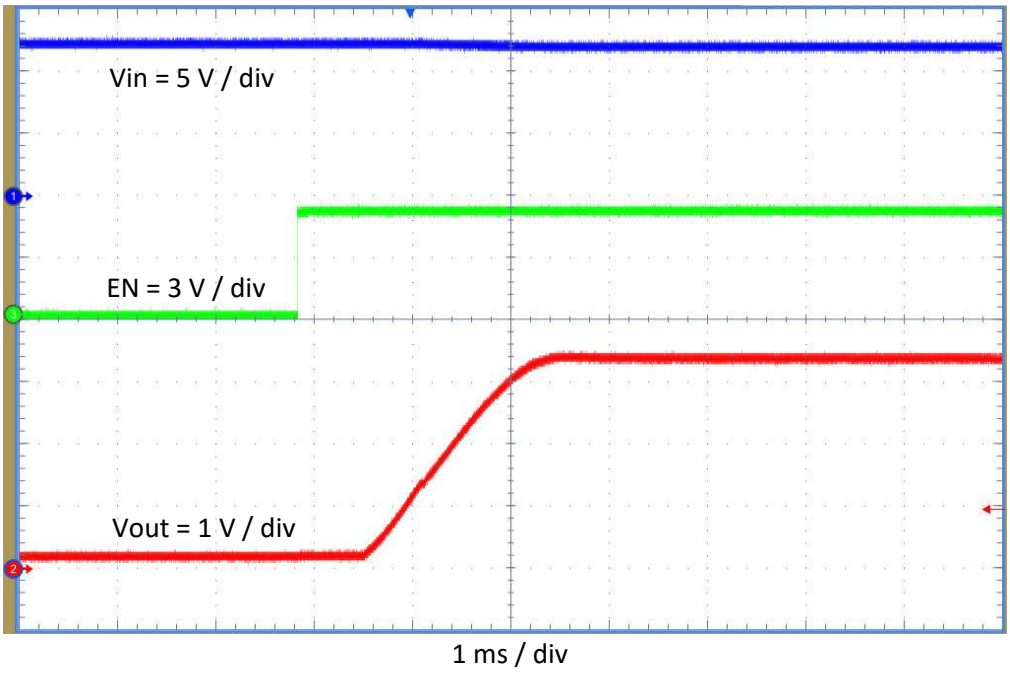

Figure 4-11. TPS563231EVM-032 Start-Up Relative to EN

4.10 Shut-Down

The TPS563231EVM-032 shut-down waveform relative to V_{IN} is shown in Figure 4-12. Load = 2 Ω resistive.

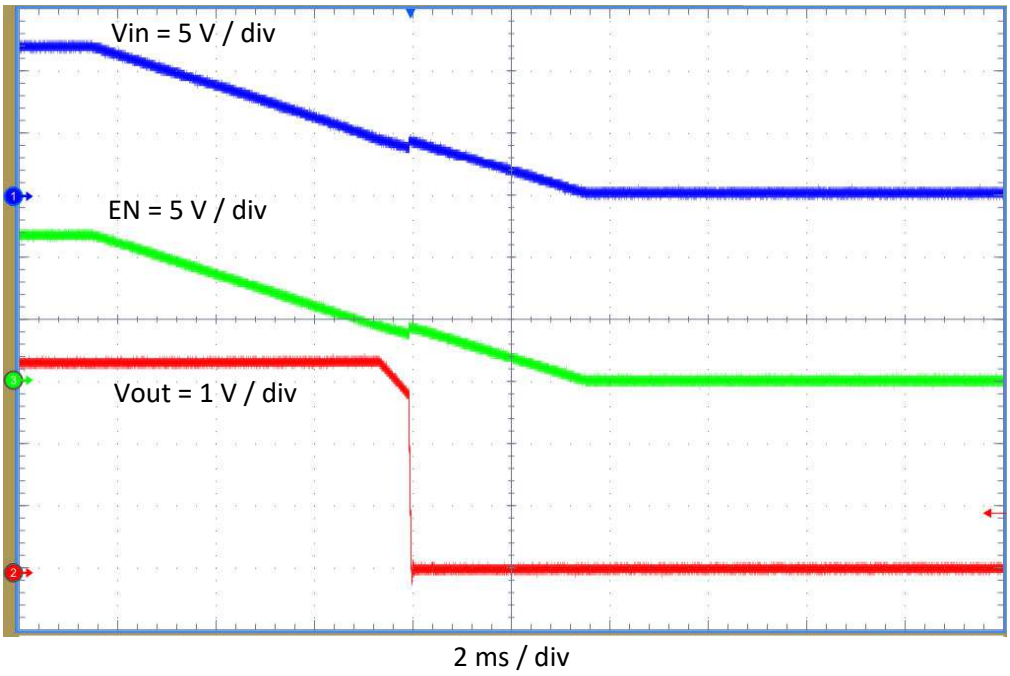

Figure 4-12. TPS563231EVM-032 Shut-Down Relative to V_{IN}

The TPS563231EVM-032 shut-down waveform relative to EN is shown in Figure 4-13. Load = 2 Ω resistive.

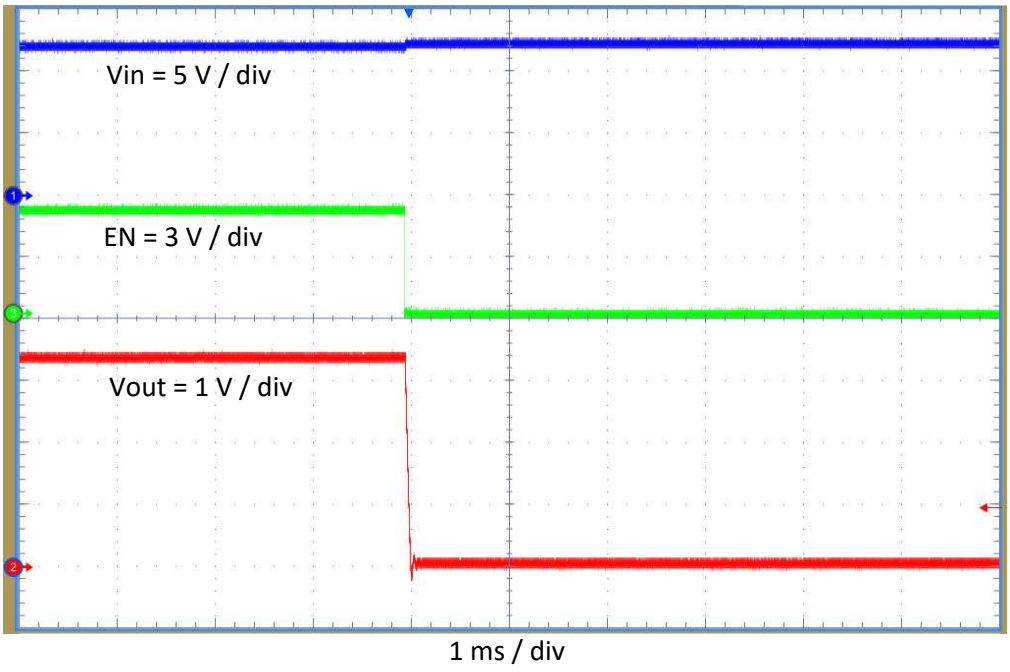

Figure 4-13. TPS563231EVM-032 Shut-Down Relative to EN

5 Board Layout

This section provides a description of the TPS563231EVM-032, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS563231EVM-032 is shown in Figure 5-1, Figure 5-2 and Figure 5-3. The top layer contains the main power traces for VIN, VOUT, and ground. Also on the top layer are connections for the pins of the TPS563231 and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitors, C1, C2, and C3 are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. The bottom layer is a ground plane along with the switching node copper fill, signal ground copper fill and the feed back trace from the point of regulation to the top of the resistor divider network.

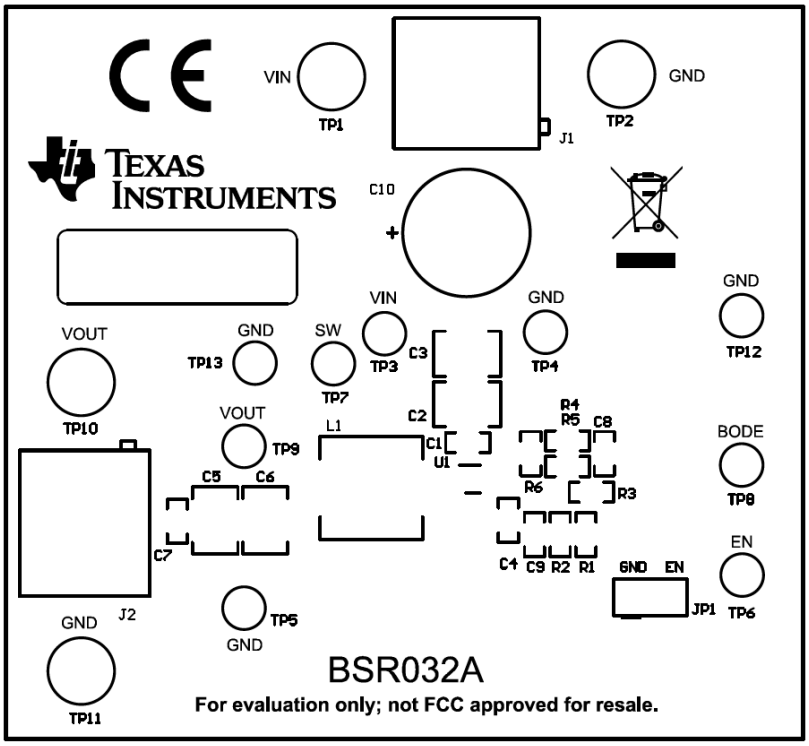

Figure 5-1. Top Assembly

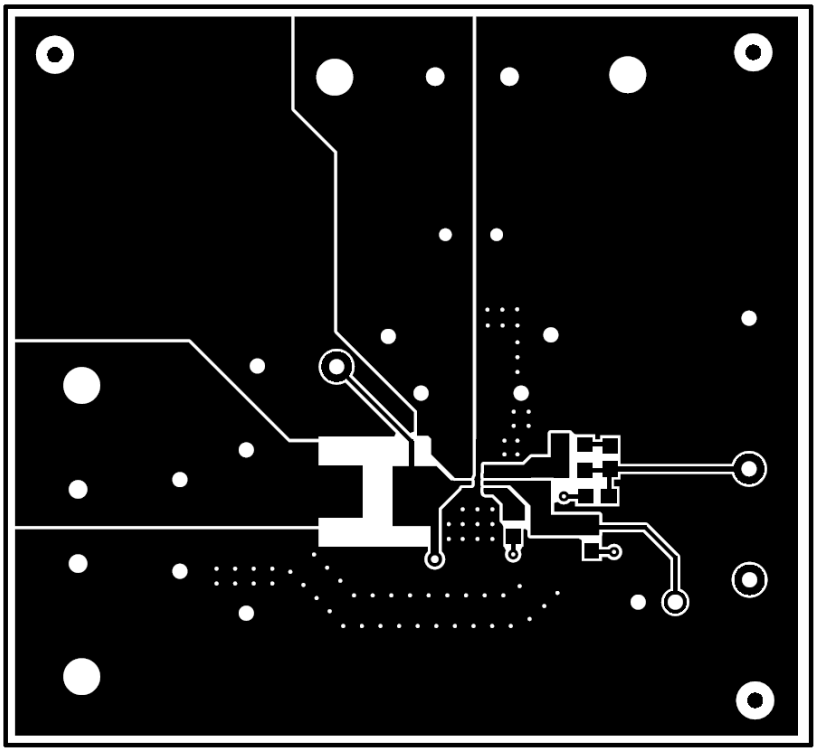

Figure 5-2. Top Layer

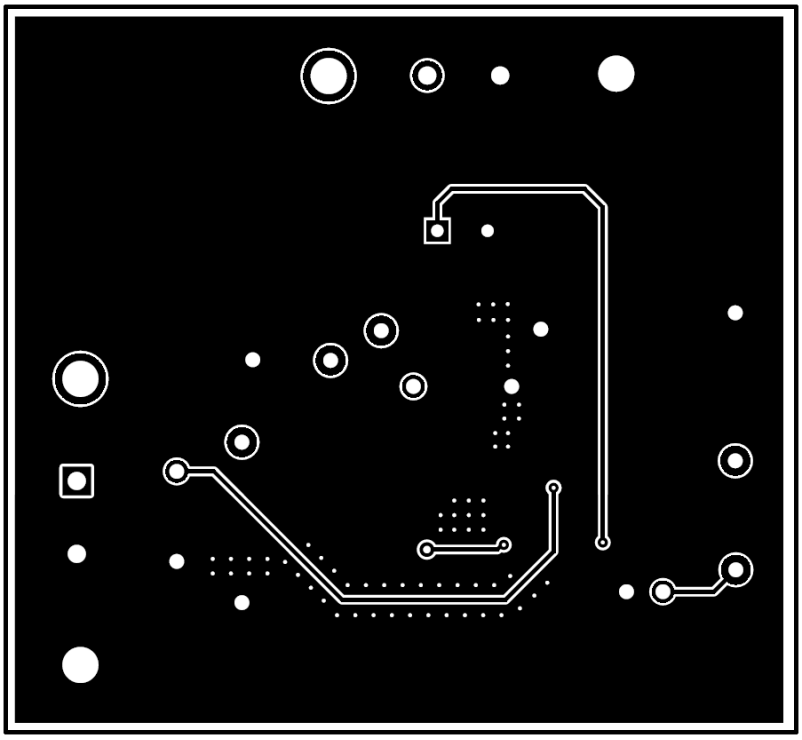

Figure 5-3. Bottom Layer

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS563231EVM-032.

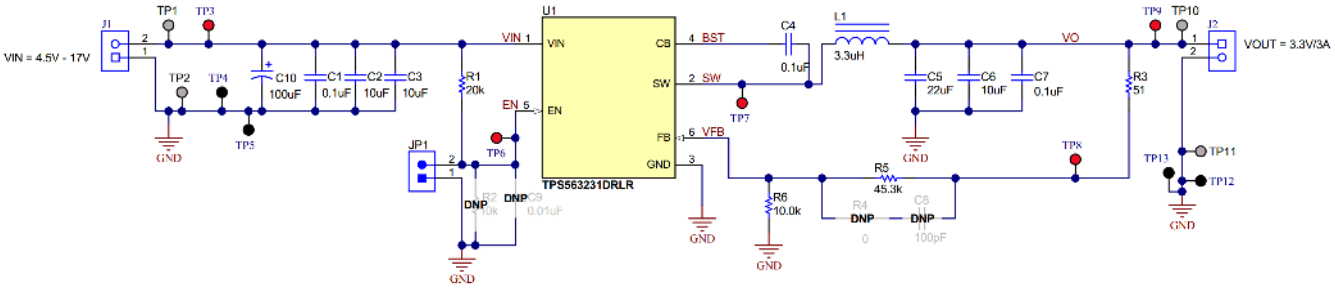

Figure 6-1. TPS563231EVM-032 Schematic Diagram

6.2 List of Materials

Table 6-1. List of Materials

DES	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
!PCB1	1	Printed Circuit Board	BSR032	Any
C1, C4,C7	3	Capacitor, ceramic, 0.1 µF, 25V, ±10%, X7R, 0603	GRM188R71E104KA01D	MuRata
C2, C3	2	Capacitor, ceramic, 10 µF, 25V, ±10%, X7R, 1210	GRM32DR71E106KA12L	MuRata
C5	1	Capacitor, ceramic, 22 µF, 10V, ±10%, X7R, 1210	GRM32ER71A226ME20L	MuRata
C6	1	Capacitor, ceramic, 10 µF, 10 V, ±10%, X7R, 1210	GRM32DR71A106KA01L	MuRata
C10	1	Capacitor, aluminum, 100 µF, 25 V, ±20%, 0.13 ohm, TH	UBT1E101MPD1 TD	Nichicon
J1, J2	2	Terminal block, 5.08 mm, 2 x 1, Brass, TH	ED120/2DS	On-Shore Technology
JP1	1	Header, 100 mil, 2 x 1, tin, TH	PEC02SAAN	Sullins Connector Solutions
L1	1	Inductor, shielded drum core, powdered iron, 3.3 µH, 6 A, 0.019 Ω, SMD	74437349033	Wurth Elektronik
LBL1	1	Thermal transfer printable labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
R1	1	Resistor, 20 kΩ, 5%, 0.1 W, 0603	CRCW060320K0JNEA	Vishay-Dale
R3	1	Resistor, 51 Ω, 5%, 0.1 W, 0603	CRCW060351R0JNEA	Vishay-Dale
R5	1	Resistor, 45.3 kΩ, 1%, 0.1 W, 0603	CRCW060345K3FKEA	Vishay-Dale
R6	1	Resistor, 10.0 kΩ, 1%, 0.1 W, 0603	CRCW060310K0FKEA	Vishay-Dale
SH-JP1	1	Shunt, 100 mil, gold plated, black	SNT-100-BK-G	Samtec
TP1, TP2, TP10, TP11	4	Terminal, turret, TH, double	1502-2	Keystone
TP3, TP6, TP7, TP8, TP9	5	Test point, miniature, red, TH	5000	Keystone
TP4, TP5, TP12, TP13	4	Test point, miniature, black, TH	5001	Keystone
U1	1	4.5-V to 17-V, 3-A 600 kHz PFM Synchronous Step- Down Converter, DRL0006A (SOT-OTHER-6)	TPS563231DRLR	Texas Instruments
C8	0	Capacitor, ceramic, 100 pF, 50 V, ±5%, C0G/NP0, 0603	GRM1885C1H101JA01D	MuRata
C9	0	Capacitor, ceramic, 0.01 µF, 50 V, ±10%, X7R, 0603	GRM188R71H103KA01D	MuRata
R2	0	Resistor, 10 kΩ, 5%, 0.1 W, 0603	CRCW060310K0JNEA	Vishay-Dale
R4	0	Resistor, 0 Ω, 5%, 0.1W, 0603	ERJ-3GEY0R00V	Panasonic

6.3 Reference

1. *TPS56323x 4.5 V to 17 V Input, 3-A Synchronous Step-Down Voltage Regulator in SOT563* data sheet (SLUSD65)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2018) to Revision B (July 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated user's guide title	2

Changes from Revision * (January 2018) to Revision A (December 2018)	Page
• Changed Figure 4-1 TPS563231EVM-032 Efficiency	6
• Changed Figure 4-2 TPS563231EVM-032 Light Load Efficiency	6
• Changed Figure 4-3 TPS563231EVM-032 Load Regulation	7
• Changed Figure 4-4 TPS563231EVM-032 Line Regulation	8

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