ACPM-7331-OR1

UMTS1900 4x4 Power Amplifier Module
(1850-1910 MHz)

Data Sheet

Description

The ACPM-7331, a Wide-band Code Division Multiple Access (WCDMA) Power Amplifier (PA), is a fully matched 10-pin surface mount module developed for WCDMA handset applications. This power amplifier module operates in the 1850-1910MHz bandwidth. The ACPM-7331 meets the stringent WCDMA linearity requirements for output power of up to 28.5dBm. The ACPM-7331 is also developed to meet HSDPA specs.

The ACPM-7331 is designed to enhance the efficiency at low and medium output power range by using 3-mode control scheme with 2 mode control pins. This provides extended talk time.

The ACPM-7331 is self contained, incorporating 50ohm input and output matching networks.

Order information

Part Number	No. of Devices	Container
ACPM-7331-OR1	1000	7"Tape and Reel
ACPM-7331-BLKR	100	BULK

Features

- Excellent Linearity
- Low quiescent current
- High Efficiency
  PAE at 28.5dBm: 33.5%
  PAE at 16dBm: 19.1%
  PAE at 8dBm: 7.0%
- 10-pin surface mounting package
  (4mmx4mmx1.1mm)
- Internal 50ohm matching networks for both RF input and output
- RoHS Compliant

Applications

- WCDMA Handset (HSDPA)

Functional Block Diagram

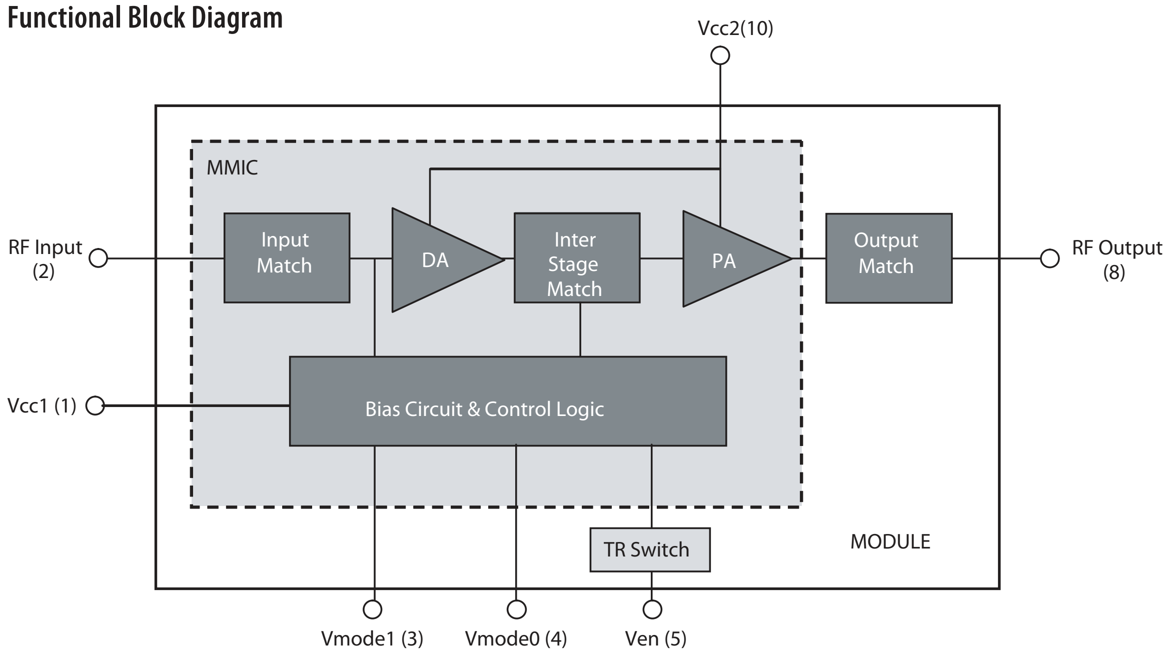


Table 1. Absolute Maximum Ratings [1]

Parameter	Symbol	Min	Nominal	Max	Unit
RF Input Power	Pin	–	–	10.0	dBm
DC Supply Voltage	Vcc	0	3.4	5.0	V
Enable Voltage	Ven	0	2.6	3.3	V
Mode Control Voltage	Vmode0	0	2.6	3.3	V
	Vmode1	0	2.6	3.3	V
Storage Temperature	Tstg	-55	–	+125	°C

Table 2. Recommended Operating Condition

Parameter	Symbol	Min	Nominal	Max	Unit
DC Supply Voltage	Vcc	3.2	3.4	4.2	V
PA Enable	Ven	1.9	2.6	2.9	V
Mode Control Voltage – High Power Mode	Vmode0 Vmode1	0 0	0 0	0.5 0.5	V V
– Mid Power Mode	Vmode0 Vmode1	1.9 0	2.6 0	2.9 0.5	V V
– Low Power Mode	Vmode0 Vmode1	1.9 1.9	1.9 1.9	2.9 2.9	V V
Operating Frequency	Fo	1850		1910	MHz
Case Operating Temperature	To	-20	25	90	°C

Table 3. Power Range Truth Table [2]

Power Mode	Symbol	Ven	Vmode0	Vmode1	Range
High Power Mode	PR3	High	Low	Low	~ 28.5dBm
Mid Power Mode	PR2	High	High	Low	~ 16dBm
Low Power Mode	PR1	High	High	High	~ 8dBm
Shut Down Mode	–	Low	–	-	–

Notes:
1. No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.
2. High (1.9–2.9V), Low (0.0V–0.5V).

Table 4. Electrical Characteristics for WCDMA Mode (Vcc=3.4V, Ven=2.6V, T=25°C, Zin/Zout=50ohm) [1]

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range		F		1850	–	1910	MHz
Gain		Gain_hi	High Power Mode, Pout=28.5 dBm	24	28		dB
		Gain_mid	Mid Power Mode, Pout=16.0 dBm	13.5	16.5		dB
		Gain_low	Low Power Mode, Pout=8.0 dBm	13	16		dB
Power Added Efficiency		PAE_hi	High Power Mode, Pout=28.5 dBm	30.1	33.5		%
		PAE_mid	Mid Power Mode, Pout=16.0 dBm	14.9	19.1		%
		PAE_low	Low Power Mode, Pout=8.0 dBm	4.9	7.0		%
Total Supply Current		Icc_hi	High Power Mode, Pout=28.5 dBm		620	690	mA
		Icc_mid	Mid Power Mode, Pout=16.0 dBm		60	77	mA
		Icc_low	Low Power Mode, Pout=8.0 dBm		26	37	mA
Quiescent Current		Iq_hi	High Power Mode		91	120	mA
		Iq_mid	Mid Power Mode		14	22	mA
		Iq_low	Low Power Mode		12	18	mA
Enable Current		Ien_hi	High Power Mode		0.18	1	mA
		Ien_mid	Mid Power Mode		0.18	1	mA
		Ien_low	Low Power Mode		0.18	1	mA
Control Current		Imode0_mid	Mid Power Mode		0.4	1	mA
		Imode1_low	Low Power Mode		0.18	1	mA
		Imode0_low	Low Power Mode		0.4	1	mA
Total Current in Power-down mode		Ipd	Ven=0V		0.2	5	µA
Adjacent Channel Leakage Ratio [2]	5 MHz offset 10 MHz offset	ACLR1_hi ACLR2_hi	High Power Mode, Pout=28.5 dBm		-40 -54	-37 -46	dBc dBc
	5 MHz offset 10 MHz offset	ACLR1_mid ACLR2_mid	Mid Power Mode, Pout=16.0 dBm		-41 -56	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	ACLR1_low ACLR2_low	Low Power Mode, Pout=8.0 dBm		-41 -57	-37 -46	dBc dBc
Harmonic Suppression	Second Third	2f0 3f0	High Power Mode, Pout=28.5 dBm		-35 -70	-30 -50	dBc dBc
Input VSWR	VSWR				1.4:1	2.0:1	
Stability (Spurious Output)		S	VSWR 6:1, All phase			-60	dBc
Noise Power in Rx Band		RxBN	High Power Mode, Pout=28.5 dBm		-136	-133	dBm/Hz
Phase Discontinuity		PDlow_mid PDmid_high	low power mode<-->mid power mode, at Pout=8dBm mid power mode<-->high power mode, at Pout=16dBm			10 15	Deg Deg
Ruggedness		Ru	Pout<28.5dBm, Pin<10dBm, All phase High Power Mode			10:1	VSWR

Notes:
1. Electrical characteristics are specified under WCDMA modulated (3GPP Uplink DPCCH + 1DPDCH) signal
2. ACP is expressed as a ratio of total adjacent power to signal power, both with 3.84MHz bandwidth at specified offsets.

Table 5. Electrical Characteristics for HSDPA Mode (Vcc=3.4V, Ven=2.6V, T=25°C, Zin/Zout=50ohm) [1]

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range		F		1850	–	1910	MHz
Gain		Gain_hih	High Power Mode, Pout=28.5 dBm	24	28		dB
		Gain_midh	Mid Power Mode, Pout=16.0 dBm	13.5	16.5		dB
		Gain_lowh	Low Power Mode, Pout=8.0 dBm	13	16		dB
Power Added Efficiency		PAE_hih	High Power Mode, Pout=28.5 dBm	31.0	34.6		%
		PAE_midh	Mid Power Mode, Pout=16.0 dBm	15.3	19.7		%
		PAE_lowh	Low Power Mode, Pout=8.0 dBm	4.9	7.0		%
Total Supply Current		Icc_hih	High Power Mode, Pout=28.5 dBm		600	670	mA
		Icc_midh	Mid Power Mode, Pout=16.0 dBm		58	75	mA
		Icc_lowh	Low Power Mode, Pout=8.0 dBm		26	37	mA
Adjacent Channel Leakage Ratio [2]	5 MHz offset 10 MHz offset	ACLR1_hih ACLR2_hih	High Power Mode, Pout=28.5 dBm	–	-39 -54	-37 -46	dBc dBc
	5 MHz offset 10 MHz offset	ACLR1_midh ACLR2_midh	Mid Power Mode, Pout=16.0 dBm	–	-40 -56	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	ACLR1_lowh ACLR2_lowh	Low Power Mode, Pout=8.0 dBm	–	-40 -56	-37 -46	dBc dBc

Notes:
1. Electrical characteristics are specified under HSDPA modulated Up-Link signal (DPCCH/DPDCH=12/15, HS-DPCCH/DPDCH=15/15)
2. ACP is expressed as a ratio of total adjacent power to signal power, both with 3.84MHz bandwidth at specified offsets

Characteristics Data (WCDMA, Vcc=3.4V, Ven=2.6V, T=25°C, CZin/Zout=50ohm)

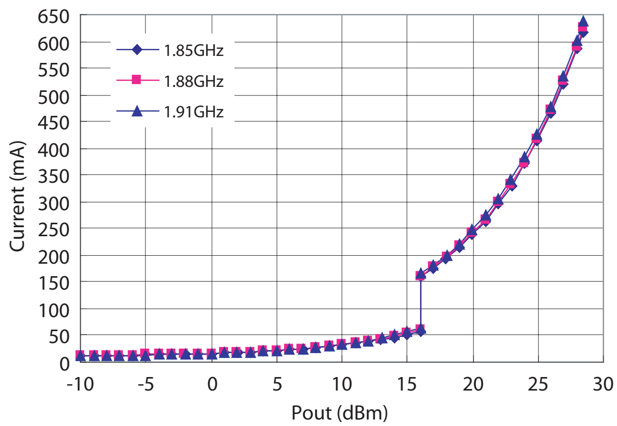


Figure 1. Total Current vs. Output Power

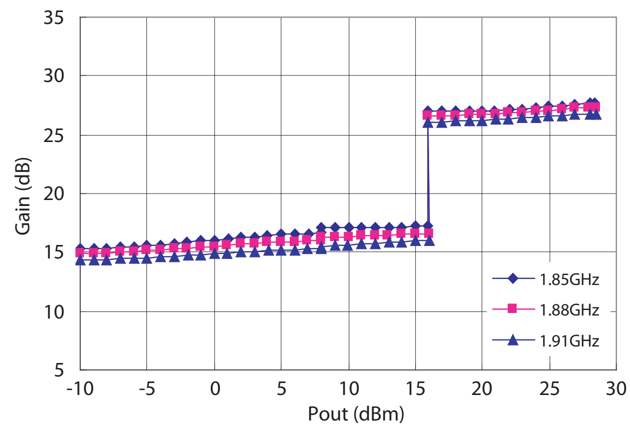


Figure 2. Gain vs. Output Power

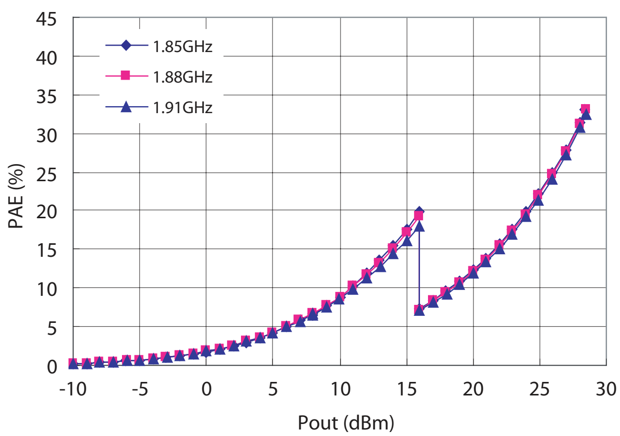


Figure 3. Power Added Efficiency vs. Output Power

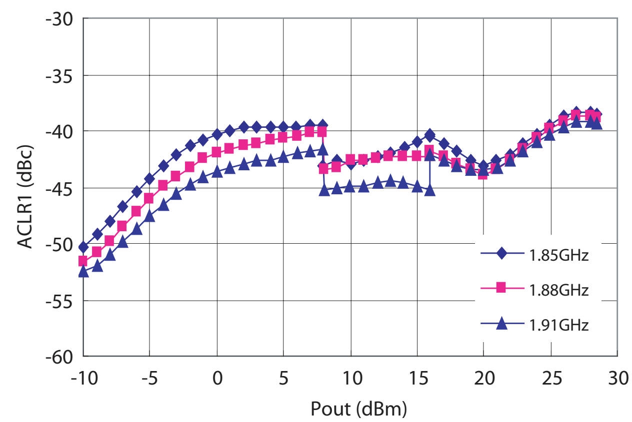


Figure 4. Adjacent Channel Leakage Ratio 1 vs. Output Power

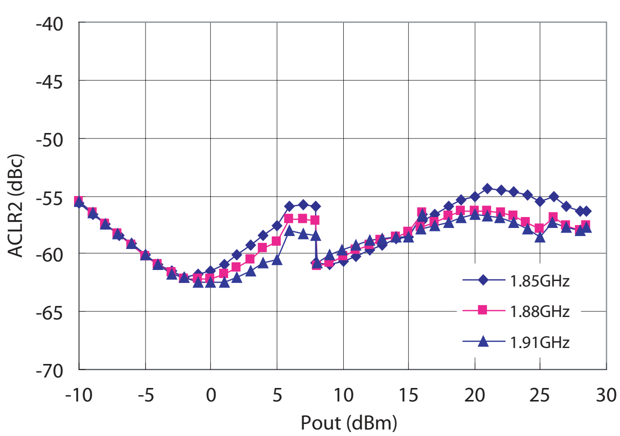


Figure 5. Adjacent Channel Leakage Ratio 2 vs. Output Power

Characteristics Data (HSDPA, Vcc=3.4V, Ven=2.6V, T=25°C, Zin/Zout=50ohm)

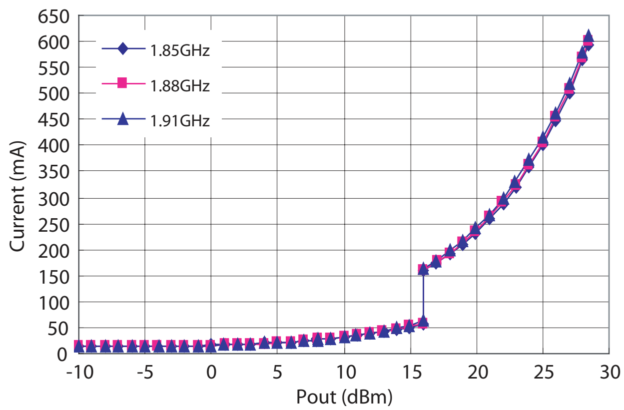


Figure 6. Total Current vs. Output Power

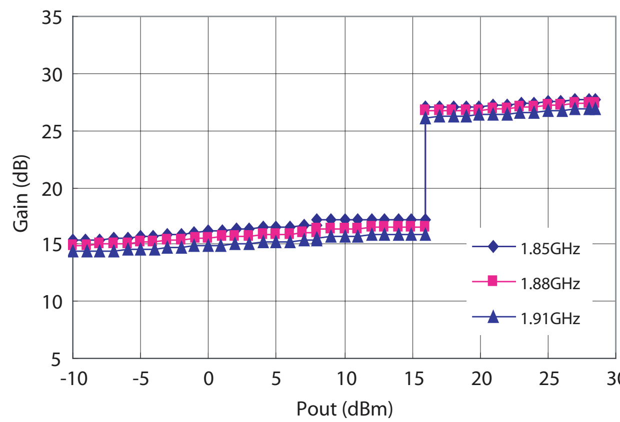


Figure 7. Gain vs. Output Power

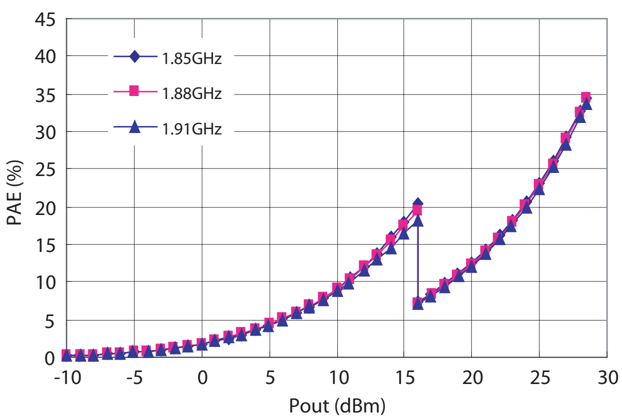


Figure 8. Power Added Efficiency vs. Output Power

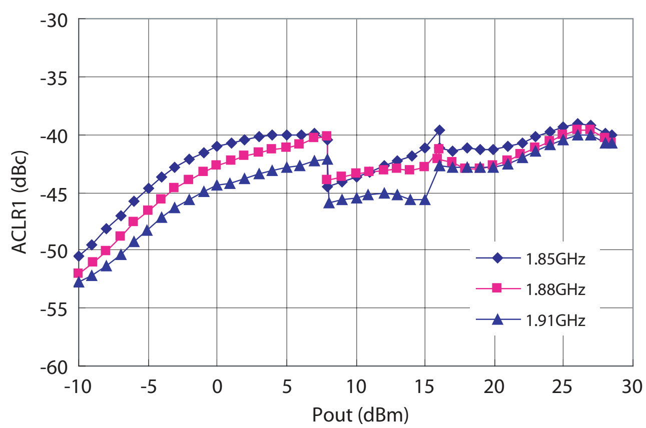


Figure 9. Adjacent Channel Leakage Ratio 1 vs. Output Power

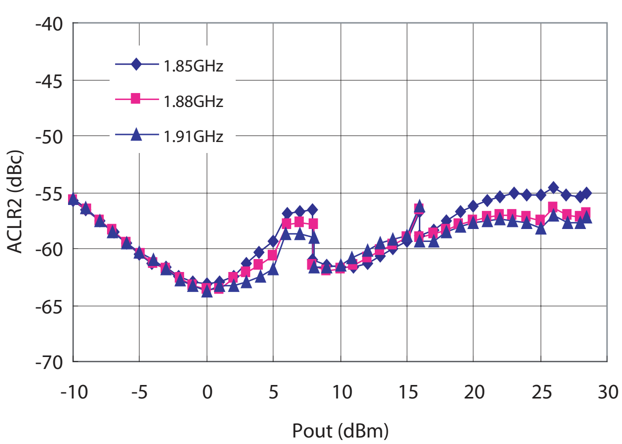


Figure 10. Adjacent Channel Leakage Ratio 2 vs. Output Power

Evaluation Board Description

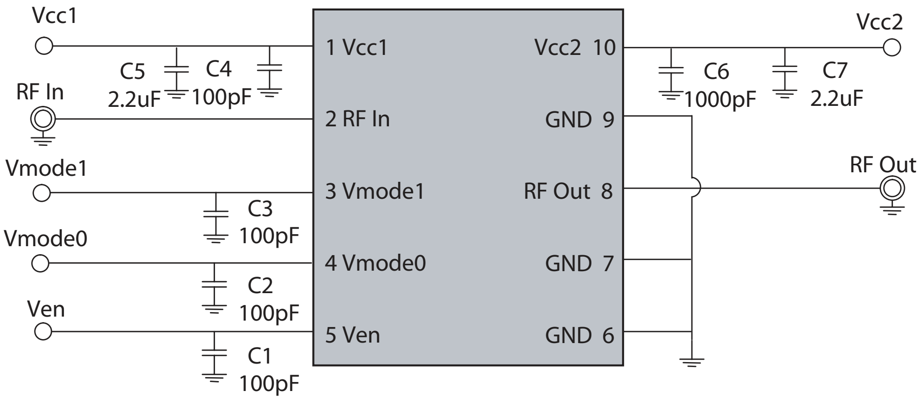


Figure 11. Evaluation Board Schematic

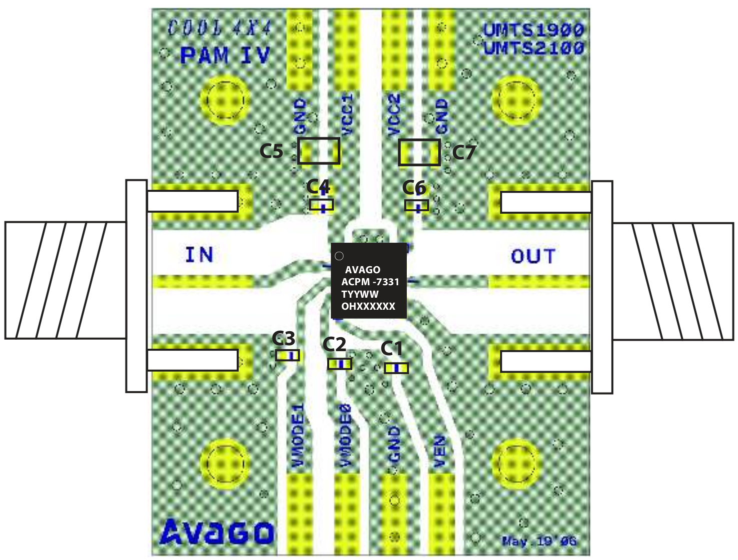
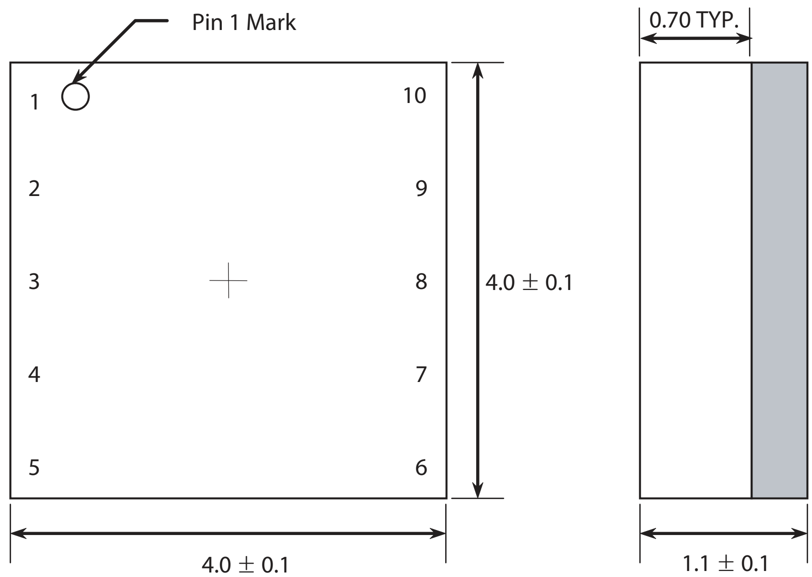


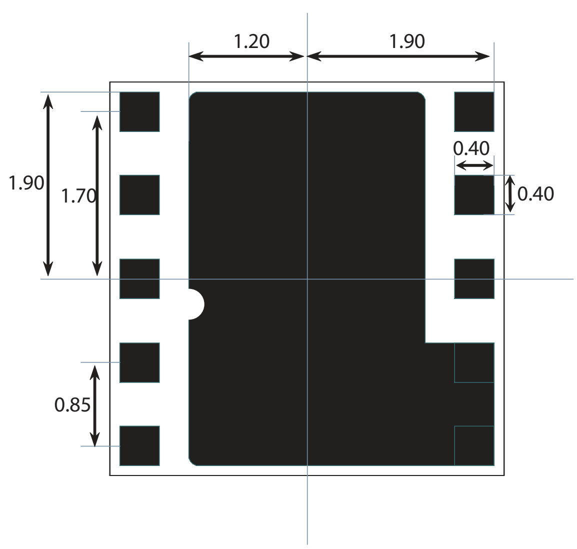
Figure 12. Evaluation Board Assembly Diagram

Package Dimensions and Pin Descriptions



TOP VIEW

SIDE VIEW



X-RAY BOTTOM VIEW

Pin #	Name	Description
1	Vcc1	Supply Voltage
2	RF In	RF Input
3	Vmode1	Control Voltage
4	Vmode0	Control Voltage
5	Ven	Enable Voltage
6	GND	Ground
7	GND	Ground
8	RF Out	RF Output
9	GND	Ground
10	Vcc2	Supply Voltage

PIN DESCRIPTIONS

Figure 13. Package Dimensional Drawing and Pin Descriptions (All dimensions are in millimeters)

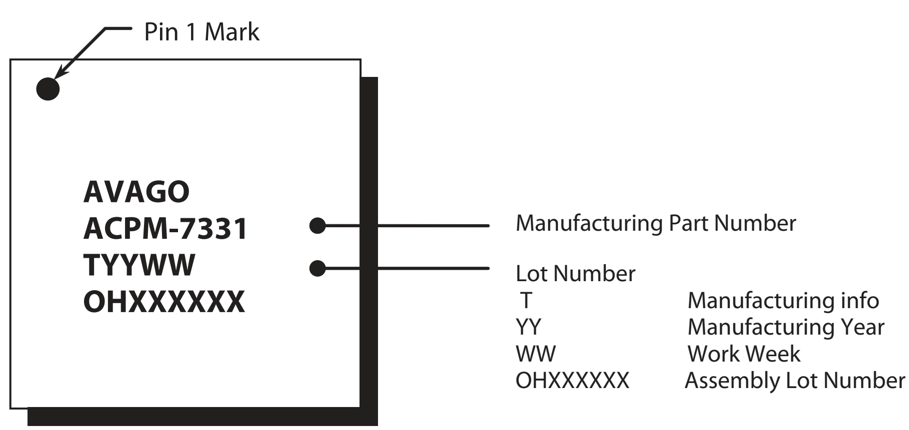


Figure 14. Marking Specifications

PCB Design Guidelines

The recommended ACPM-7331 PCB land pattern is shown in Figure 15 and Figure 16. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

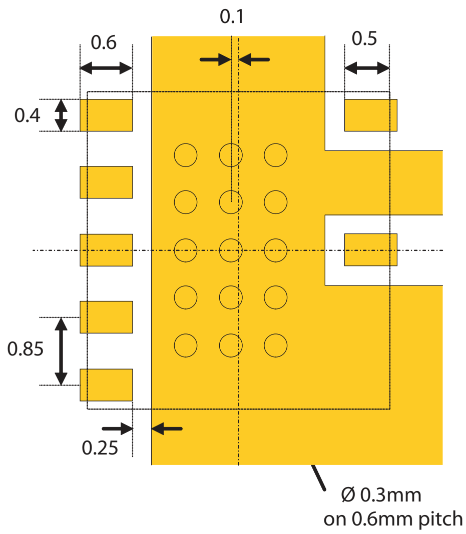


Figure 15. Metallization

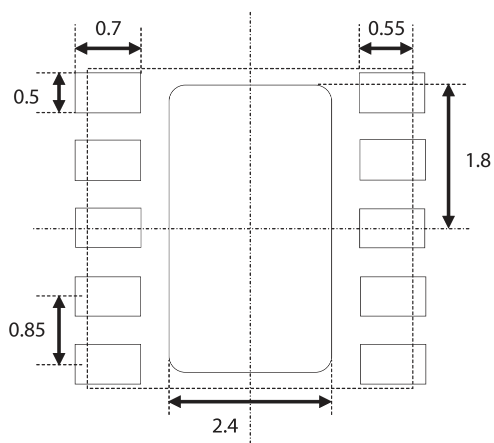


Figure 16. Solder Mask Opening

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 17. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.10mm(4mils)or 0.127mm(5mils) thick stainless steel which is capable of producing the required fine stencil outline.

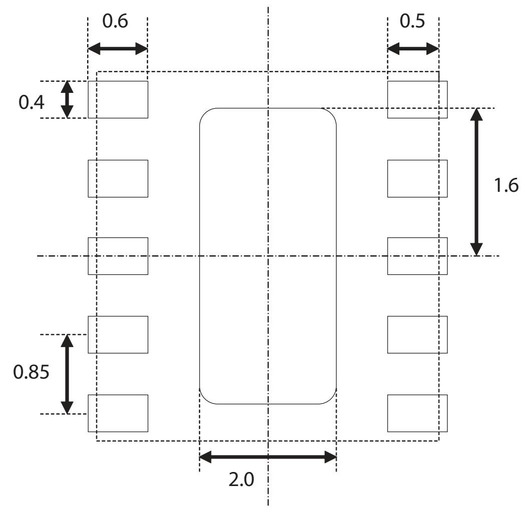
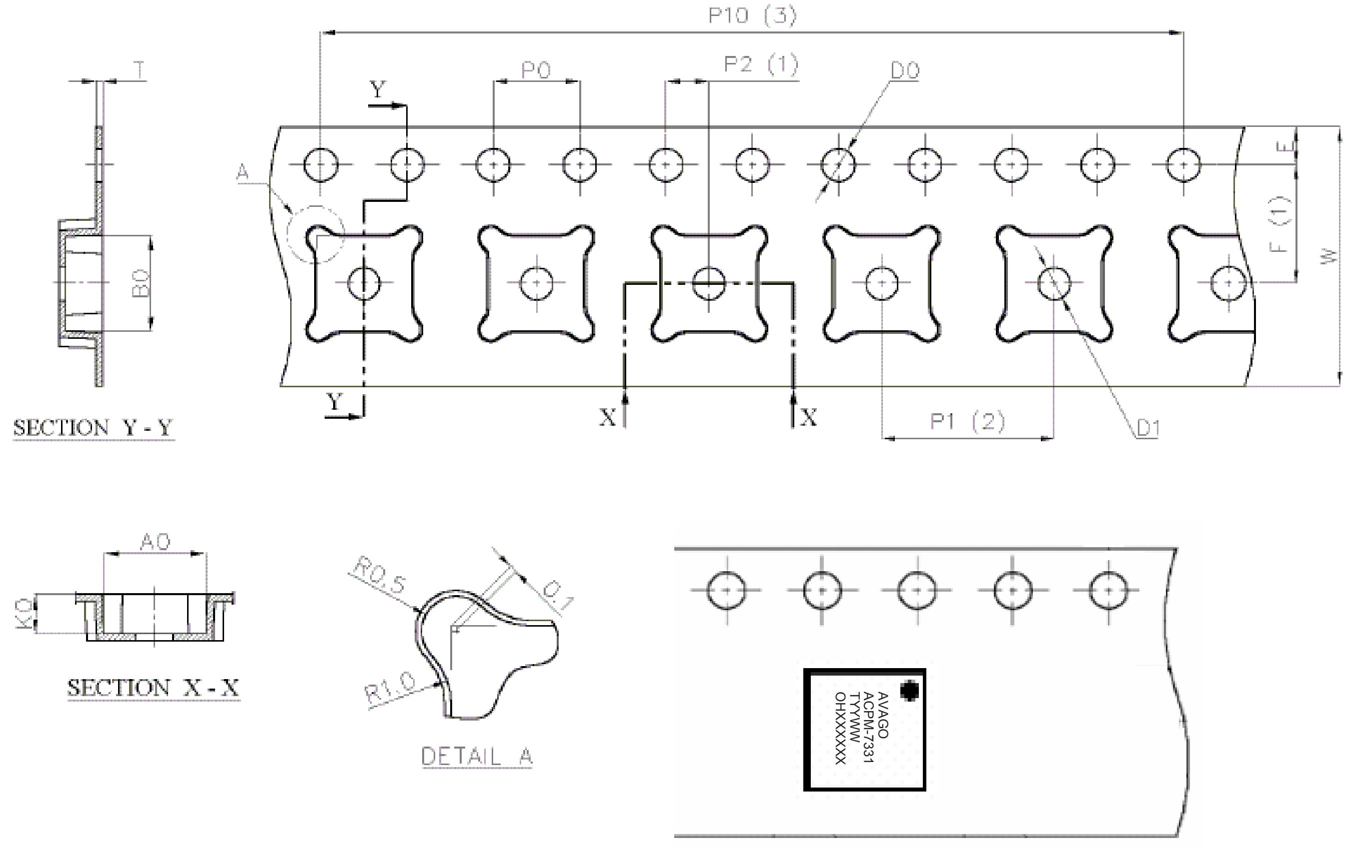


Figure 17. Solder Paste Stencil Aperture

Tape and Reel Information



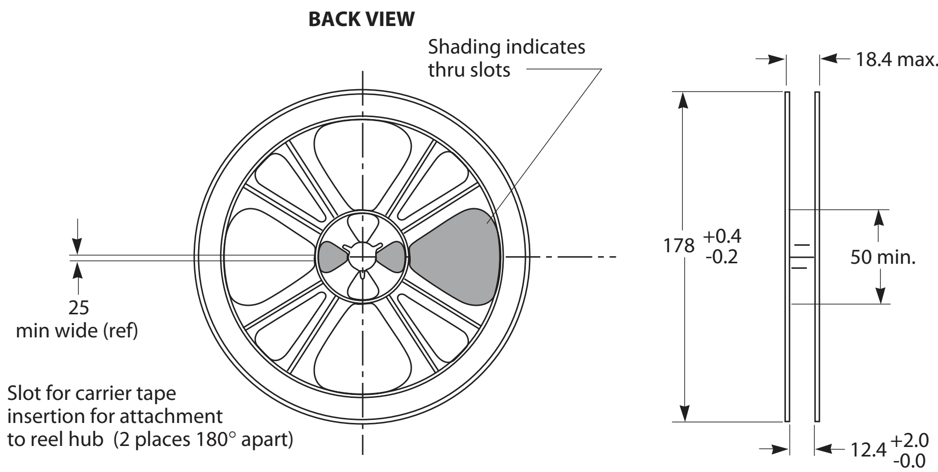
Dimension List

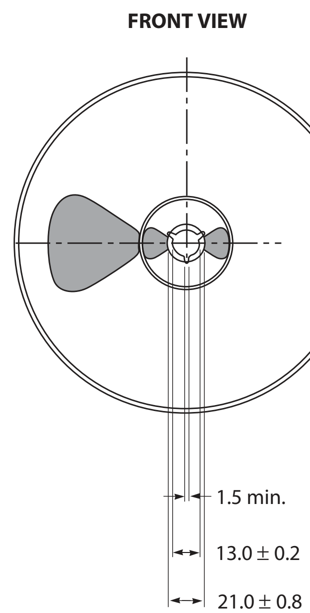
Dimension	Millimeter
A0	4.40±0.10
B0	4.40±0.10
K0	1.70±0.10
D0	1.55±0.05
D1	1.60±0.10
P0	4.00±0.10
P1	8.00±0.10

Dimension	Millimeter
P2	2.00±0.05
P10	40.00±0.20
E	1.75±0.10
F	5.50±0.05
W	12.00±0.30
T	0.30±0.05

Figure 18. Tape and Reel Format – 4 mm x 4 mm.

Reel Drawing





NOTES:
1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipme of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Figure 19. Plastic Reel Format (all dimensions are in millimeters)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

ACPM-7331 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the ACPM-7331 is targeted at 260°C +0/-5°C. Figure 20 and Table 8 show typical SMT profile for maximum temperature of 260 +0/-5°C.

Table 6. ESD Classification

Pin #	Name	Description	HBM	CDM	Classification
1	Vcc1	Supply Voltage	± 2000V	± 200V	Class 2
2	RF In	RF Input	± 2000V	± 200V	Class 2
3	Vmode1	Control Voltage	± 2000V	± 200V	Class 2
4	Vmode0	Control Voltage	± 2000V	± 200V	Class 2
5	Ven	Enable Voltage	± 2000V	± 200V	Class 2
6	GND	Ground	± 2000V	± 200V	Class 2
7	GND	Ground	± 2000V	± 200V	Class 2
8	RF Out	RF Output	± 2000V	± 200V	Class 2
9	GND	Ground	± 2000V	± 200V	Class 2
10	Vcc2	Supply Voltage	± 2000V	± 200V	Class 2

Note :
1. Module products should be considered extremely ESD sensitive.

Table 7. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30°C/60% RH or as stated
1	Unlimited at =< 30oC/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :
1. The MSL Level is marked on the MSL Label on each shipping bag.

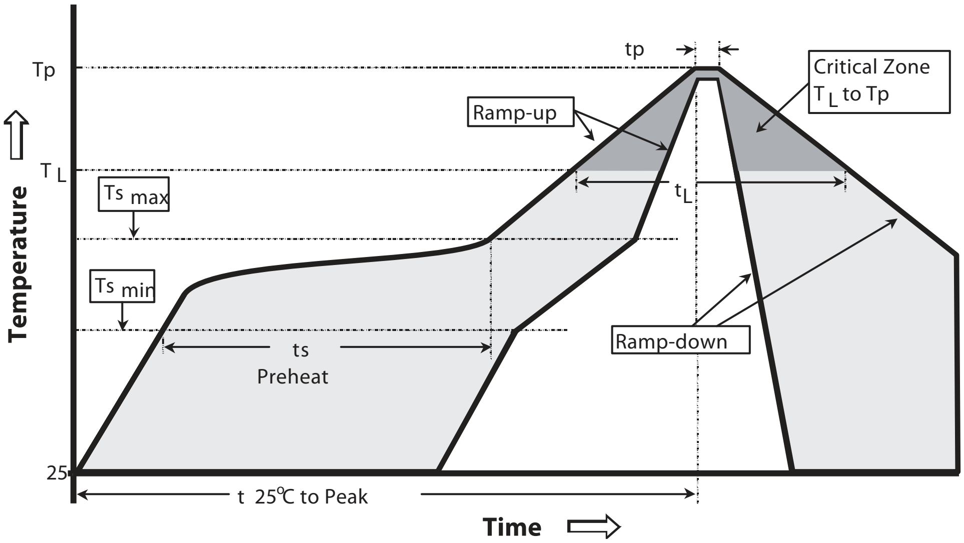


Figure 20. Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Table 8. Typical SMT Reflow Profile for Maximum Temperature = 260+0 / -5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3°C/sec max	3°C /sec max
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100°C 150°C 60-120 sec	 150°C 200°C 60-180 sec
Tsmax to TL - Ramp-up Rate		 3°C /sec max
Time maintained above: - Temperature (TL) - Time (TL)	 183°C 60-150 sec	 217°C 60-150 sec
Peak temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6°C /sec max	6°C /sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30°C and 60% RH.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 andIPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 7. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table 9 lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°C, 25°C, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 9:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s (this used largest known Diffusivity @ 30°C).

Table 9. Recommended Equivalent Total Floor Life (days) @ 20 °C , 25°C & 30°C For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)

Maximum Percent Relative Humidity

Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm Including PQFPs >84 pin, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30°
		∞	∞	∞	78	53	42	36	14	10	8	25°
		∞	∞	∞	103	69	57	47	19	13	10	20°
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30°
		∞	∞	13	11	10	9	9	7	6	5	25°
		∞	∞	17	14	13	12	12	10	8	7	20°
	Level 4	∞	5	4	4	4	3	3	3	2	2	30°
		∞	6	5	5	5	5	4	3	3	3	25°
		∞	8	7	7	7	7	6	5	4	4	20°
	Level 5	∞	4	3	3	2	2	2	2	1	1	30°
		∞	5	5	4	4	3	3	2	2	2	25°
		∞	7	7	6	5	5	4	3	2	3	20°
	Level 5a	∞	2	1	1	1	1	1	1	1	1	30°
		∞	3	2	2	2	2	2	1	1	1	25°
		∞	5	4	3	3	3	2	2	2	2	20°
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pin SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30°
		∞	∞	∞	∞	148	51	37	6	4	3	25°
		∞	∞	∞	∞	∞	69	49	8	5	4	20°
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30°
		∞	∞	25	15	12	10	9	5	3	3	25°
		∞	∞	32	19	15	13	12	7	5	4	20°
	Level 4	∞	7	5	4	4	3	3	2	2	1	30°
		∞	9	7	5	5	4	4	3	2	2	25°
		∞	11	9	7	6	6	5	4	3	3	20°
	Level 5	∞	4	3	3	2	2	2	1	1	1	30°
		∞	5	4	3	3	3	3	2	1	1	25°
		∞	6	5	5	4	4	4	3	3	2	20°
	Level 5a	∞	2	1	1	1	1	1	1	0.5	0.5	30°
		∞	2	2	2	2	2	2	1	1	1	25°
		∞	3	2	2	2	2	2	2	2	1	20°
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs or All BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	28	1	1	1	30°
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°
	Level 3	∞	∞	∞	∞	∞	11	7	1	1	1	30°
		∞	∞	∞	∞	∞	14	10	2	1	1	25°
		∞	∞	∞	∞	∞	20	13	2	2	1	20°
	Level 4	∞	∞	∞	9	5	4	3	1	1	1	30°
		∞	∞	∞	12	7	5	4	2	1	1	25°
		∞	∞	∞	17	9	7	6	2	2	1	20°
	Level 5	∞	∞	13	5	3	2	2	1	1	1	30°
		∞	∞	18	6	4	3	3	2	1	1	25°
		∞	∞	26	8	6	5	4	2	2	1	20°
	Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30°
		∞	13	5	3	2	2	2	1	1	1	25°
		∞	18	6	4	3	2	2	2	2	1	20°

AV01-0608EN - November 21, 2006