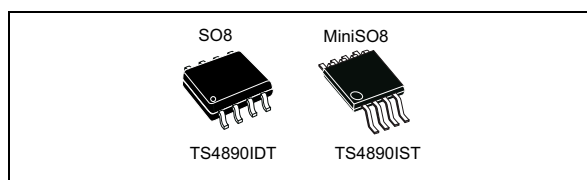


Rail-to-rail output 1 W audio power amplifier with standby mode active low

Datasheet - production data



The unity-gain stable amplifier can be configured by external gain setting resistors.

Table 1. Device summary⁽¹⁾

Part number	Temp. range	Marking
TS4890IDT	-40 + 85 °C	4890
TS4890IST		4890I

1. Available in tape and reel only.

Features

- Operating from $V_{CC} = 2.2\text{ V}$ to 5.5 V
- 1 W rail-to-rail output power @ $V_{CC} = 5\text{ V}$, THD=1%, $f=1\text{ kHz}$, with $8\ \Omega$ load
- Ultra low consumption in standby mode (10 nA)
- 75 dB PSSR @ 217 Hz from 5 to 2.2 V
- Pop and click reduction circuitry
- Ultra low distortion (0.1%)
- Unity gain stable
- Available in SO8 and MiniSO8

Applications

- Mobile phones (cellular/cordless)
- Laptop/notebook computers
- PDAs
- Portable audio devices

Description

The TS4890 is an audio power amplifier, which can deliver 1 W of continuous RMS output power into 8 Ω load @ 5 V.

This audio amplifier shows 0.1% distortion level (THD) from a 5 V supply for a $P_{out} = 250\text{ mW}$ RMS. An external standby mode control reduces the supply current to less than 10 nA. An internal thermal shutdown protection is also provided.

The TS4890 has been designed for high quality audio applications such as mobile phones, and to minimize the number of external components.

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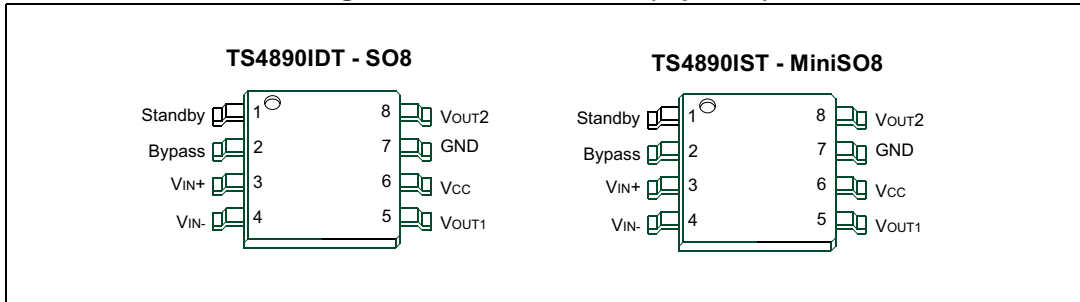
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1 General information

1.1 Pin connections (top view)

Figure 1. Pin connections (top view)



1.2 Typical application schematic

Figure 2. Typical application schematic

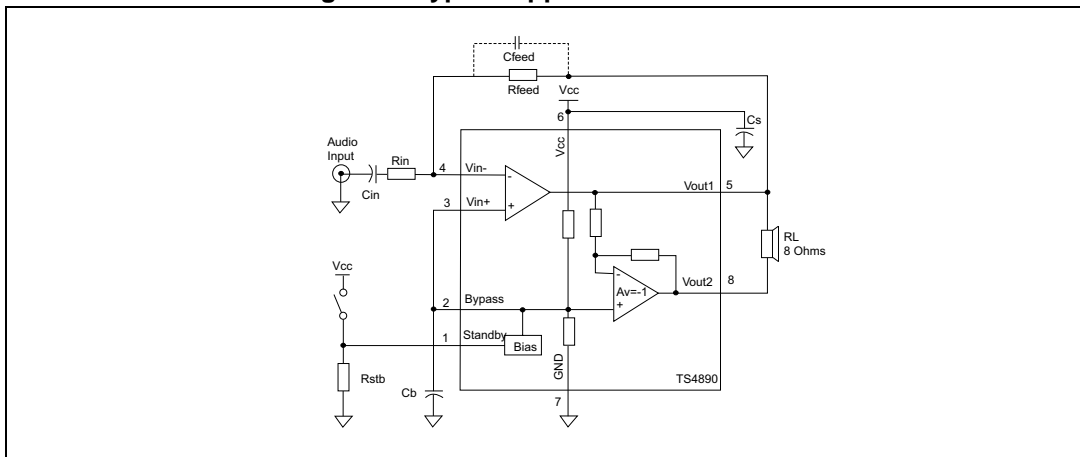


Table 2. Component description

Components	Functional description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin ($f_c = 1 / (2 \times \pi \times R_{in} \times C_{in})$)
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply bypass capacitor which provides power supply filtering
Cb	Bypass pin capacitor which provides half supply filtering
Cfeed	Low pass filter capacitor allowing the high frequency to be cut (low pass filter cut-off frequency $1 / (2 \times \pi \times R_{feed} \times C_{feed})$)

Table 2. Component description

Components	Functional description
Rstb	Pull-down resistor which fixes the right supply level on the standby pin
Gv	Closed loop gain in BTL configuration = $2 \times (R_{feed} / R_{in})$

2 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_i	Input voltage ⁽²⁾	GND to V_{CC}	
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction to ambient ⁽³⁾	175 (SO8)	°C/W
		215 (MiniSO8)	
P_d	Power dissipation ⁽⁴⁾	See	W
ESD	Human body model	2	kV
	Machine model	200	V
	Latch-up immunity	Class A	
	Lead temperature (soldering, 10 s)	260	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed $V_{CC} + 0.3 \text{ V} / \text{GND} - 0.3 \text{ V}$.
3. The device is protected in case of overtemperature by a thermal shutdown active @ 150 °C.
4. Exceeding the power derating curves during a long period may involve abnormal working of the device.

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
V_{ICM}	Common mode input voltage range	GND + 1 V to V_{CC}	
V_{STB}	Standby voltage input: device on device off	$1.5 \leq V_{STB} \leq V_{CC}$ $\text{GND} \leq V_{STB} \leq 0.5$	
R_L	Load resistor	4 -32	Ω
R_{thja}	Thermal resistance junction-to-ambient ⁽¹⁾	150 (SO8)	°C/W
		190 (MiniSO8)	

1. This thermal resistance can be reduced with a suitable PCB layout (see Fig. 24).

3 Electrical characteristics

$V_{CC} = +5\text{ V}$, $GND = 0\text{ V}$, $T_{amb} = 25\text{ °C}$ (unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current no input signal, no load		6	8	mA
$I_{STANDBY}$	Standby current ⁽¹⁾ , no input signal, $V_{stdby} = GND$, $R_L = 8\ \Omega$		10	1000	nA
V_{oo}	Output offset voltage no input signal, $R_L = 8\ \Omega$		5	20	mV
P_o	Output power THD = 1% max., $f = 1\text{ kHz}$, $R_L = 8\ \Omega$		1		W
THD + N	Total harmonic distortion + noise $P_o = 250\text{ mW RMS}$, $G_v = 2$, $20\text{ Hz} < f < 20\text{ kHz}$, $R_L = 8\ \Omega$		0.15		%
PSRR	Power supply rejection ratio ⁽²⁾ $f = 217\text{ Hz}$, $R_L = 8\ \Omega$, $R_{Feed} = 22\text{ k}\Omega$, $V_{ripple} = 200\text{ mV RMS}$		77		dB
ϕ_M	Phase margin at unity gain $R_L = 8\ \Omega$, $C_L = 500\text{ pF}$		70		Degrees
GM	Gain margin $R_L = 8\ \Omega$, $C_L = 500\text{ pF}$		20		dB
GBP	Gain bandwidth product $R_L = 8\ \Omega$		2		MHz

1. Standby mode is active when V_{stdby} is tied to GND.

2. Dynamic measurements - $20 \cdot \log(\text{RMS}(V_{out})/\text{RMS}(V_{ripple}))$. V_{ripple} is the superimposed sinus signal to V_{CC} @ $f = 217\text{ Hz}$.

Table 6. Electrical characteristics ($V_{CC} = +3.3\text{ V}$, $GND = 0\text{ V}$, $T_{amb} = 25\text{ °C}$, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current no input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby current ⁽¹⁾ , no input signal, $V_{stdby} = GND$, $R_L = 8\ \Omega$		10	1000	nA
V_{oo}	Output offset voltage no input signal, $R_L = 8\ \Omega$		5	20	mV
P_o	Output power THD = 1% max., $f = 1\text{ kHz}$, $R_L = 8\ \Omega$		450		mW

Table 6. Electrical characteristics ($V_{CC}= +3.3\text{ V}$, $GND= 0\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
THD + N	Total harmonic distortion + noise $P_o = 250\text{ mW RMS}$, $G_v = 2$, $20\text{ Hz} < f < 20\text{ kHz}$, $R_L = 8\ \Omega$		0.15		%
PSRR	Power supply rejection ratio ⁽²⁾ $f = 217\text{ Hz}$, $R_L = 8\ \Omega$, $R_{Feed} = 22\text{ k}\Omega$, $V_{ripple} = 200\text{ mV RMS}$		77		dB
ϕ_M	Phase margin at unity gain $R_L = 8\ \Omega$, $C_L = 500\text{ pF}$		70		Degrees
GM	Gain margin $R_L = 8\ \Omega$, $C_L = 500\text{ pF}$		20		dB
GBP	Gain bandwidth product $R_L = 8\ \Omega$		2		MHz

- Standby mode is active when V_{stbly} is tied to GND.
- Dynamic measurements - $20 \cdot \log(\text{RMS}(V_{out})/\text{RMS}(V_{ripple}))$. V_{ripple} is the superimposed sinus signal to V_{CC} @ $f = 217\text{ Hz}$.

Table 7. Electrical characteristics ($V_{CC}= +2.6\text{ V}$, $GND= 0\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current no input signal, no load		5	8	mA
$I_{STANDBY}$	Standby current ⁽¹⁾ , no input signal, $V_{stbly} = GND$, $R_L = 8\ \Omega$		10	1000	nA
V_{oo}	Output offset voltage no input signal, $R_L = 8\ \Omega$		5	20	mV
P_o	Output power THD = 1% max., $f = 1\text{ kHz}$, $R_L = 8\ \Omega$		260		mW
THD + N	Total harmonic distortion + noise $P_o = 200\text{ mW RMS}$, $G_v = 2$, $20\text{ Hz} < f < 20\text{ kHz}$, $R_L = 8\ \Omega$		0.15		%
PSRR	Power supply rejection ratio ⁽²⁾ $f = 217\text{ Hz}$, $R_L = 8\ \Omega$, $R_{Feed} = 22\text{ k}\Omega$, $V_{ripple} = 200\text{ mV RMS}$		77		dB
ϕ_M	Phase margin at unity gain $R_L = 8\ \Omega$, $C_L = 500\text{ pF}$		70		Degrees
GM	Gain margin $R_L = 8\ \Omega$, $C_L = 500\text{ pF}$		20		dB
GBP	Gain bandwidth product $R_L = 8\ \Omega$		2		MHz

1. Standby mode is active when V_{stdby} is tied to GND.
2. Dynamic measurements - $20 \cdot \log(\text{RMS}(V_{\text{out}})/\text{RMS}(V_{\text{ripple}}))$. V_{ripple} is the superimposed sinus signal to V_{CC} @ $f = 217 \text{ Hz}$.

Table 8. Electrical characteristics ($V_{\text{CC}} = +2.2 \text{ V}$, $\text{GND} = 0 \text{ V}$, $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current no input signal, no load		5	8	mA
I_{STANDBY}	Standby current ⁽¹⁾ , no input signal, $V_{\text{stdby}} = \text{GND}$, $R_{\text{L}} = 8 \text{ } \Omega$		10	1000	nA
V_{oo}	Output offset voltage no input signal, $R_{\text{L}} = 8 \text{ } \Omega$		5	20	mV
P_{o}	Output power THD = 1% max., $f = 1 \text{ kHz}$, $R_{\text{L}} = 8 \text{ } \Omega$		180		mW
THD + N	Total harmonic distortion + noise $P_{\text{o}} = 200 \text{ mW RMS}$, $G_{\text{v}} = 2$, $20 \text{ Hz} < f < 20 \text{ kHz}$, $R_{\text{L}} = 8 \text{ } \Omega$		0.15		%
PSRR	Power supply rejection ratio ⁽²⁾ $f = 217 \text{ Hz}$, $R_{\text{L}} = 8 \text{ } \Omega$, $R_{\text{Feed}} = 22 \text{ k}\Omega$, $V_{\text{ripple}} = 100 \text{ mV RMS}$		77		dB
ϕ_{M}	Phase margin at unity gain $R_{\text{L}} = 8 \text{ } \Omega$, $C_{\text{L}} = 500 \text{ pF}$		70		Degrees
GM	Gain margin $R_{\text{L}} = 8 \text{ } \Omega$, $C_{\text{L}} = 500 \text{ pF}$		20		dB
GBP	Gain bandwidth product $R_{\text{L}} = 8 \text{ } \Omega$		2		MHz

1. Standby mode is active when V_{stdby} is tied to GND.
2. Dynamic measurements - $20 \cdot \log(\text{RMS}(V_{\text{out}})/\text{RMS}(V_{\text{ripple}}))$. V_{ripple} is the superimposed sinus signal to V_{CC} @ $f = 217 \text{ Hz}$.

4 Electrical characteristics curves

Figure 3. Open loop frequency response

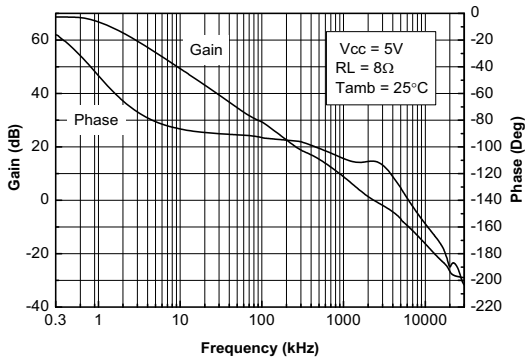


Figure 4. Open loop frequency response ($Z_L=8\Omega$)

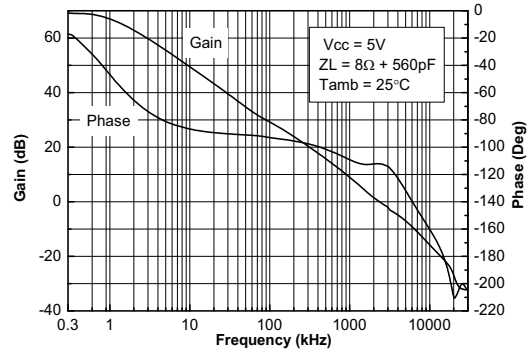


Figure 5. Open loop frequency response ($V_{CC}=3.3V$)

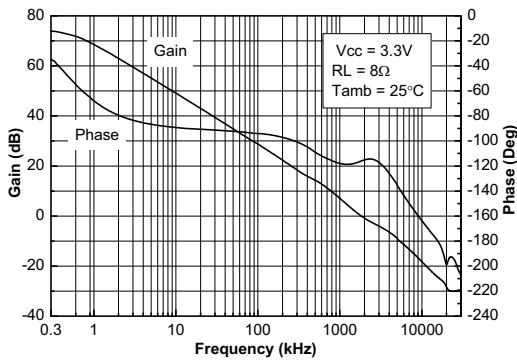


Figure 6. Open loop frequency response (560 pF)

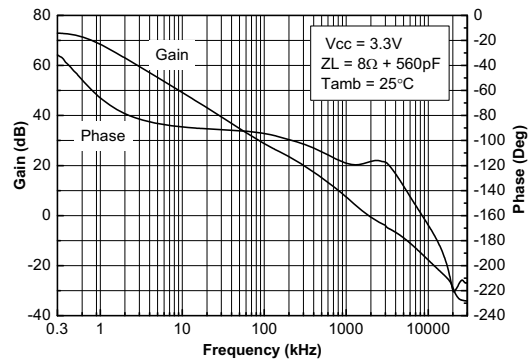


Figure 7. Open loop frequency response (Vcc=2.6 V)

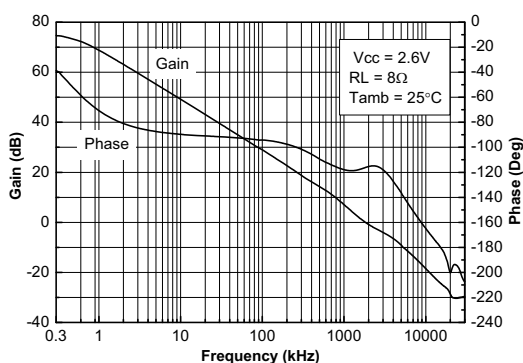


Figure 8. Open loop frequency response (Vcc=2.6 V+560 pF)

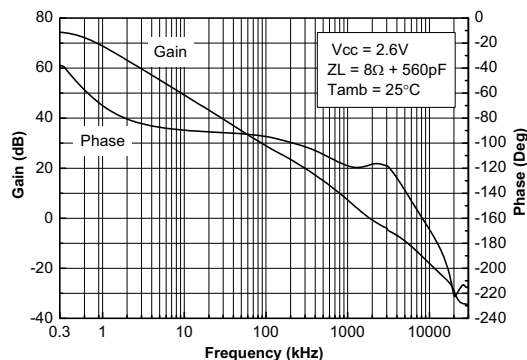


Figure 9. Open loop frequency response (Vcc=2.2 V)

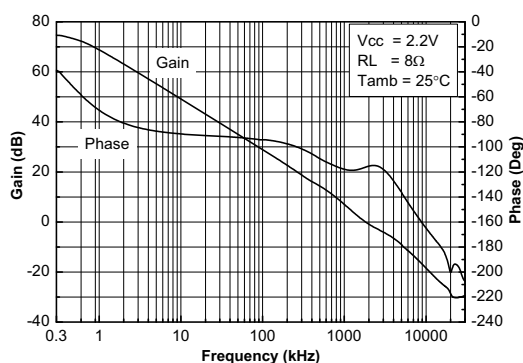


Figure 10. Open loop frequency response (Vcc=2.2 V+560 pF)

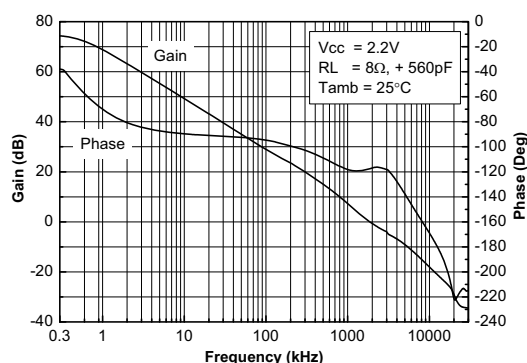


Figure 11. Open loop frequency response (Vcc=5 V)

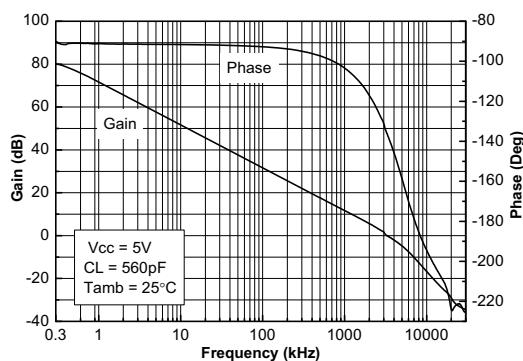


Figure 12. Open loop frequency response (Vcc=5 V+ 560 pF)

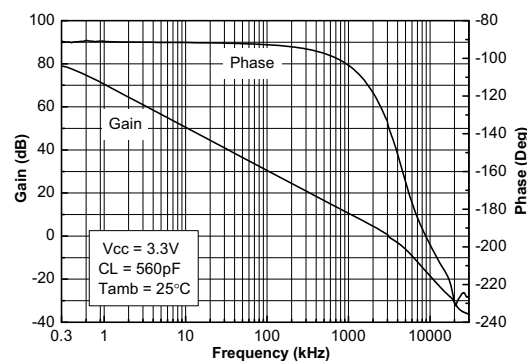


Figure 13. Open loop frequency response (Vcc=2.6 V; CL=560 pF)

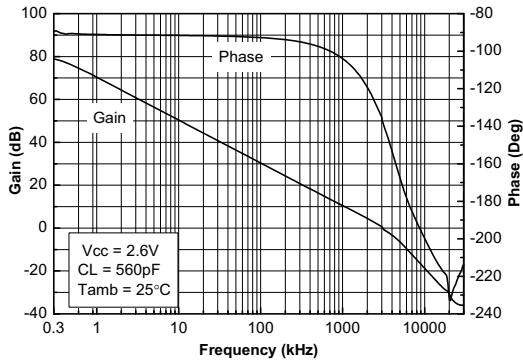


Figure 14. Open loop frequency response (Vcc=2.2 V; CL=560 pF)

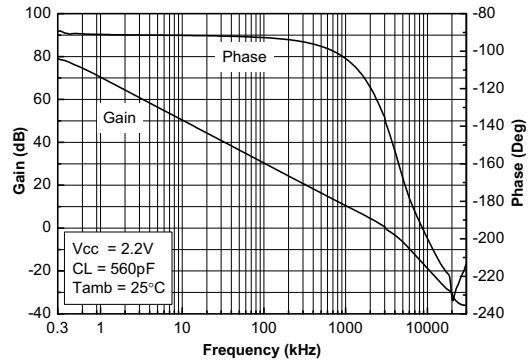


Figure 15. Power supply rejection ratio (PSRR) vs power supply

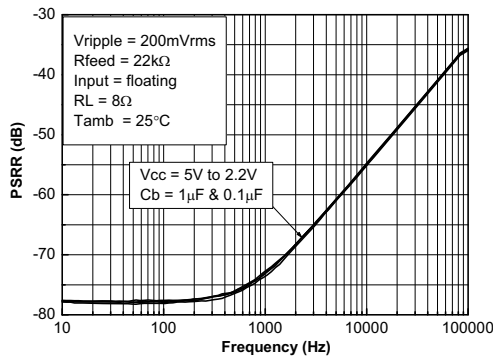


Figure 16. Power Supply Rejection Ratio (PSRR) vs feedback capacitor

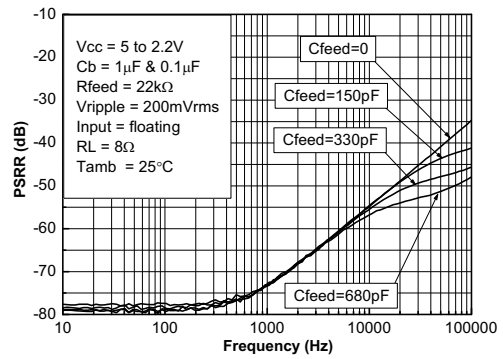


Figure 17. Power supply rejection ratio (PSRR) vs bypass capacitor

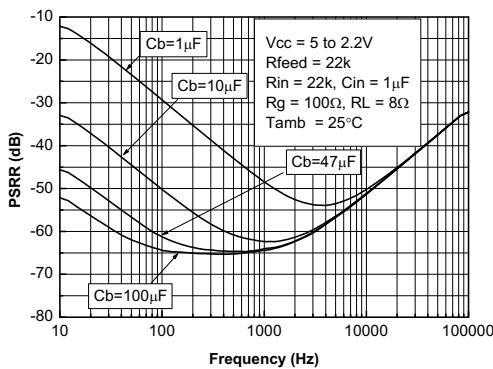


Figure 18. Power supply rejection ratio (PSRR) vs input capacitor

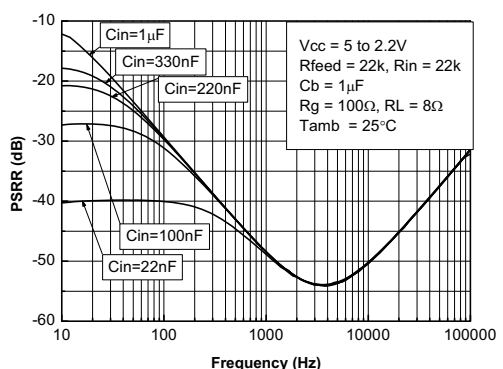


Figure 19. Power supply rejection ratio (PSRR) vs feedback resistor

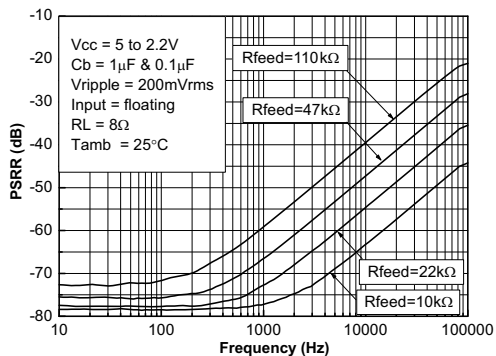


Figure 20. Pout @ THD + N = 1% vs supply voltage vs RL

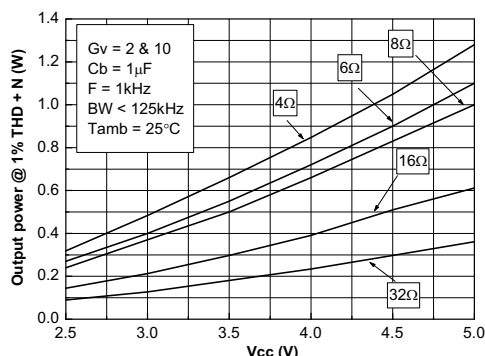


Figure 21. Pout @ THD + N = 10% vs supply voltage vs RL

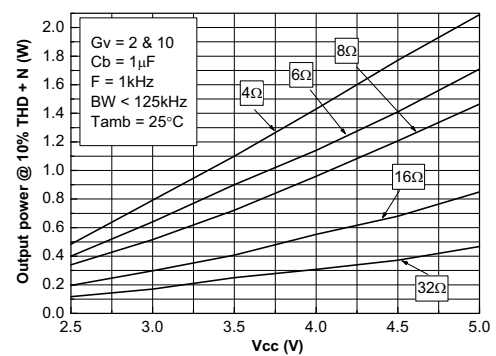


Figure 22. Power dissipation vs Pout

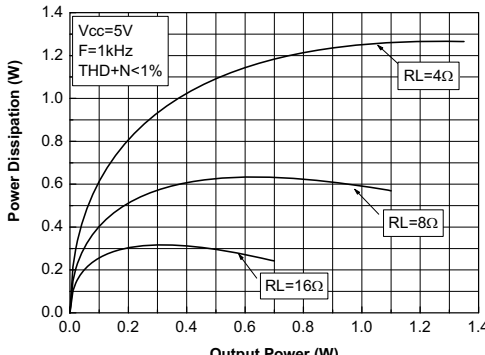


Figure 23. Power dissipation vs Pout (Vcc = 3.3 V)

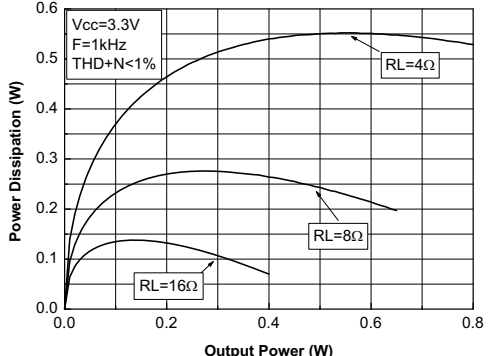


Figure 24. Power dissipation vs Pout (Vcc = 2.6 V)

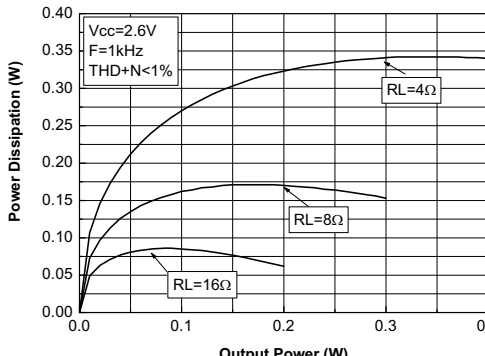


Figure 25. Power dissipation vs Pout (F=1 kHz)

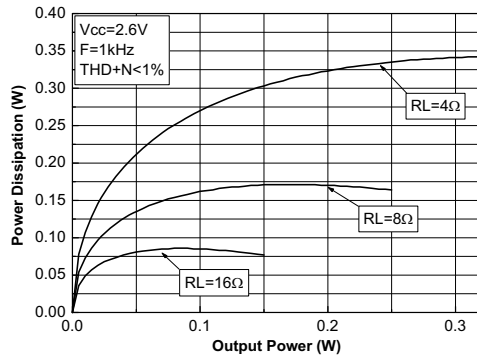


Figure 26. Power derating curves

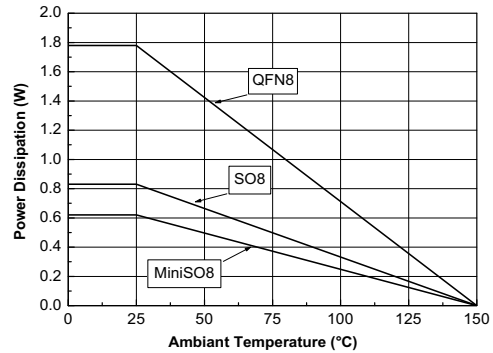


Figure 27. THD + N vs output power

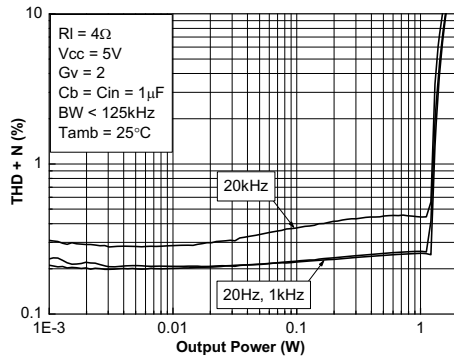


Figure 28. THD + N vs output power (VCC=5 V)

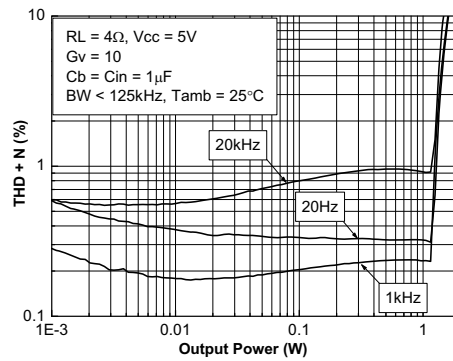


Figure 29. THD + N vs output power (Gv=2)

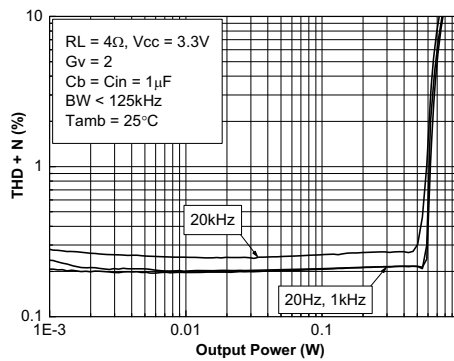


Figure 30. THD + N vs output power (Vcc=3.3 V)

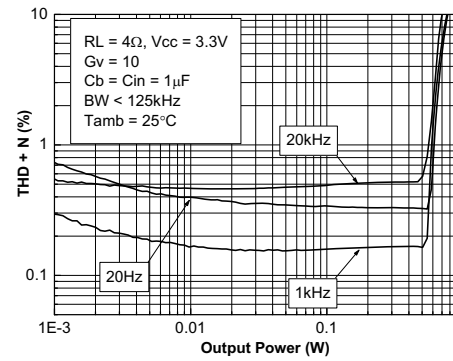


Figure 31. THD + N vs output power (Vcc=2.6 V)

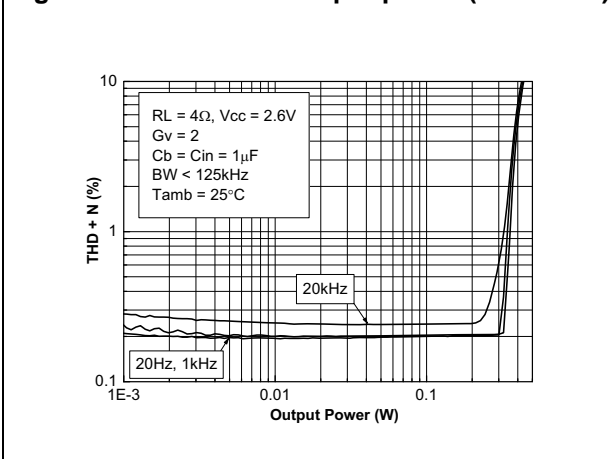


Figure 32. THD + N vs output power (RL=4 Ω)

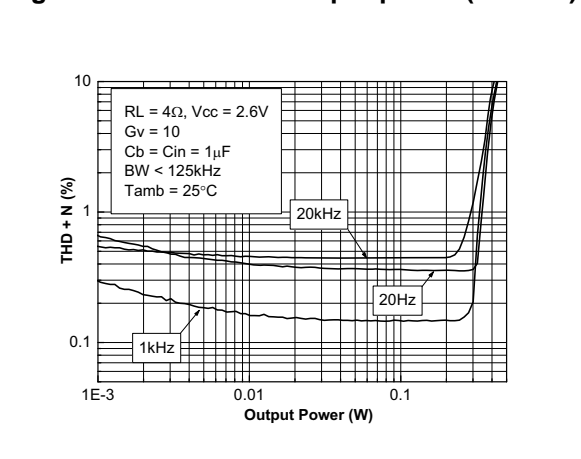


Figure 33. THD + N vs output power (VCC=2.2 V)

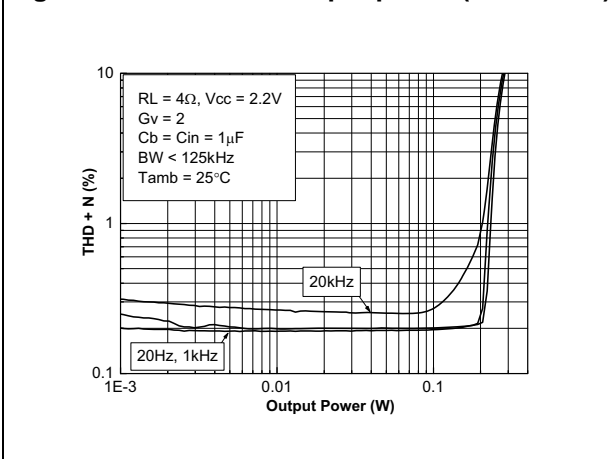


Figure 34. THD + N vs output power (Gv=10)

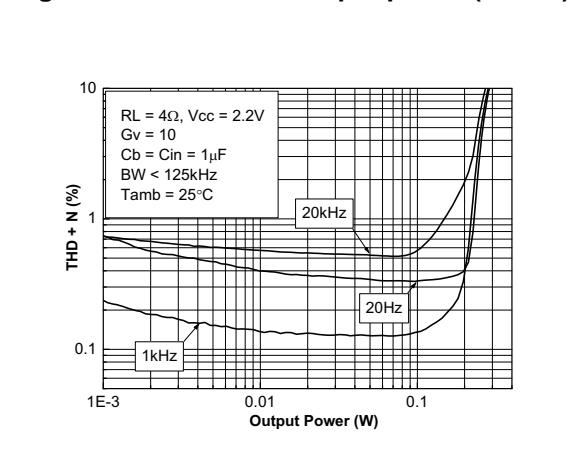


Figure 35. THD + N vs output power (RL=8 Ω)

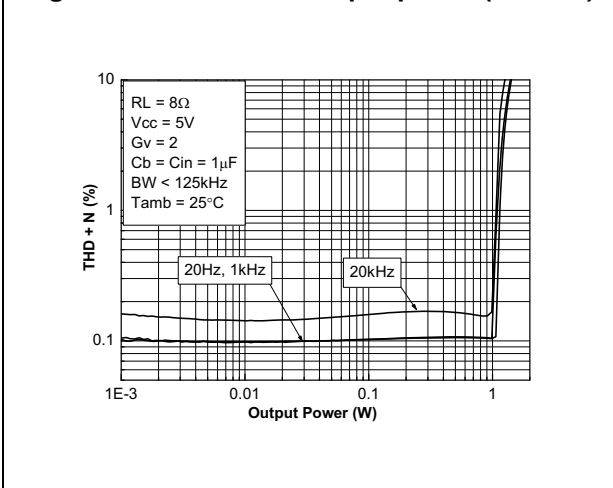


Figure 36. THD + N vs output power (Vcc=5 V, RL= 8 Ω)

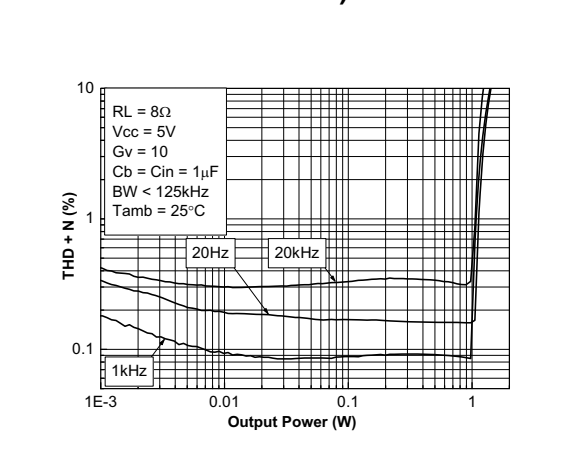


Figure 37. THD + N vs output power (Vcc=3.3 V, Gv= 2)

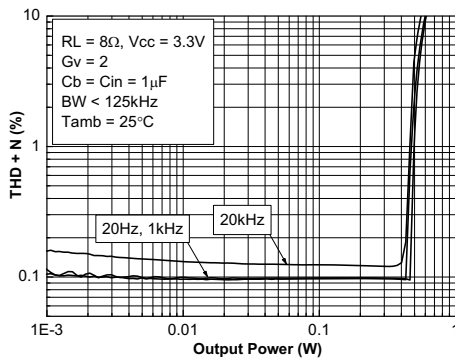


Figure 38. HD + N vs output power (Vcc=3.3 V, Gv= 10)

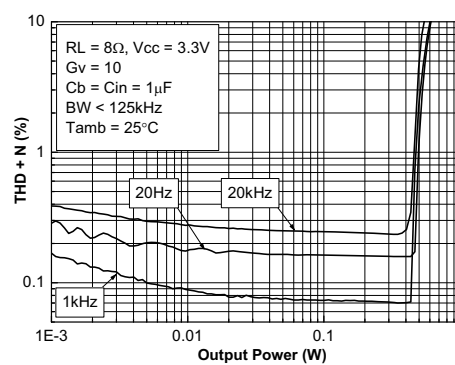


Figure 39. THD + N vs output power (Vcc=2.6 V, Gv= 2)

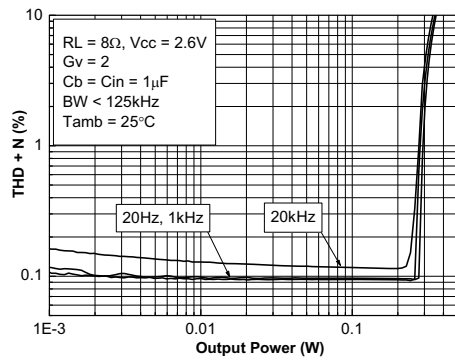


Figure 40. THD + N vs output power (Vcc=2.6 V, Gv= 10)

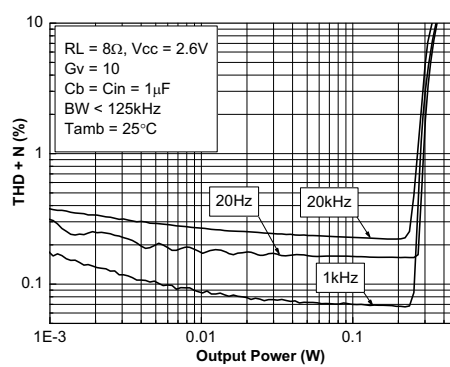


Figure 41. THD + N vs output power (Vcc=2.2 V, Gv= 2)

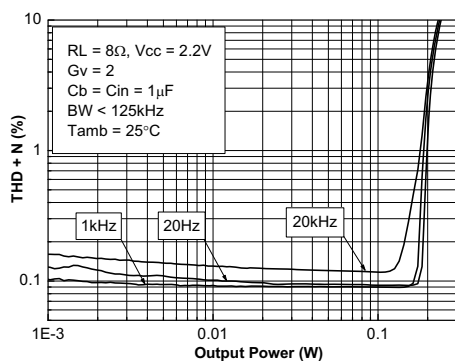
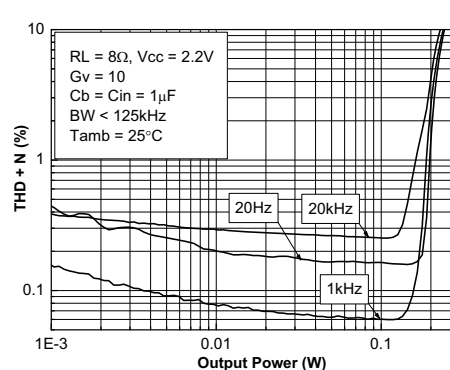


Figure 42. THD + N vs output power (Vcc=2.2 V, Gv= 10)



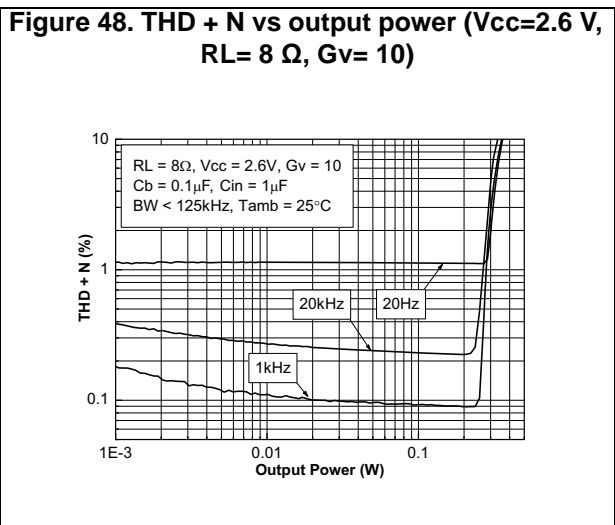
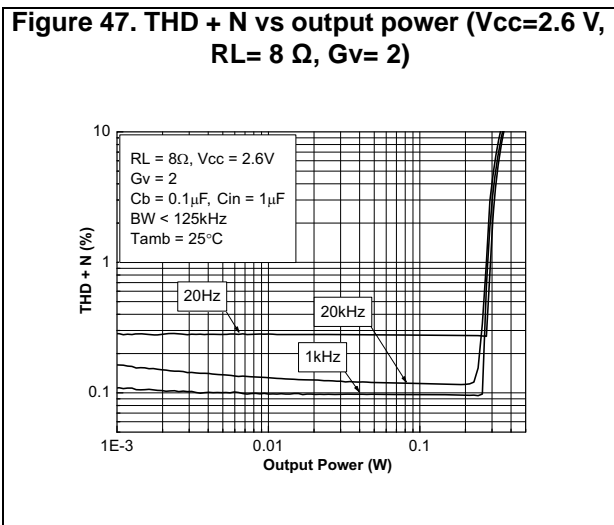
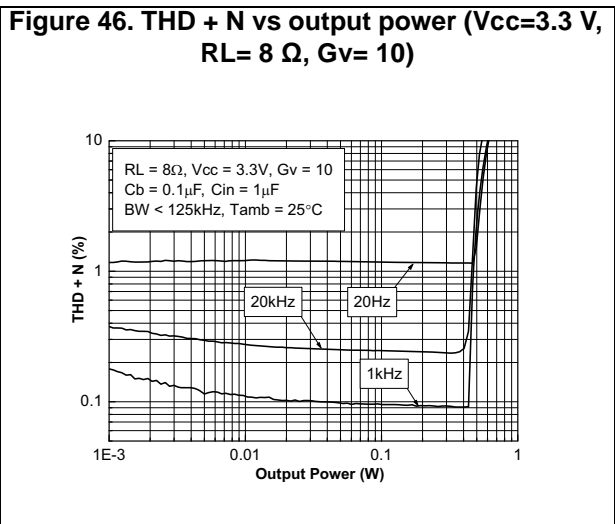
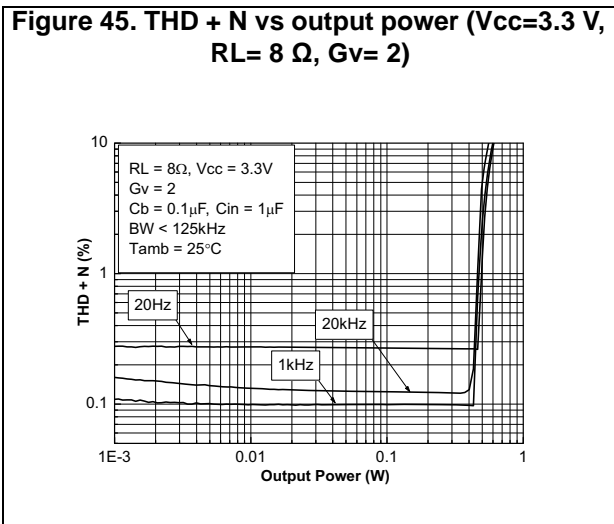
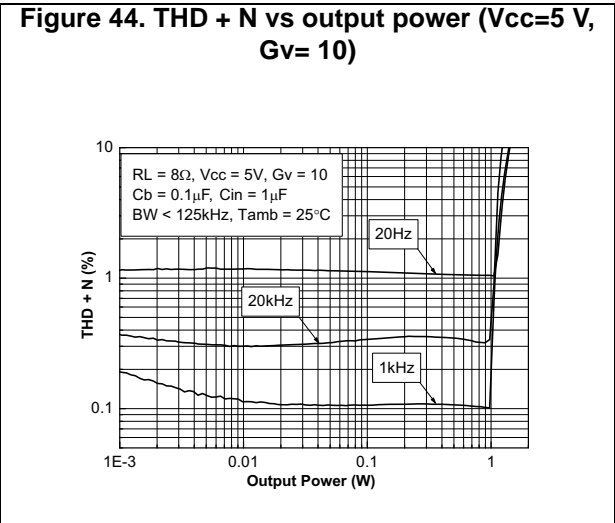
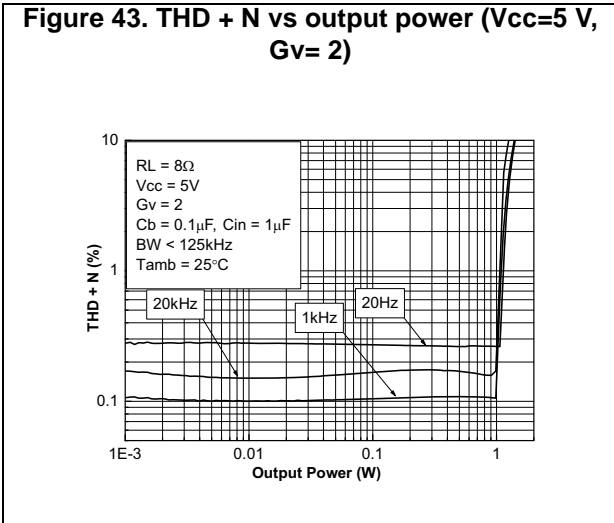


Figure 49. THD + N vs output power (Vcc=2.2 V, RL= 8 Ω, Gv= 2)

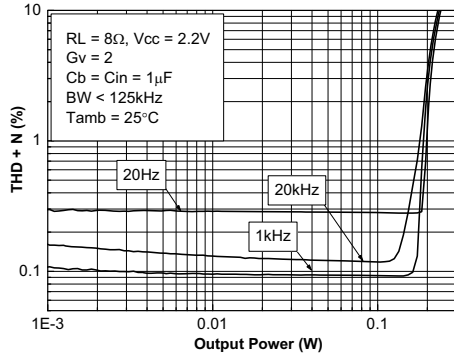


Figure 50. THD + N vs output power (Vcc=2.2 V, RL= 8 Ω, Gv= 10)

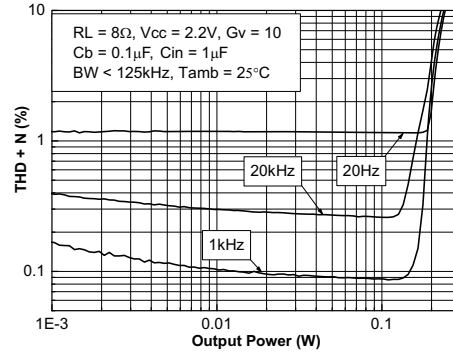


Figure 51. THD + N vs output power (Vcc=5 V, RL= 16 Ω, Gv= 2)

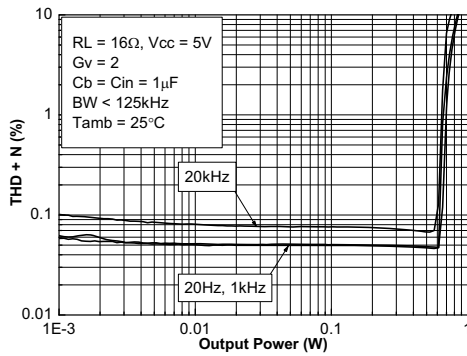


Figure 52. THD + N vs output power (Vcc=5 V, RL= 16 Ω, Gv= 10)

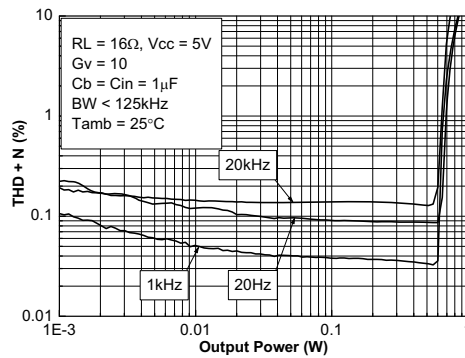


Figure 53. THD + N vs output power (Vcc=3.3 V, RL= 16 Ω, Gv= 2)

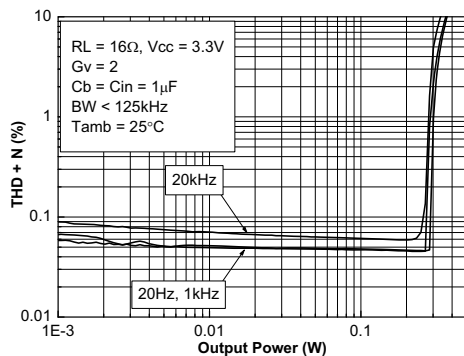


Figure 54. THD + N vs output power (Vcc=3.3 V, RL= 16 Ω, Gv= 10)

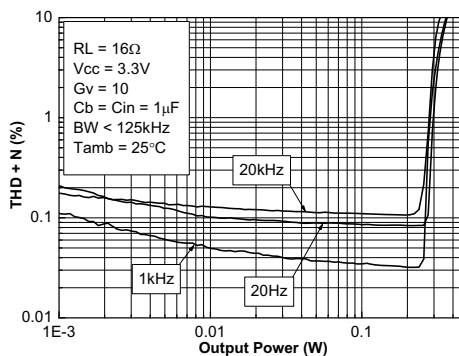


Figure 55. THD + N vs output power (Vcc=2.6 V, RL= 16 Ω, Gv= 2)

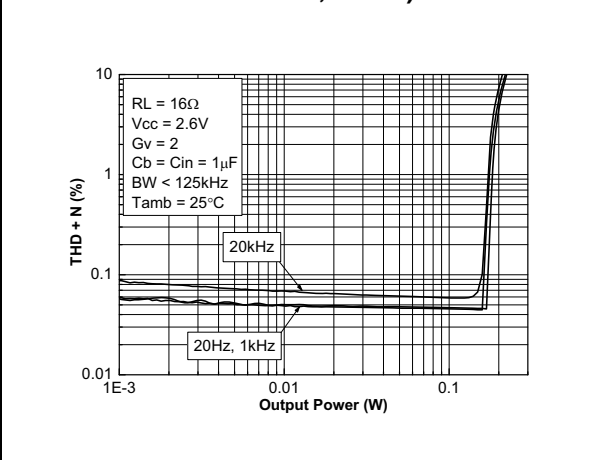


Figure 56. THD + N vs output power (Vcc=2.6 V, RL= 16 Ω, Gv= 10)

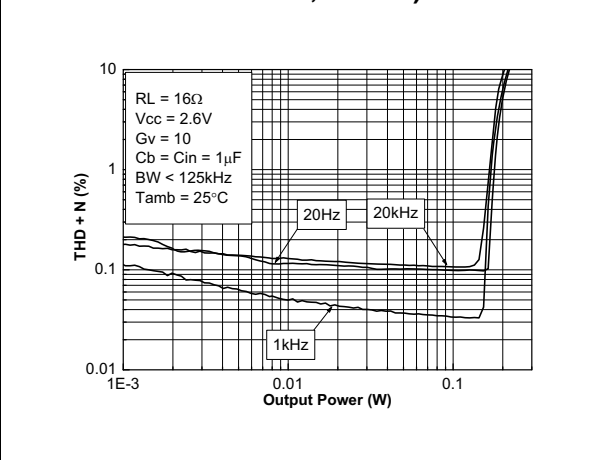


Figure 57. THD + N vs output power (Vcc=2.2 V, RL= 16 Ω, Gv= 2)

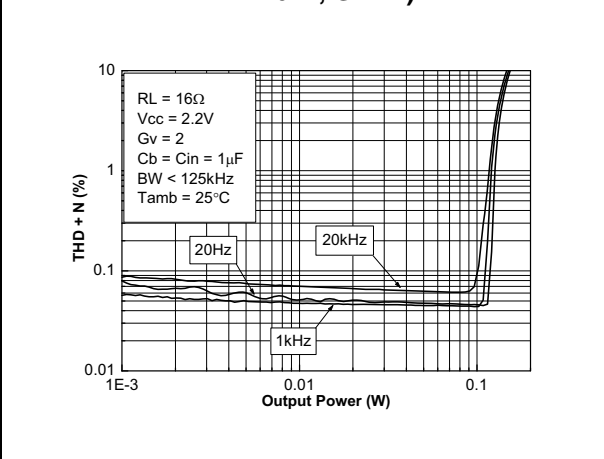


Figure 58. THD + N vs output power (Vcc=2.2 V, RL= 16 Ω, Gv= 10)

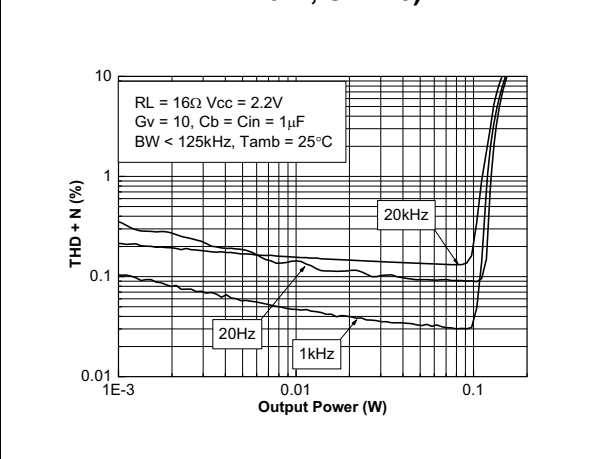


Figure 59. THD + N vs frequency (Vcc=5 V, RL= 4 Ω, Gv= 2)

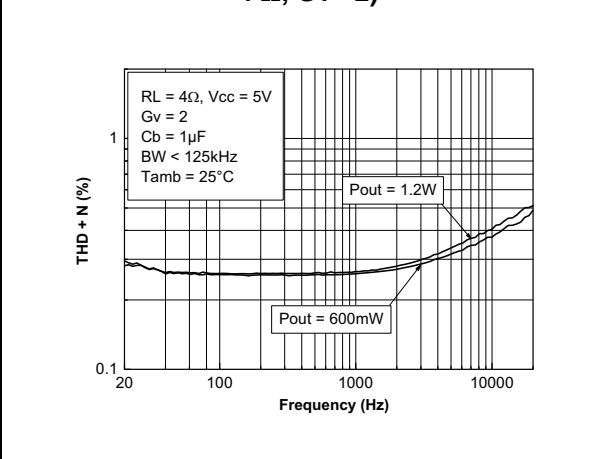


Figure 60. THD + N vs frequency (Vcc=5 V, RL= 4 Ω, Gv= 10)

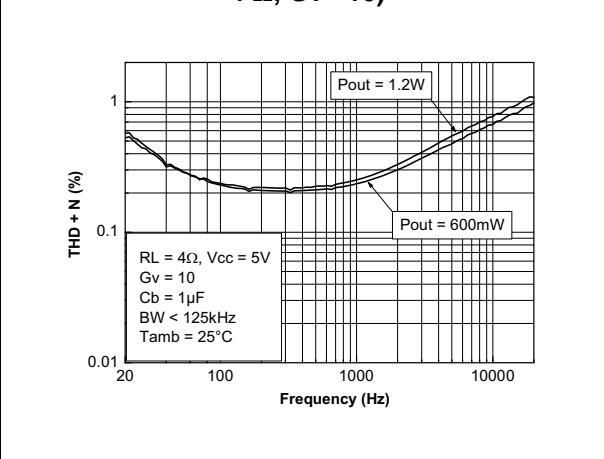


Figure 61. THD + N vs frequency (Vcc=3.3 V, RL= 4 Ω, Gv= 2)

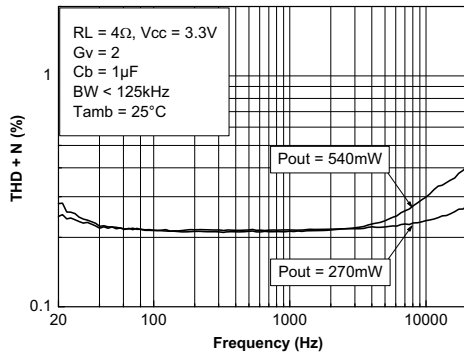


Figure 62. THD + N vs frequency (Vcc=3.3 V, RL= 4 Ω, Gv= 10)

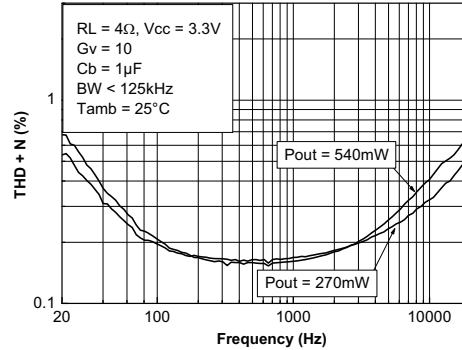


Figure 63. THD + N vs frequency (Vcc=2.6 V, RL= 4 Ω, Gv= 2)

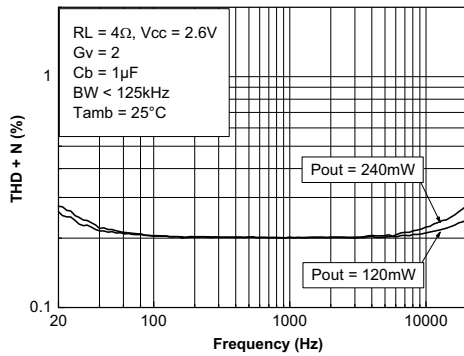


Figure 64. THD + N vs frequency (Vcc=2.6 V, RL= 4 Ω, Gv= 10)

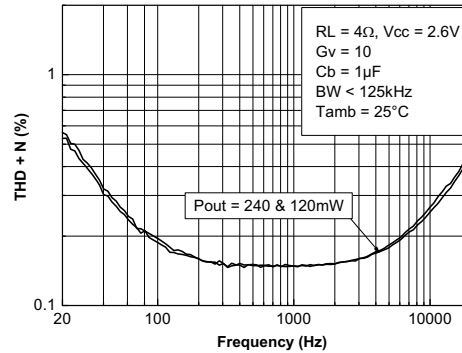


Figure 65. THD + N vs frequency (Vcc=2.2 V, RL= 4 Ω, Gv= 2)

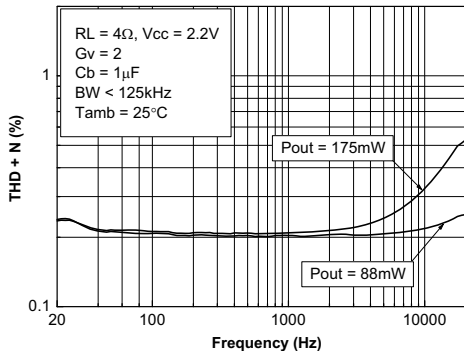


Figure 66. THD + N vs frequency (Vcc=2.2 V, RL= 4 Ω, Gv= 10)

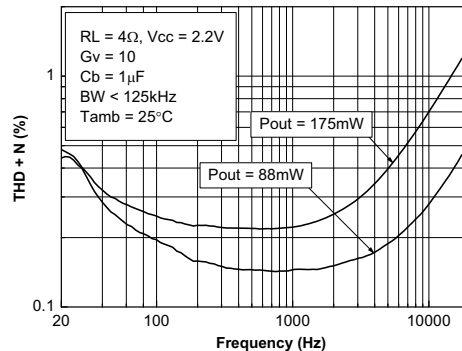


Figure 67. THD + N vs frequency (Vcc=5 V, RL= 8 Ω, Gv= 2)

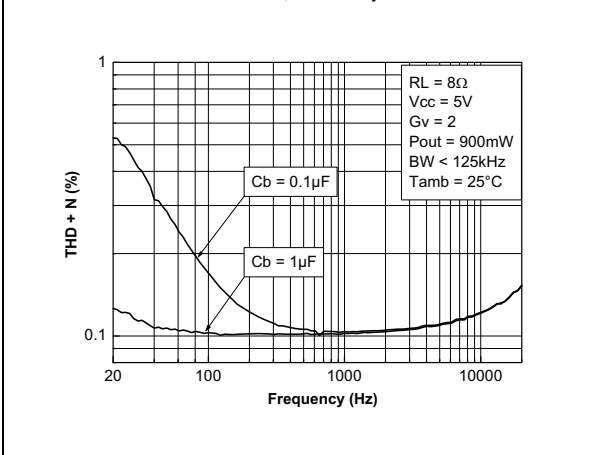


Figure 68. THD + N vs frequency (Vcc=5 V, RL= 8 Ω, Gv= 2)

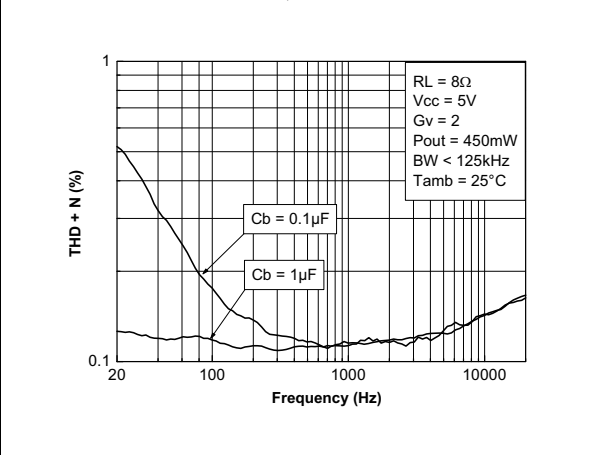


Figure 69. THD + N vs frequency (Vcc=5 V, RL= 8 Ω, Gv= 10)

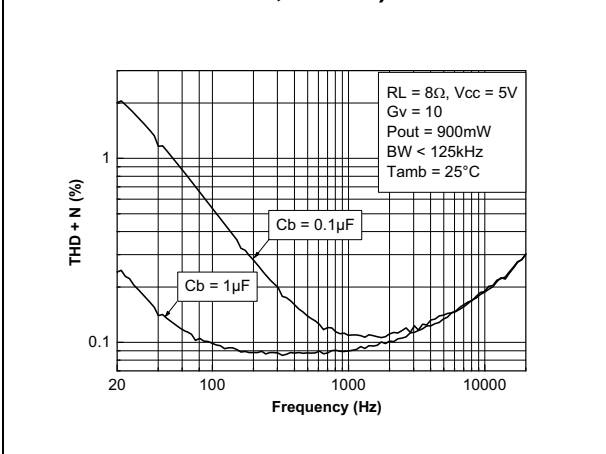


Figure 70. THD + N vs frequency (Pout= 450 mW)

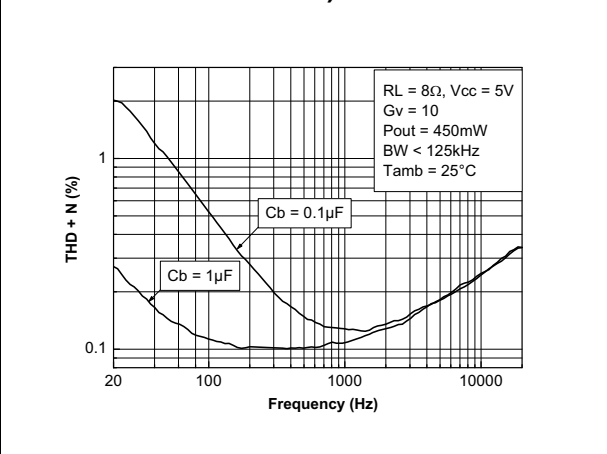


Figure 71. THD + N vs frequency (Pout= 400 mW)

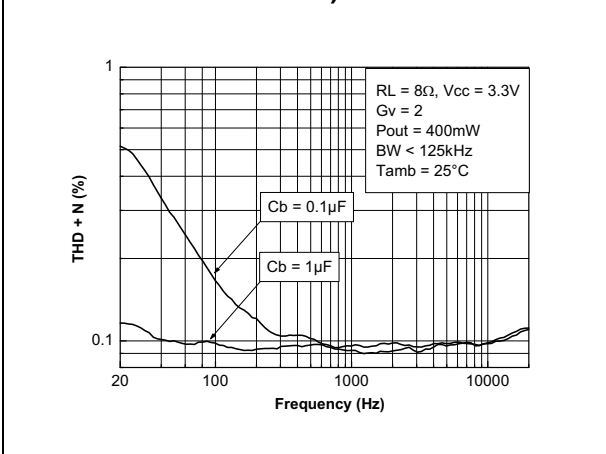


Figure 72. THD + N vs frequency (Pout= 200 mW)

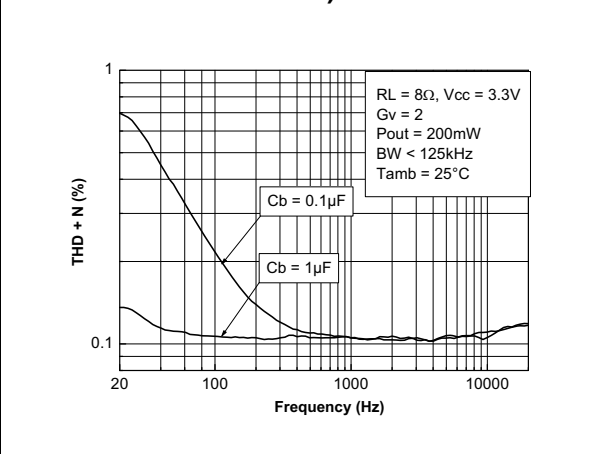


Figure 73. THD + N vs frequency ($V_{CC}=3.3\text{ V}$, $R_L= 8\ \Omega$, $G_v= 10$, $P_{out}= 400\text{ mW}$)

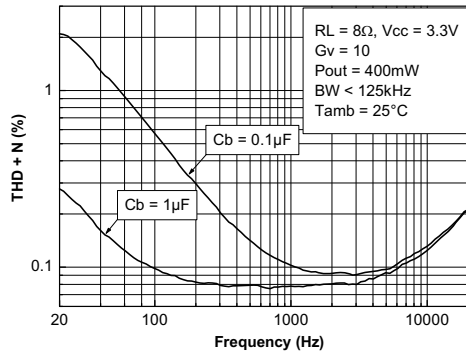


Figure 74. THD + N vs frequency ($P_{out}= 200\text{ mW}$)

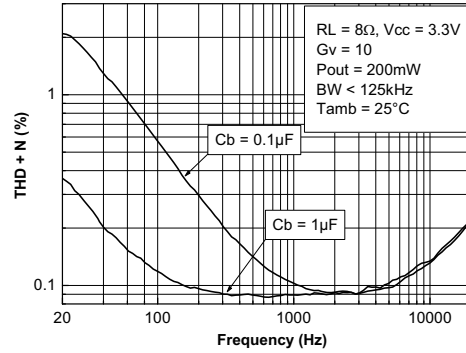


Figure 75. THD + N vs frequency ($P_{out}= 220\text{ mW}$)

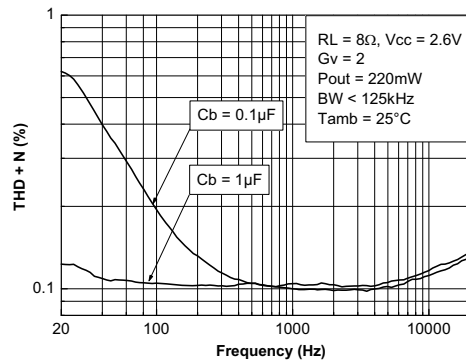


Figure 76. THD + N vs frequency ($P_{out}= 110\text{ mW}$)

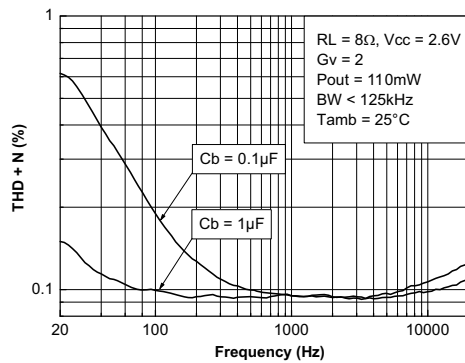


Figure 77. THD + N vs frequency ($V_{CC}=2.6\text{ V}$, $P_{out}= 220\text{ mW}$)

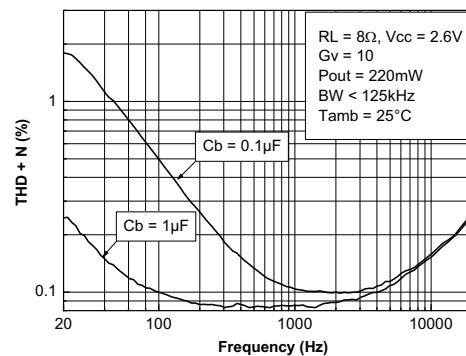
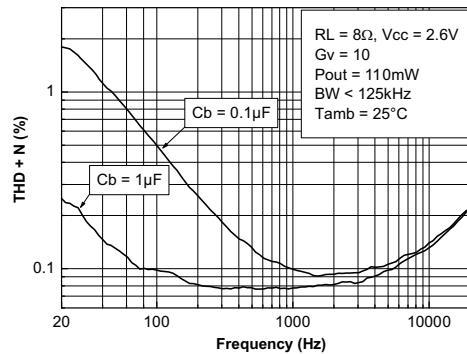


Figure 78. THD + N vs frequency ($P_{out}=110\text{ mW}$)



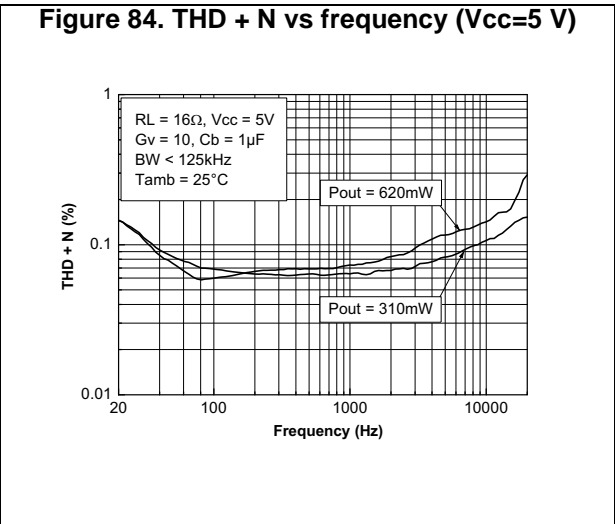
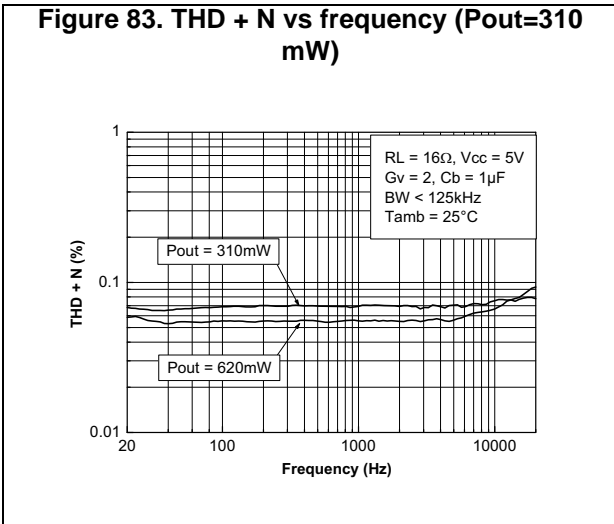
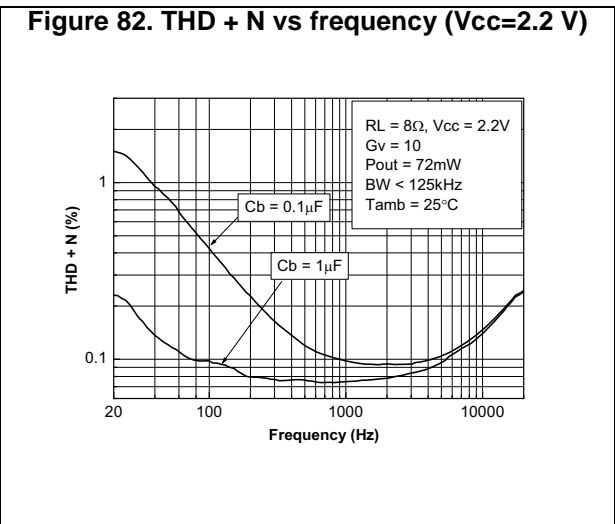
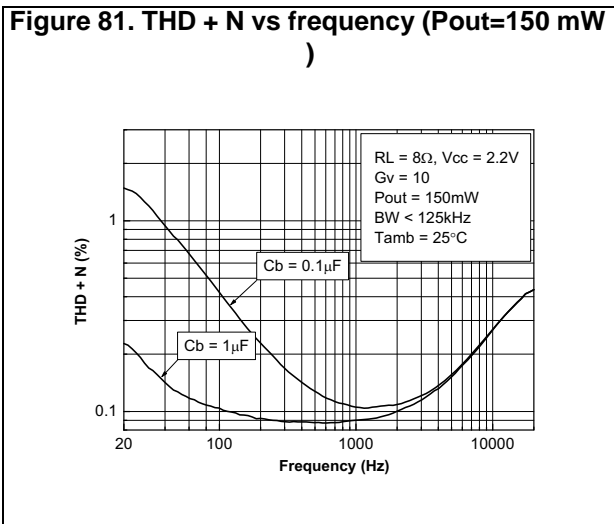
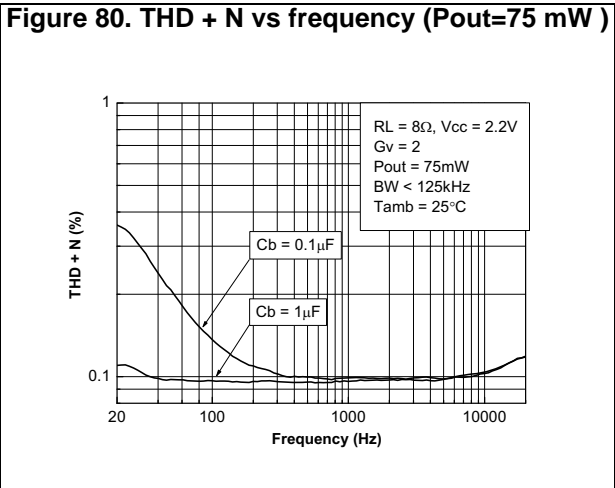
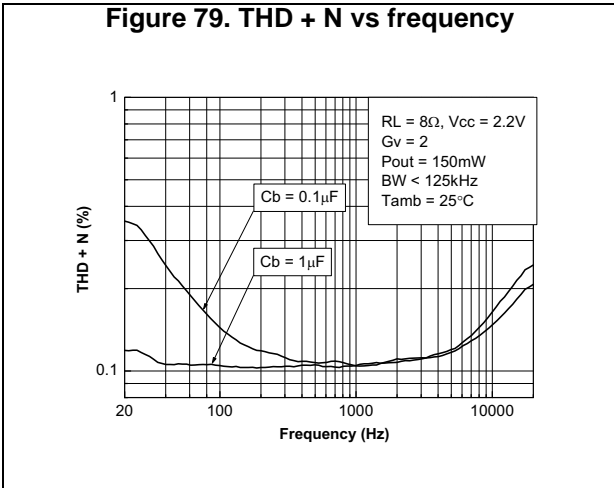


Figure 85. THD + N vs frequency (Gv=2)

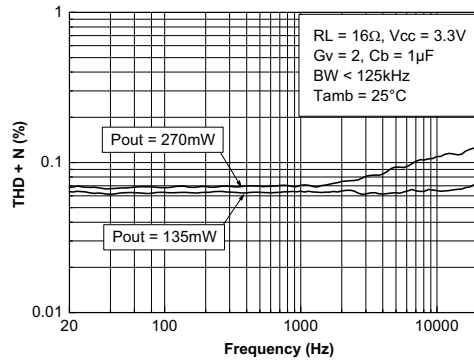


Figure 86. THD + N vs frequency (Vcc=3.3 V)

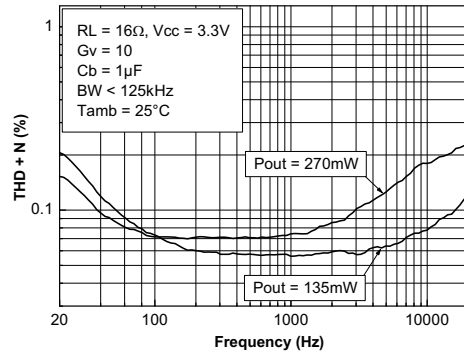


Figure 87. THD + N vs frequency (Gv=10)

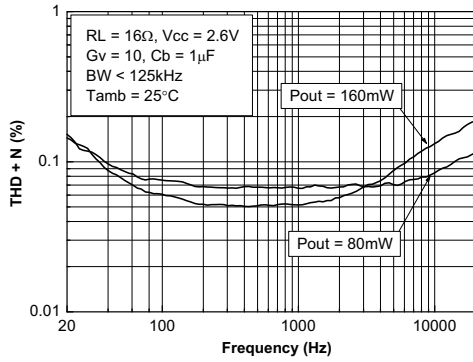


Figure 88. THD + N vs frequency (Vcc=2.6 V)

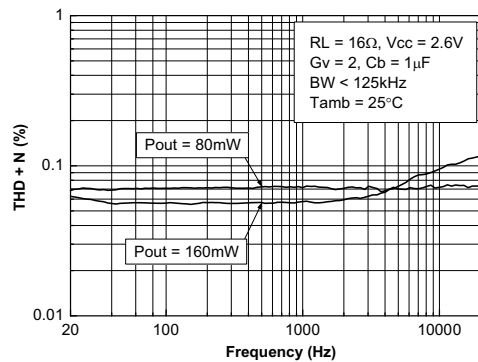


Figure 89. THD + N vs frequency (Vcc=2.2 V)

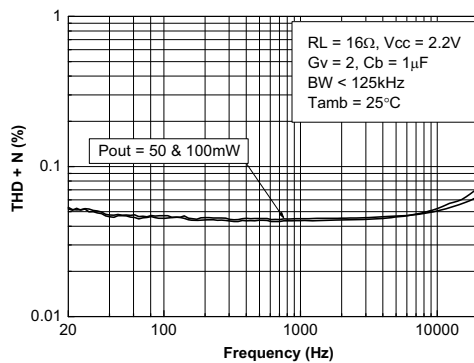


Figure 90. THD + N vs frequency (Pout=50 mW)

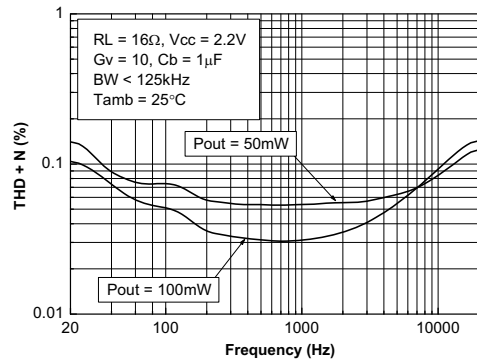


Figure 91. Signal-to-noise ratio vs power supply with unweighted filter (Gv=2)

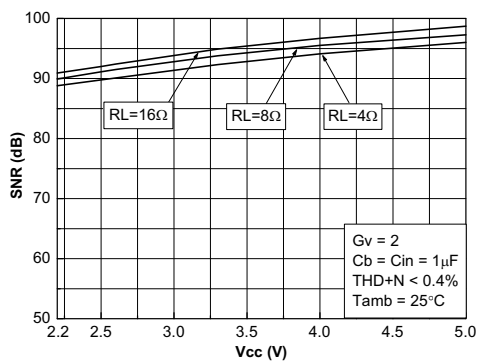


Figure 92. Signal-to-noise ratio vs power supply with unweighted filter (20Hz to 20kHz)

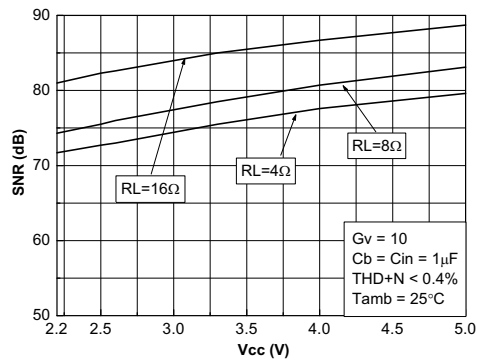


Figure 93. Signal-to-noise ratio vs power supply Gv=2

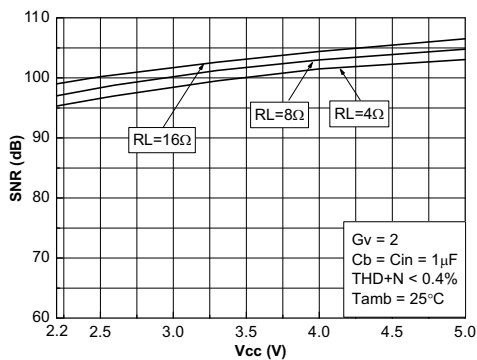


Figure 94. Signal-to-noise ratio vs power supply with weighted filter type A

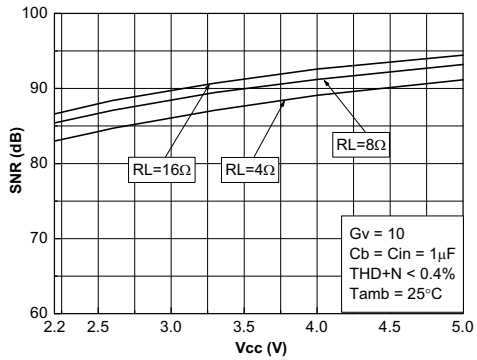


Figure 95. Frequency response gain vs Cin, and Cfeed

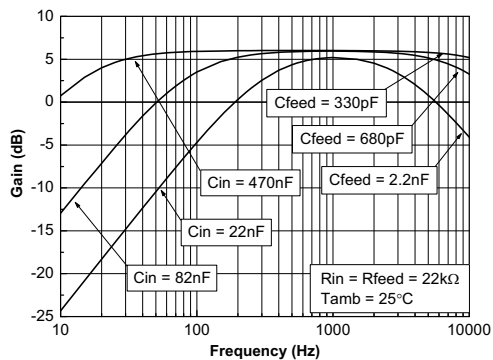


Figure 96. Current consumption vs power supply voltage (no load)

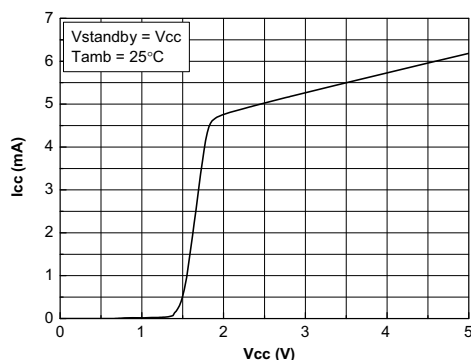


Figure 97. Current consumption vs standby voltage @ Vcc = 5 V

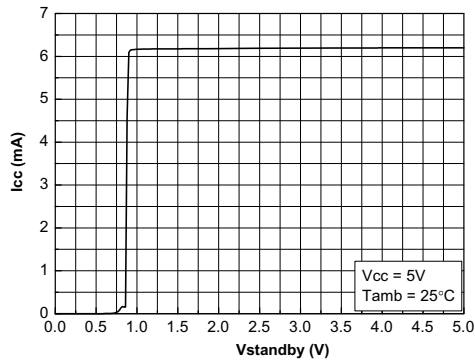


Figure 98. Current consumption vs standby voltage @ Vcc = 3.3 V

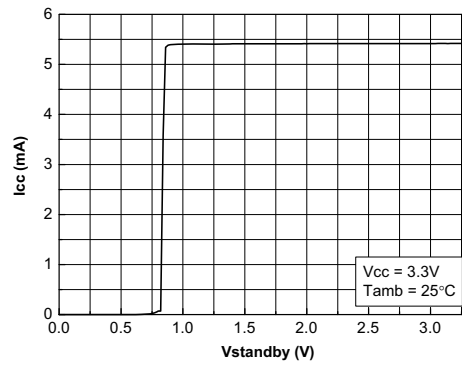


Figure 99. Current consumption vs standby voltage @ Vcc = 2.6 V

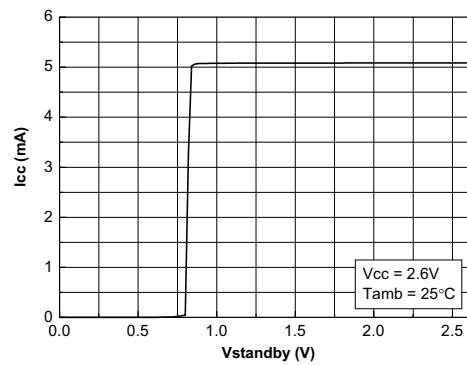


Figure 100. Current consumption vs standby voltage @ Vcc = 2.2 V

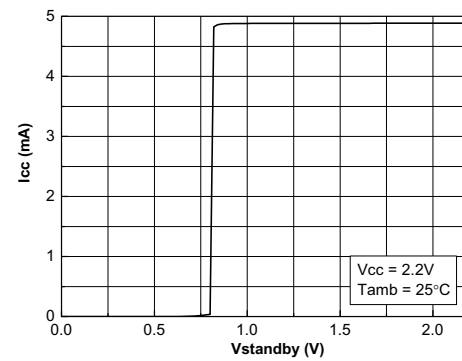


Figure 101. Clipping voltage vs power supply voltage

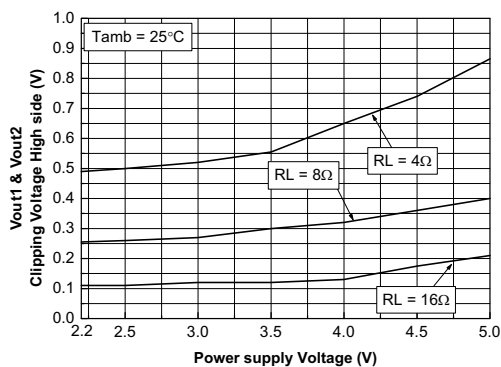


Figure 102. Clipping voltage vs power supply voltage and load resistor

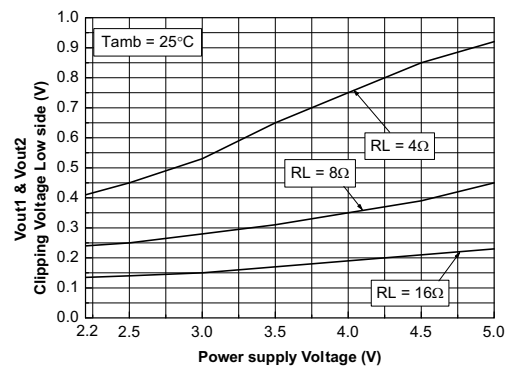


Figure 103. Vout1+Vout2 unweighted noise floor

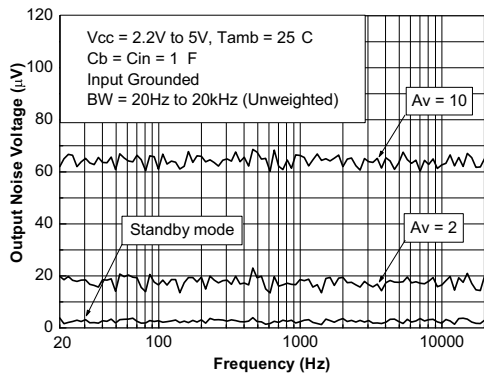
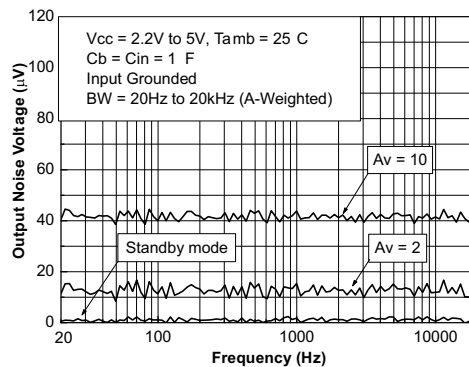


Figure 104. Vout1+Vout2 A-weighted noise floor



5 Application information

Figure 105. Demoboard schematic

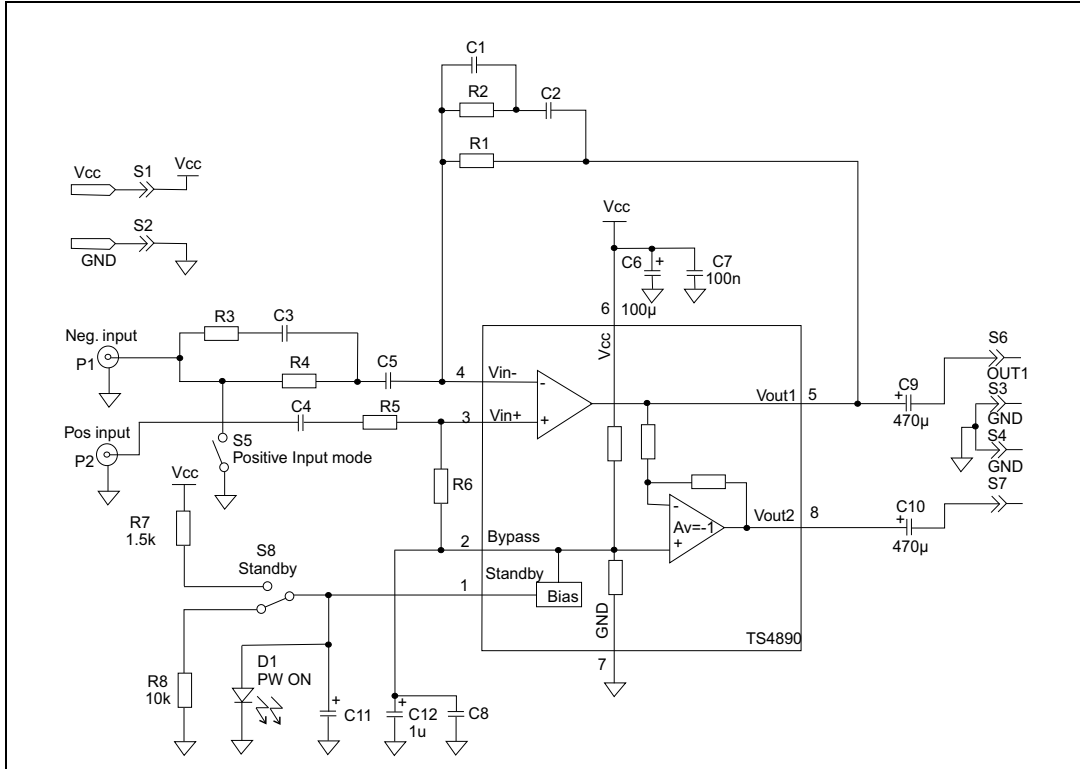


Figure 106. SO8 and MiniSO8 demoboard component side

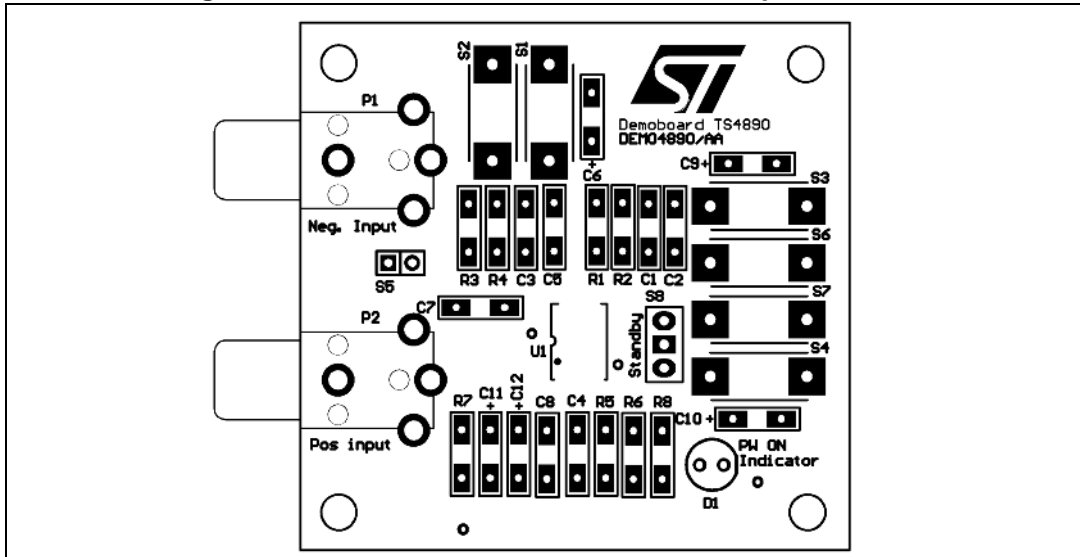


Figure 107. SO8 and MiniSO8 demoboard top solder layer

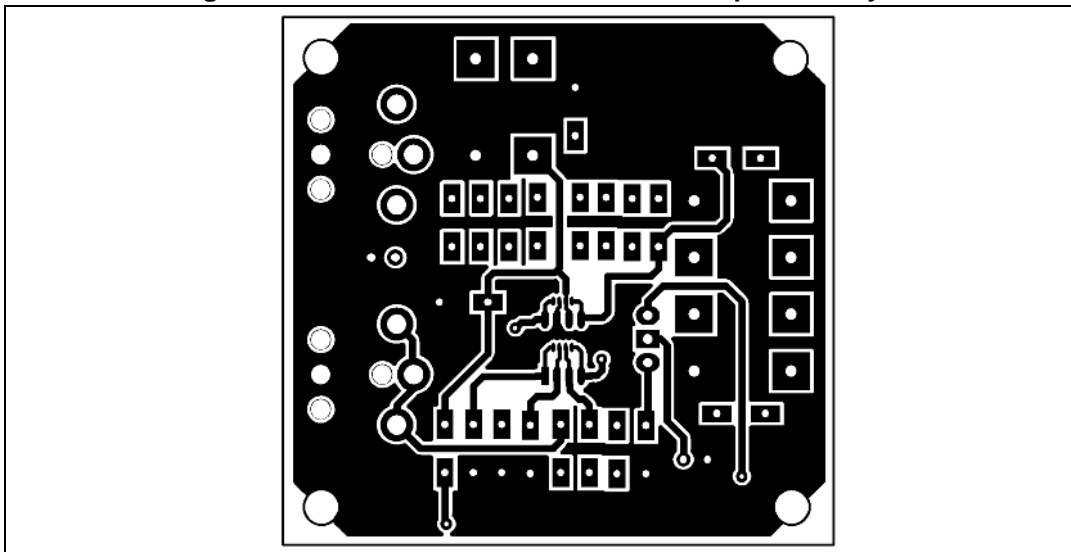
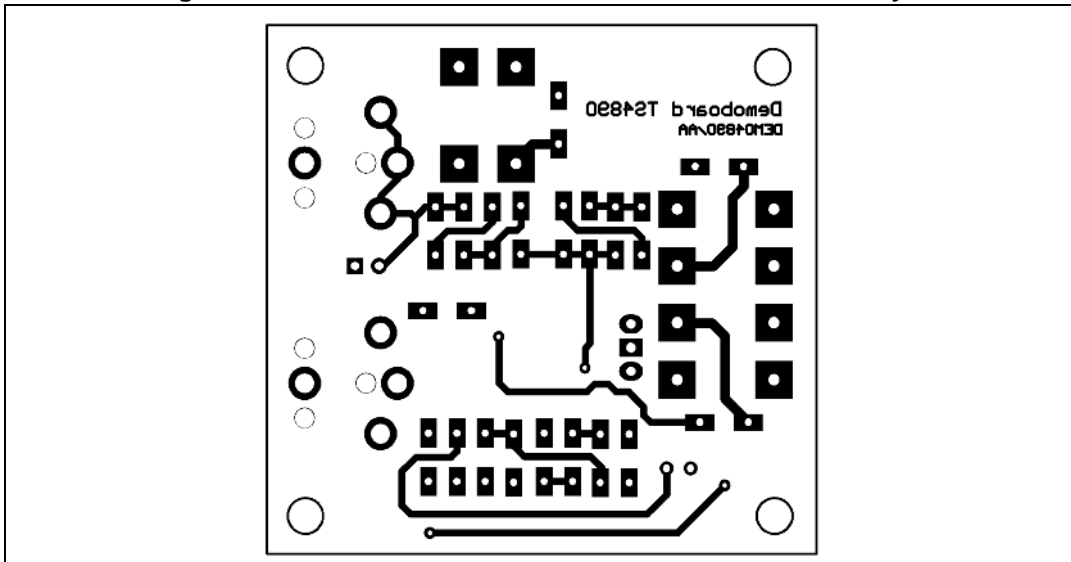


Figure 108. SO8 and MiniSO8 demoboard bottom solder layer



5.1 BTL configuration principle

The TS4890 is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load are connected to two single ended output amplifiers. Thus, we have:

- Single ended output 1 = $V_{out1} = V_{out}$ (V)
- Single ended output 2 = $V_{out2} = V_{out}$ (V)
- and $V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is:

$$P_{out} = \frac{(2V_{out_{RMS}})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

5.2 Gain in typical application schematic

In flat region (no effect of C_{in}), the output voltage of the first stage is:

$$V_{out1} = -V_{in} \frac{R_{feed}}{R_{in}} (V)$$

For the second stage: $V_{out2} = -V_{out1}$ (V)

The differential output voltage is:

$$V_{out2} - V_{out1} = 2V_{in} \frac{R_{feed}}{R_{in}} (V)$$

The differential gain named gain (G_v) for more convenient usage is:

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2 \frac{R_{feed}}{R_{in}}$$

Remark: V_{out2} is in phase with V_{in} and V_{out1} is 180 phased with V_{in} . It means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1} .

5.3 Low and high frequency response

In low frequency region, the effect of C_{in} starts. C_{in} with R_{in} forms a high pass filter with a -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}} (Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel on R_{feed} . Its form a low pass filter with a -3 dB cut-off frequency.

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}} (Hz)$$

5.4 Power dissipation and efficiency

Hypothesis:

- Voltage and current in the load are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{cc})

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin \omega t (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (W)$$

Then, the average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = 2 \frac{V_{PEAK}}{\pi R_L} (A)$$

The power delivered by the supply voltage is $P_{supply} = V_{cc} I_{CC_{AVG}}$ (W).

Then, the power dissipated by the amplifier is $P_{diss} = P_{supply} - P_{out}$ (W)

$$P_{diss} = \frac{2\sqrt{2}V_{cc}}{\pi\sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} (W)$$

and the maximum value is obtained when

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is

$$P_{dissmax} = \frac{2V_{cc}^2}{\pi^2 R_L} (W)$$

Remark: This maximum value is only depending on power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply.

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so

$$\frac{\pi}{4} = 78.5\text{percentage}$$

5.5 Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4890. A power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b .

C_s has especially an influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.

With 100 μF , you can expect similar THD+N performance like shown in the datasheet.

If C_s is lower than 100 μF , in high frequency THD+N increases and disturbances on the power supply rail are less filtered.

To the contrary, if C_s is higher than 100iF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N in lower frequency, but its function is critical on the final result of PSRR with input grounded in lower frequency.

If C_b is lower than 1 μF , THD+N increases in lower frequency (see THD+N vs frequency curves) and the PSRR worsens up.

If C_b is higher than 1 μF , the benefit on THD+N in lower frequency is small but the benefit on PSRR is substantial (see PSRR vs. C_b curves).

Note that C_{in} has a non-negligible effect on PSRR in lower frequency. Lower is its value, higher is the PSRR.

5.6 Pop and click performance

In order to have the best performances with the pop and click circuitry, the formula below must be followed:

$$\tau_{in} \leq \tau_b$$

with

$$\tau_{in} = (R_{in} + R_{feed}) \times C_{in}(S)$$

and

$$\tau_b = 50\text{k}\Omega \times C_b(\text{s})$$

5.7 Power amplifier design examples

Given:

- Load impedance: 8 Ω
- Output power @ 1% THD+N: 0.5 W
- Input impedance: 10 k Ω min.
- Input voltage peak to peak: 1 V_{pp}
- Bandwidth frequency: 20 Hz to 20 kHz (0, -3 dB)
- THD+N in 20 Hz to 20 kHz < 0.5% @ P_{out}=0.45 W
- Ambient temperature max. = 50 °C
- SO8 package

First of all, we must calculate the minimum power supply voltage to obtain 0.5 W into 8 Ω . See curves in [Figure 15](#), we can read 3.5 V. Thus, the power supply voltage value min. is 3.5 V. Following the maximum power dissipation equation:

$$P_{\text{dissmax}} = \frac{2V_{\text{CC}}^2}{\pi^2 R_L} (\text{W})$$

with 3.5 V we have P_{dissmax} = 0.31 W.

Refer to power derating curves ([Figure 24](#)), with 0.31 W the maximum ambient temperature is 100 °C. This last value could be higher if you follow the example layout shows on the demoboard (better dissipation).

The gain of the amplifier in flat region is:

$$G_V = \frac{V_{\text{OUTPP}}}{V_{\text{INPP}}} = \frac{\sqrt[2]{2R_L P_{\text{OUT}}}}{V_{\text{INPP}}} = 5.65$$

We have R_{in} > 10 k Ω . Let us take R_{in} = 10 k Ω , then R_{feed} = 28.25 k Ω . We could use for R_{feed} = 30 k Ω in normalized value and the gain is G_v = 6.

In lower frequency we want 20 Hz (-3dB cut off frequency). Then:

$$C_{\text{IN}} = \frac{1}{2\pi R_{\text{in}} F_{\text{CL}}} = 795\text{nF}$$

So, we could use for C_{IN} a 1 μF capacitor value that gives 16 Hz. In higher frequency we want 20 kHz (-3dB cut off frequency). The Gain bandwidth product of the TS4890 is 2 MHz typical and does not change when the amplifier delivers power into the load. The first amplifier has a gain of:

$$\frac{R_{\text{feed}}}{R_{\text{in}}} = 3$$

and the theoretical value of the -3 dB cut of higher frequency is $2 \text{ MHz}/3 = 660 \text{ kHz}$. We can keep this value or limiting the bandwidth by adding a capacitor C_{feed} , in parallel on R_{feed} . Then:

$$C_{\text{FEED}} = \frac{1}{2\pi R_{\text{FEED}} F_{\text{CH}}} = 265 \text{ pF}$$

So, we could use for C_{feed} a 220 pF capacitor value that gives 24 kHz. Now, we can choose the value of C_b with the constraint THD+N in 20 Hz to 20 kHz $< 0.5\%$ @ $P_{\text{out}}=0.45 \text{ W}$. If you refer to the closest THD+N vs frequency measurement: [Figure 71](#) ($V_{\text{cc}}=3.3 \text{ V}$, $G_v=10$), with $C_b = 1 \mu\text{F}$, the THD+N vs frequency is always below 0.4%. As the behavior is the same with $V_{\text{cc}} = 5 \text{ V}$ ([Figure 67](#)), $V_{\text{cc}} = 2.6 \text{ V}$ ([Figure 67](#)). As the gain for these measurements is higher (worst case), we can consider with $C_b = 1 \mu\text{F}$, $V_{\text{cc}} = 3.5 \text{ V}$ and $G_v = 6$, that the THD+N in 20 Hz to 20 kHz range with $P_{\text{out}} = 0.45 \text{ W}$ is lower than 0.4%. In the following tables, you could find three other examples with values required for the demoboard. Remark: components with (*) marking are optional.

Application n°1: 20 Hz to 20 kHz bandwidth and 6 dB gain BTL power amplifier

Table 9. Components

Designator	Part type
R1	22 k / 0.125 W
R4	22 k / 0.125 W
R6	Short-circuit
R7	$(V_{\text{cc}}-V_{\text{f_led}})/I_{\text{f_led}}$
R8	10 k/0.125 W
C5	470 nF
C6	100 μF
C7	100 nF
C9	Short-circuit
C10	Short-circuit
C12	1 μF
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 connector 2.54 mm pitch
P1	PCB phono jack
D1	Led 3 mm
U1	TS4890ID or TS4890IS

Application n°2: 20 Hz to 20 kHz bandwidth and 20 dB gain BTL power amplifier

Table 10. Components 2

Designator	Part type
R1	110 k / 0.125 W
R4	22 k / 0.125 W
R6	Short-circuit
R7	$(V_{cc}-V_{f_led})/I_{f_led}$
R8	10 k/0.125 W
C5	470 nF
C6	100 μ F
C7	100 nF
C9	Short-circuit
C10	Short-circuit
C12	1 μ F
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 connector 2.54 mm pitch
P1	PCB phono jack
D1	Led 3 mm
U1	TS4890ID or TS4890IS

Application n°3: 50 Hz to 10 kHz bandwidth and 10 dB gain BTL power amplifier

Table 11. Components 3

Designator	Part type
R1	33 k / 0.125 W
R2	Short-circuit
R4	22 k / 0.125 W
R6	Short-circuit
R7	$(V_{cc}-V_{f_led})/I_{f_led}$
R8	10 k/0.125 W
C2	470 nF
C5	150 nF
C6	100 μ F

Table 11. Components 3

Designator	Part type
C7	100 nF
C9	Short-circuit
C10	Short-circuit
C12	1 μ F
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 connector 2.54 mm pitch
P1	PCB phono jack
D1	Led 3 mm
U1	TS4890ID or TS4890IS

Application n°4: differential inputs BTL power amplifier

In this configuration, we need to place these components: R1, R4, R5, R6, R7, C4, C5, C12.

We have also: R4 = R5, R1 = R6, C4 = C5. The gain of the amplifier is:

$$G_{VDIFF} = 2 \frac{R1}{R4}$$

For Vcc=5 V, a 20 Hz to 20 kHz bandwidth and 20 dB gain BTL power amplifier you could follow the bill of material below:

Table 12. Components 4

Designator	Part type
R1	110 k / 0.125 W
R4	22 k / 0.125 W
R5	22 k / 0.125 W
R6	Short-circuit
R7	(Vcc-Vf_led)/If_led
R8	10 k/0.125 W
C4	470 nF
C5	470 nF
C6	100 μ F
C7	100 nF
C9	Short-circuit
C10	Short-circuit

Table 12. Components 4

Designator	Part type
C12	1 μ F
D1	Led 3 mm
S1, S2, S6, S7	2 mm insulated plug 10.16 mm pitch
S8	3 connector 2.54 mm pitch
P1, P2	PCB phono jack
U1	TS4890ID or TS4890IS

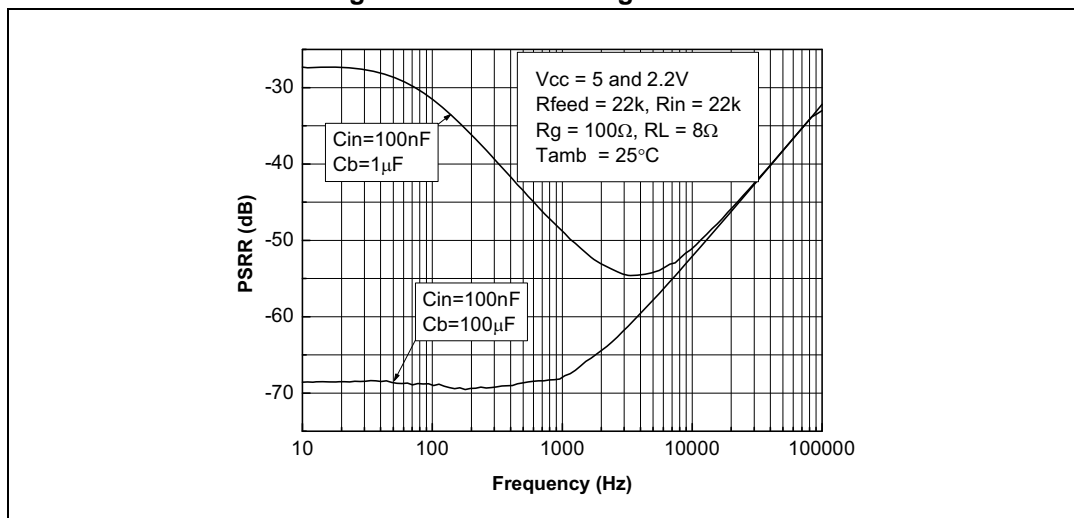
How to use the PSRR curves

We have finished a design and we have chosen for the components:

- $R_{in} = R_{feed} = 22\text{ k}\Omega$
- $C_{in} = 100\text{ nF}$
- $C_b = 1\text{ }\mu\text{F}$

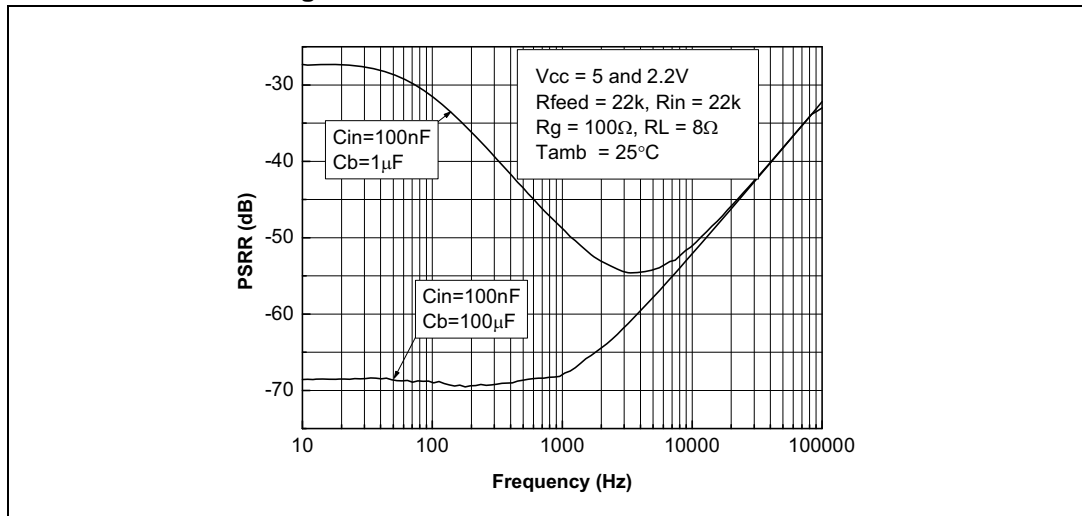
Now, in [Figure 16](#), we can see the PSRR (input grounded) vs frequency curves. At 217 Hz, we have a PSRR value of -36 dB. In reality we want a value about -70dB. So, we need a gain of 34 dB. Now, in [Figure 15](#) we can see the effect of C_b on the PSRR (input grounded) vs frequency. With $C_b = 100\text{ }\mu\text{F}$, we can reach the -70 dB value. The process to obtain the final curve ($C_b = 100\text{ }\mu\text{F}$, $C_{in} = 100\text{ nF}$, $R_{in} = R_{feed} = 22\text{ k}\Omega$) is a simple transfer point by point on each frequency of the curve on [Figure 16](#) to the curve on [Figure 15](#). The measurement result is shown on the next figure.

Figure 109. PSRR changes with C_b



The PSRR is the power supply rejection ratio. It is a kind of SVR in a determined frequency range. The PSRR of a device, is the ratio between a power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

Figure 110. PSRR measurement schematic



Principle of operation

- We fixed the DC voltage supply (V_{cc})
- We fixed the AC sinusoidal ripple voltage (V_{ripple})
- No bypass capacitor C_s is used

The PSRR value for each frequency is:

$$PSRR(dB) = 20 \times \text{Log}_{10} \left[\frac{\text{Rms}(V_{ripple})}{\text{Rms}(V_{s_-} - V_{s_+})} \right]$$

Remark: The measure of the Rms voltage is not an Rms selective measure but a full range (2 Hz to 125 kHz) Rms measure. It means that we measure the effective Rms signal + the noise.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.1 SO8 package information (TS4890IDT)

Figure 111. SO8 package outline

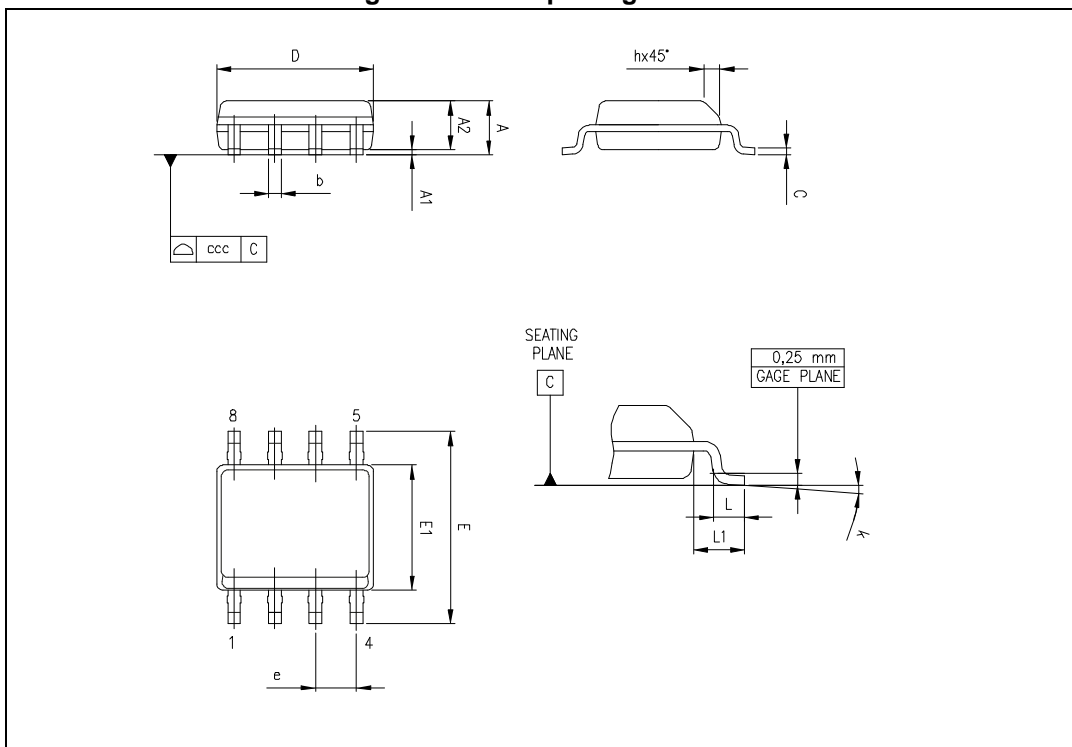


Table 13. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197

Table 13. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0					8°
ccc			0.1			0.004

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 MiniSO8 package information (TS4890IST)

Figure 112. MiniSO8 package outline

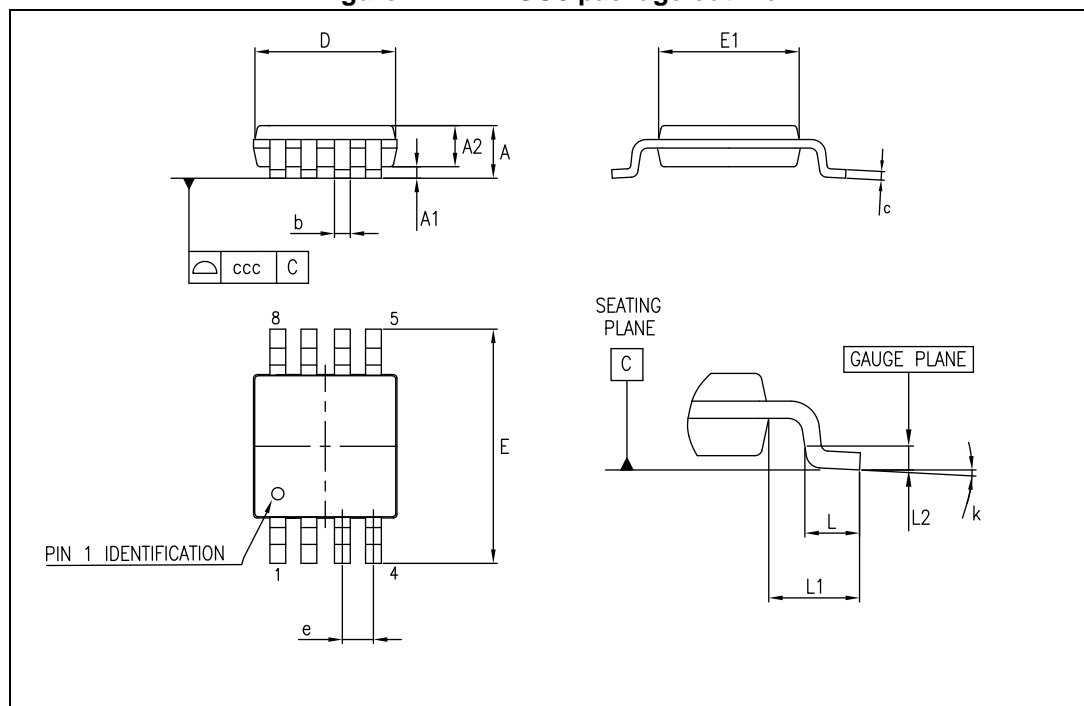


Table 14. MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7 Revision history

Table 15. Document revision history

Date	Revision	Changes
15-Feb-2019	7	Removed DFN8 package. Updated the document accordingly

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