GENERAL DESCRIPTION

The XRP6124 is a non synchronous step down (buck) controller for up to 5Amps point of loads. A wide 3V to 30V input voltage range allows for single supply operations from industry standard 3.3V, 5V, 12V and 24V power rails.

With a proprietary Constant On-Time (COT) control scheme, the XRP6124 provides extremely fast line and load transient response while the operating frequency remains nearly constant. It requires no loop compensation hence simplifying circuit implementation and reducing overall component count. The XRP76124 also implements an emulated ESR circuitry allowing usage of ceramic output capacitors and insuring stable operations without the use of extra external components.

Built-in soft start prevents high inrush currents while under voltage lock-out and output short protections insure safe operations under abnormal operating conditions.

The XRP6124 is available in a RoHS compliant, green/halogen free space-saving 5-pin SOT23 package.

APPLICATIONS

- Point of Load Conversions
- Audio-Video Equipment
- Industrial and Medical Equipment
- Distributed Power Architecture

FEATURES

- 5A Point-of-Load Capable
  - Down to 1.2V Output Voltage Conversion
- Wide Input Voltage Range
  - 3V to 18V: XRP6124
  - 4.5V to 30V: XRP6124HV
- Constant On-Time Operations
  - Constant Frequency Operations
  - No External Compensation
  - Supports Ceramic Output Capacitors
- Built-in 2ms Soft Start
- Short Circuit Protection
- <1µA shutdown current
- RoHS Compliant, Green/Halogen Free 5-pin SOT23 Package

TYPICAL APPLICATION DIAGRAM

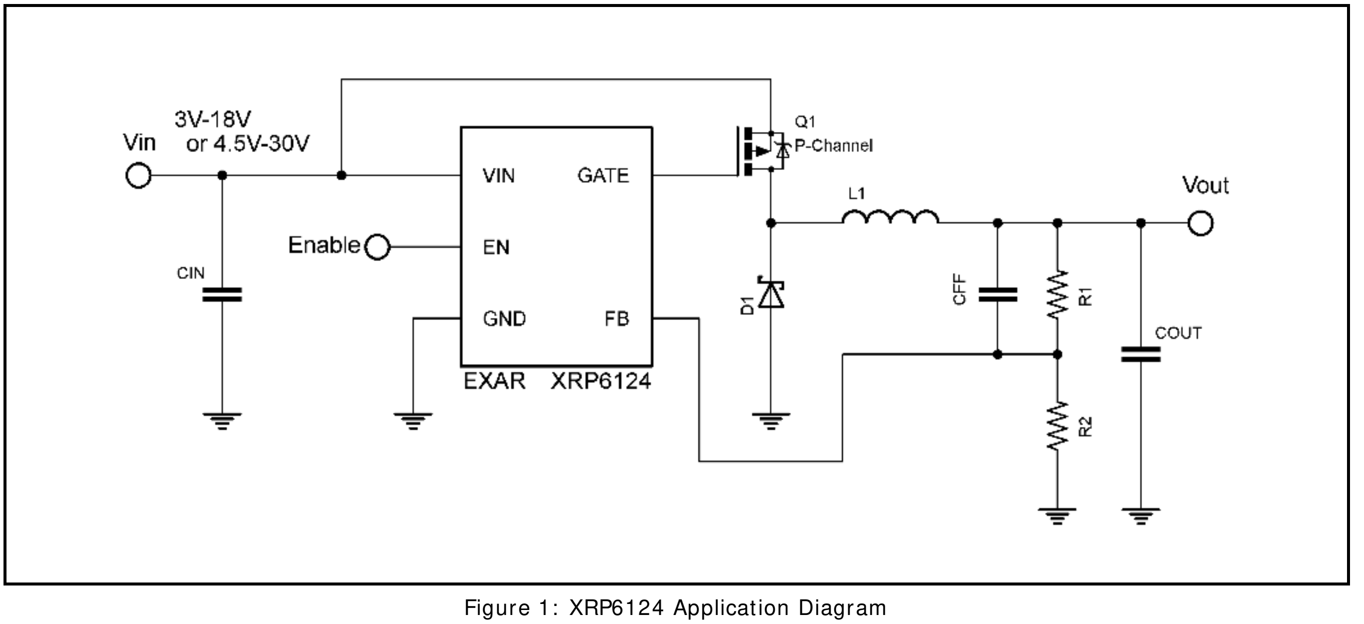


Figure 1: XRP6124 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN} (XRP6124) .... -0.3V to 20V
V_{IN} (XRP6124HV) .... -0.3V to 32V
GATE .... VIN-GATE<8V
FB, EN .... -0.3V to 5.5V
Storage Temperature .... -65°C to 150°C
Power Dissipation .... Internally Limited
Lead Temperature (Soldering, 10 sec) .... 300°C
ESD Rating (HBM - Human Body Model) 2kV

OPERATING RATINGS

Input Voltage Range V_{IN} (XRP6124)................3.0V to 18V
Input Voltage Range V_{IN} (XRP6124HV)............4.5V to 30V
Junction Temperature Range ....-40°C to 125°C
Thermal Resistance θ_{JA} ....191°C/W

ELECTRICAL SPECIFICATIONS

Specifications are for an Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 3.0V to 18V, T_J = –40°C to 125°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
UVLO Turn-On Threshold	2.5	2.8	3.0	V	•	XRP6124
UVLO Turn-On Threshold	3.8	4.2	4.5	V	•	XRP6124HV
UVLO Hysteresis		0.1		V		
Operating Input Voltage Range	3.0		18	V	•	XRP6124
	4.5		30	V	•	XRP6124HV
Shutdown VIN Current		1.5	3	µA		EN=0V, V_{IN}=12V
Operating VIN Current		0.5	1	mA		VFB=1.2V and after fault
Reference Voltage	0.792	0.8	0.808	V		
	0.784	0.8	0.816	V	•	
VSC_TH, Feedback pin Short Circuit Latch Threshold	0.50	0.55	0.65	V	•	
T_{ON}, Switch On-Time	0.4	0.5	0.6	µs	•	V_{IN}=12V, XRP6124
T_{ON}, Switch On-Time	0.4	0.5	0.6	µs	•	V_{IN}=24V, XRP6124HV
T_{OFF_MIN}, Minimum Off-Time		250	350	ns	•	V_{IN}=12V
Soft Start Time		2		ms		
EN Turn-On Threshold	2			V		
EN Turn-Off Threshold			1	V		
EN Bias Current		0.01	0.1	µA		
Gate Driver Pull-Down Resistance		6	9	Ω		
Gate Driver Pull-up Resistance		5	8	Ω		
tr, gate rise time		45		ns		C_{GATE}=1nF
tf, gate fall time		35		ns		C_{GATE}=1nF
VIN - GATE voltage difference	5.5	6.4	8	V	•	VIN=12V
VIN - GATE voltage difference	2.6			V	•	VIN=3.0V

BLOCK DIAGRAM

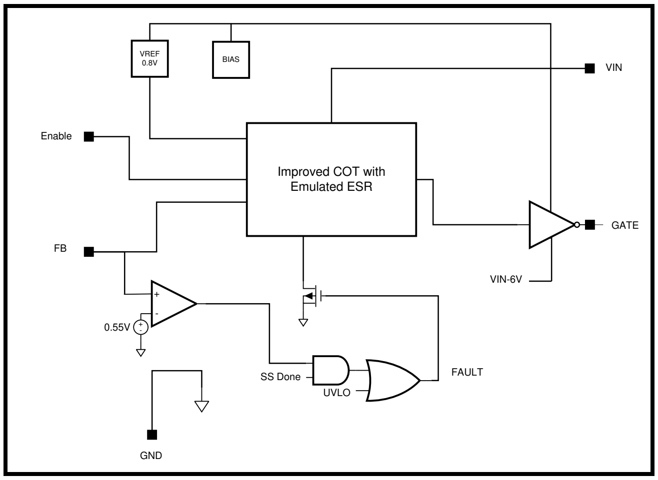


Figure 2: XRP6124 Block Diagram

PIN ASSIGNMENT

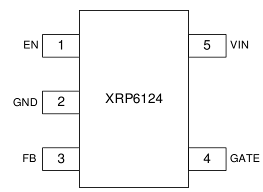


Figure 3: XRP6124 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
EN	1	Enable Pin. Actively pull high to enable the part.
GND	2	Ground
FB	3	Feedback pin
GATE	4	Gate Pin. Connect to gate of PFET. This pin pulls the gate of the PFET approximately 6V below Vin in order to turn on the FET. For 6V>VIN>3V the gate pulls to within 0.4V of ground. Therefore a PFET with a gate rating of 2.6V or lower should be used.
VIN	5	Input Voltage

ORDERING INFORMATION(1)

Part Number	Operating Temperature Range	Lead-Free	Package	Packing Method	Note 1
XRP6124ESTR0.5-F	-40°C≤T_J≤125°C	Yes(2)	5-pin SOT23	Tape & Reel	0.5µs/18V max
XRP6124HVESTR0.5-F					0.5µs/30V max
XRP6124EVB	XRP6124 Evaluation Board				
XRP6124HVEVB	XRP6124HV Evaluation Board				

NOTES:

1.Refer to www.exar.com/XRP6124 for most up-to-date Ordering Information

2. Visit www.exar.com for additional information on Environmental Rating.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at $T_J = T_A = 25°C$, unless otherwise specified – Curves are based on Schematic and BOM from Application Information section of this datasheet. Refer to figure 20 for XRP6124 and to figure 21 for XRP6124HV.

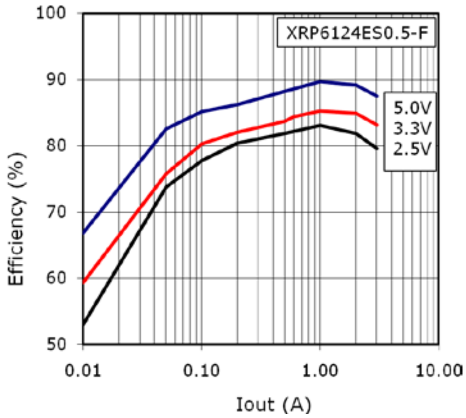


Fig. 4: Efficiency versus I_{OUT}, V_{IN}= 12V

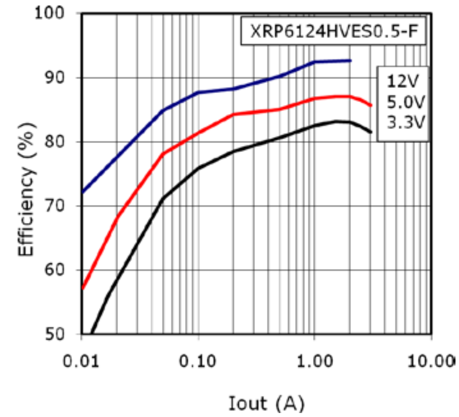


Fig. 5: Efficiency versus I_{OUT}, V_{IN}= 24V

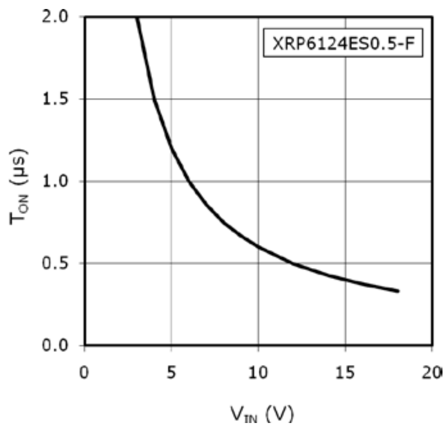


Fig. 6: T_{ON} versus V_{IN}

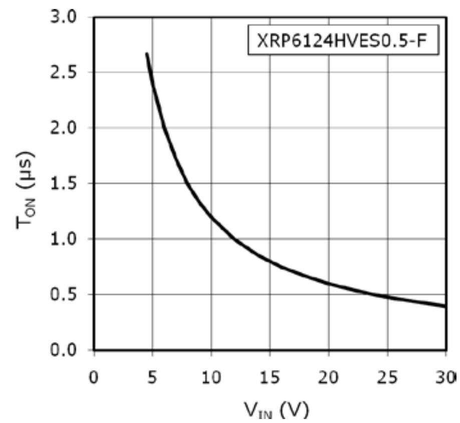


Fig. 7: T_{ON} versus V_{IN}

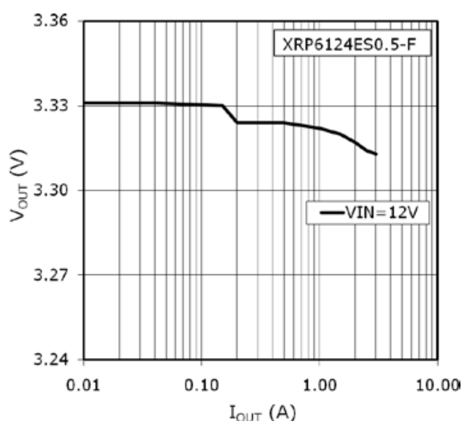


Fig. 8: Load Regulation

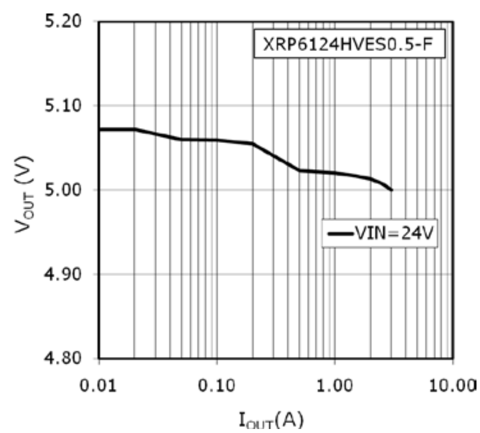


Fig. 9: Load Regulation

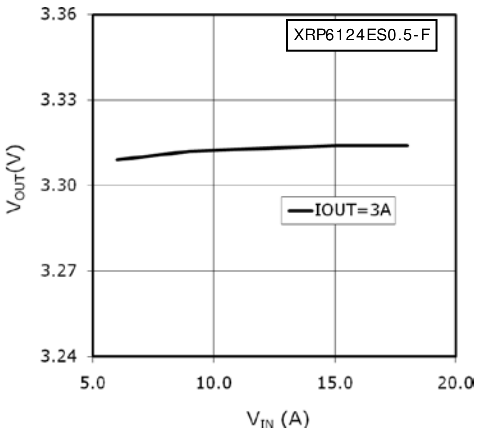


Fig. 10: Line Regulation

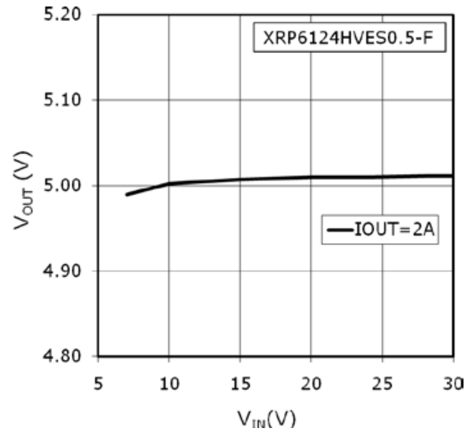


Fig. 11: Line Regulation

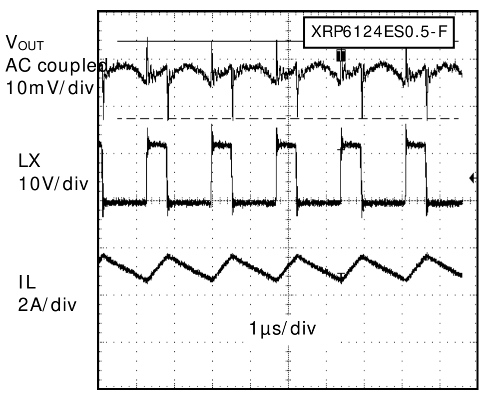


Fig. 12: Steady state, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A

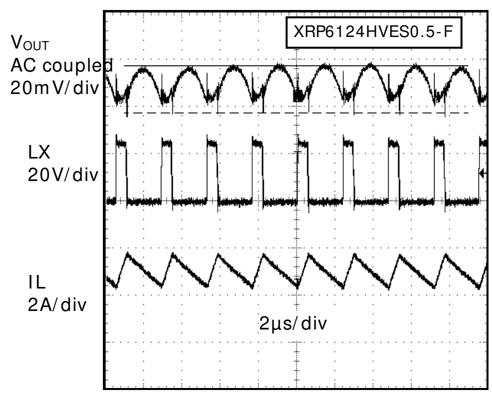


Fig. 13: Steady state, V_{IN} = 24V, V_{OUT} = 5.0V, I_{OUT} = 3A

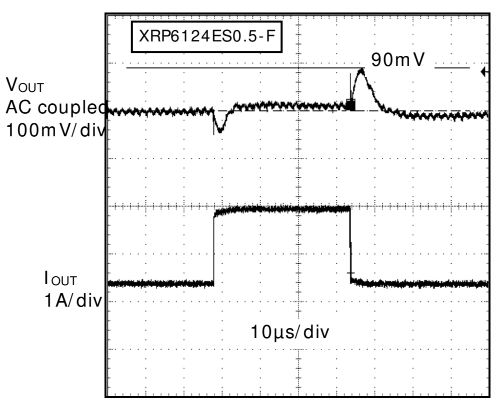


Fig. 14: Load step transient response, 1.4A-3A-1.4A

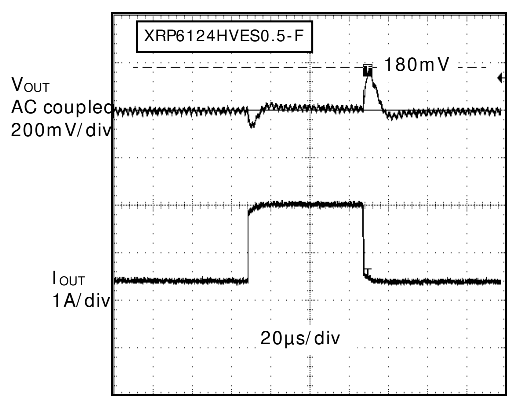


Fig. 15: Load step transient response, 1.4A-3A-1.4A

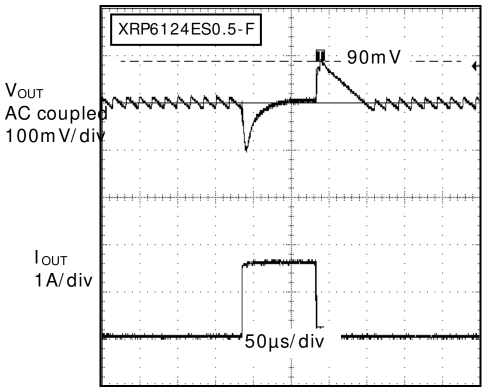


Fig. 16: Load step transient response corresponding to a CCM-DCM transition, 0.05A-1.6A-0.05A

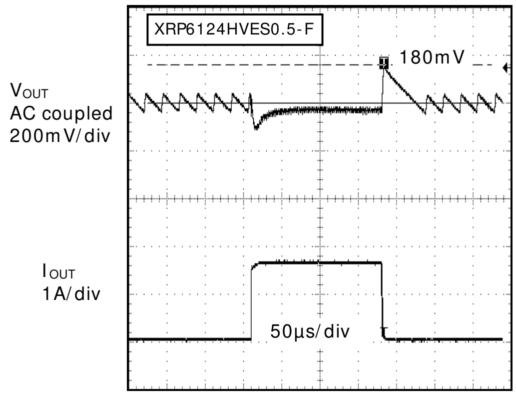


Fig. 17: Load step transient response corresponding to a CCM-DCM transition, 0.05A-1.6A-0.05A

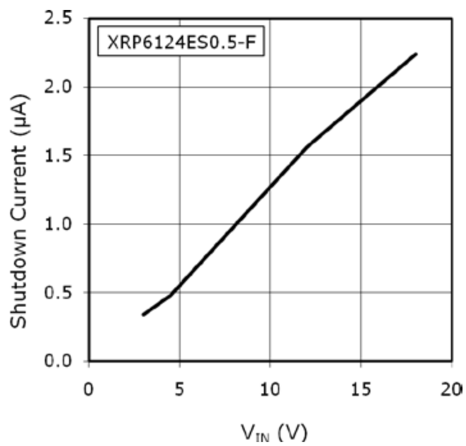


Fig. 18: Shutdown current versus V_{IN}, V_{EN} = 0V

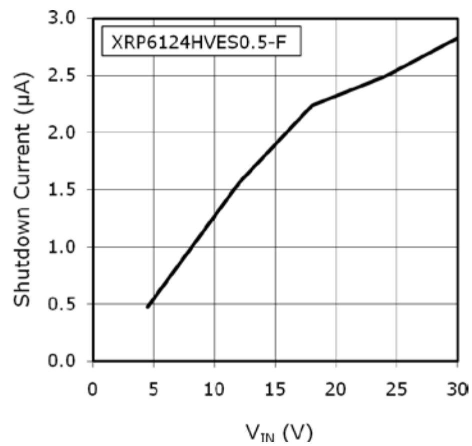


Fig. 19: Shutdown current versus V_{IN}, V_{EN} = 0V

THEORY OF OPERATION

THEORY OF OPERATION

The XRP6124 utilizes a proprietary Constant On-Time (COT) control with emulated ESR. The on-time is internally set and automatically adjusts during operation, inversely with the voltage V_{IN}, in order to maintain a constant frequency. Therefore the switching frequency is independent of the inductor and capacitor size, unlike hysteretic controllers. The emulated ESR ramp allows the use of ceramic capacitors for output filtering.

At the beginning of each cycle, the XRP6124 turns on the P-Channel FET for a fixed duration. The on-time is internally set and adjusted by V_{IN}. At the end of the on-time the FET is turned off, for a predetermined minimum off time $T_{OFF-MIN}$ (nominally 250ns). After the $T_{OFF-MIN}$ has expired the voltage at feedback pin FB is compared to a voltage ramp at the feedback comparators positive input. Once V_{FB} drops below the ramp voltage, the FET is turned on and a new cycle starts. This voltage ramp constitutes an emulated ESR and makes possible the use of ceramic capacitors, in addition to other capacitors, as output filter for the buck converter.

VOLTAGE OPTIONS

The XRP6124 is available in two voltage options as shown in table 1. The low-voltage and high-voltage options have T_{ON} of 0.5µs at $12V_{IN}$ and $24V_{IN}$ respectively. Note that T_{ON} is inversely proportional to V_{IN}. The constant of proportionality K, for each voltage option is shown in table 1. Variation of T_{ON} versus V_{IN} is shown graphically in figures 6 and 7.

Voltage rating (V)	Part Number	T_{ON} (µs)	$K=T_{ON} x V_{IN}$ **(µs.V)**
3-18	XRP6124ES0.5-F	0.5 @ $12V_{IN}$	6
4.5-30	XRP6124HVES0.5-F	0.5 @ $24V_{IN}$	12

Table 1 : XRP6124 voltage options

For a buck converter the switching frequency fs can be expressed in terms of V_{IN}, V_{OUT} and T_{ON} as follows:

$$fs = \frac{V_{OUT}}{V_{IN} \times T_{ON}}$$

Since for each voltage option, the product of V_{IN} and T_{ON} is the constant K shown in table 1, then switching frequency is determined by V_{OUT} as shown in table 2.

V_{OUT}	Switching frequency fs(kHz)	
	XRP6124ES0.5-F	XRP6124HVES0.5-F
1.2	200	100
1.5	250	125
1.8	300	150
2.5	417	208
3.3	550	275
5.0	833	417
12	---	1000

Table 2: Switching frequency fs
for the XRP6124 voltage options

Where it is advantageous, the high-voltage option may be used for low-voltage applications. For example a $12V_{IN}$ to $5V_{OUT}$ conversion using a low-voltage option will result in switching frequency of 833kHz as shown in table 2. If it is desired to increase the converter efficiency, then switching losses can be reduced in half by using a high-voltage option operating at a switching frequency of 417kHz.

V_{OUT}	Maximum Output Current I_{OUT}(A)				
	XRP6124ES0.5-F			XRP6124HVES0.5-F	
	$3.3V_{IN}$	$5.0V_{IN}$	$12V_{IN}$	$18V_{IN}$	$24V_{IN}$
1.2	5	5	4	---	---
1.5	5	5	4	4	---
1.8	5	5	4	4	4
2.5	4	4	4	4	4
3.3	---	4	3	4	4
5.0	---	---	3	3	3
12	---	---	---	2	2

Table 3: Maximum recommended I_{OUT}

SHORT-CIRCUIT PROTECTION

The purpose of this feature is to prevent an accidental short-circuit at the output from damaging the converter. The XRP6124 has a short-circuit comparator that constantly monitors the feedback node, after soft-start is finished. If the feedback voltage drops below 0.55V, equivalent to output voltage dropping below 69% of nominal, the comparator will trip causing the IC to latch off. In order to restart the XRP6124, the input voltage has to be reduced below UVLO threshold and then increased to its normal operating point.

SOFT-START

To limit in-rush current the XRP6124 has an internal soft-start. The nominal soft-start time is 2ms and commences when V_{IN} exceeds the UVLO threshold. As explained above, the short-circuit comparator is enabled as soon as soft-start is complete. Therefore if the input voltage has a very slow rising edge such that at the end of soft-start the output voltage has not reached 69% of its final value then the XRP6124 will latch-off.

ENABLE

By applying a logic-level signal to the enable pin EN the XRP6124 can be turned on and off. Pulling the enable below 1V shuts down the controller and reduces the V_{IN} leakage current to 1.5µA nominal as seen in figure 18. Enable signal should always be applied after the input voltage or concurrent with it. Otherwise XRP6124 will latch up. In applications where an independent enable signal is not available, a Zener diode can be used to derive V_{EN} from V_{IN}.

DISCONTINUOUS CONDUCTION MODE, DCM

Because XRP6124 is a non-synchronous controller, when load current I_{OUT} is reduced to less than half of peak-to-peak inductor current ripple ΔIL, the converter enters DCM mode of operation. The switching frequency fs is now I_{OUT} dependent and no longer governed by the relationship shown in table 2. As I_{OUT} is decreased so does fs until a minimum switching frequency, typically in the range of few hundred Hertz, is reached at no load. This contributes to good converter efficiency at light load as seen in figures 4 and 5. The reduced fs corresponding to light load, however, increases the output voltage ripple and causes a slight increase in output voltage as seen in figures 8 and 9. Another effect of reduced fs at light load is slow down of transient response when a load step transitions from a high load to a light load. This is shown in figures 16 and 17.

APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

Use an external resistor divider to set the output voltage. Program the output voltage from:

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

where:

R1 is the resistor between V_{OUT} and FB

R2 is the resistor between FB and GND (nominally 2kΩ)

0.8V is the nominal feedback voltage.

FEED-FORWARD CAPACITOR CFF

CFF, which is placed in parallel with R1, provides a low-impedance/high-frequency path for the output voltage ripple to be transmitted to FB. It also helps get an optimum transient response. An initial value for CFF can be calculated from:

$$CFF = \frac{1}{2 \times \pi \times fs \times 0.1 \times R1}$$

where:

fs is the switching frequency from table 2

This value can be adjusted as necessary to provide an optimum load step transient response.

OUTPUT INDUCTOR

Select the output inductor L1 for inductance L, DC current rating I_{DC} and saturation current rating I_{SAT}. I_{DC} should be larger than regulator output current. I_{SAT}, as a rule of thumb, should be 50% higher than the regulator output current. Calculate the inductance from:

$$L = (V_{IN} - V_{OUT})\left(\frac{V_{OUT}}{\Delta I_L \times fs \times V_{IN}}\right)$$

Where:

ΔI_L is peak-to-peak inductor current ripple nominally set to 30% of I_{OUT}

f_S is nominal switching frequency from table 2

OUTPUT CAPACITOR C_{OUT}

Select the output capacitor for voltage rating, capacitance C_{OUT} and Equivalent Series Resistance ESR. The voltage rating, as a rule of thumb, should be twice the output voltage. When calculating the required capacitance, usually the overriding requirement is current load-step transient. If the unloading transient requirement (i.e., when I_{OUT} transitions from a high to a low current) is met, then usually the loading transient requirement (when I_{OUT} transitions from a low to a high current) is met as well. Therefore calculate the C_{OUT} capacitance based on the unloading transient requirement from:

$$C_{OUT} = L \times \left(\frac{I_{High}^2 - I_{LOW}^2}{(V_{OUT} + V_{transient})^2 - V_{OUT}^2}\right)$$

Where:

L is the inductance calculated in the preceding step

I_{High} is the value of I_{OUT} prior to unloading. This is nominally set equal to regulator current rating.

I_{Low} is the value of I_{OUT} after unloading. This is nominally set equal to 50% of regulator current rating.

$V_{transient}$ is the maximum permissible voltage transient corresponding to the load step mentioned above. $V_{transient}$ is typically specified from 3% to 5% of V_{OUT}.

ESR of the capacitor has to be selected such that the output voltage ripple requirement $V_{OUT(ripple)}$, nominally 1% of V_{OUT}, is met. Voltage ripple $V_{OUT(ripple)}$ is composed mainly of two components: the resistive ripple due to ESR and capacitive ripple due to C_{OUT} charge transfer. For applications requiring low voltage ripple, ceramic capacitors are recommended because of their low ESR which is typically in the range of 5mΩ. Therefore $V_{OUT(ripple)}$ is mainly capacitive. For ceramic capacitors calculate the $V_{OUT(ripple)}$ from:

$$V_{OUT(ripple)} = \frac{\Delta I_L}{8 \times C_{OUT} \times fs}$$

Where:

C_{OUT} is the value calculated above

If tantalum or electrolytic capacitors are used then $V_{OUT(ripple)}$ is essentially a function of ESR:

$$V_{OUT(ripple)} = \Delta I_L \times ESR$$

INPUT CAPACITOR C_{IN}

Select the input capacitor for voltage rating, RMS current rating and capacitance. The voltage rating, as a rule of thumb, should be 50% higher than the regulator's maximum input voltage. Calculate the capacitor's current rating from:

$$I_{CIN,RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Where:

I_{OUT} is regulator's maximum current

D is duty cycle ($D = V_{OUT}/V_{IN}$)

Calculate the C_{IN} capacitance from:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{fs \times V_{IN}^2 \times \Delta V_{IN}}$$

Where:

ΔV_{IN} is the permissible input voltage ripple, nominally set to 1% of V_{IN}.

TYPICAL APPLICATIONS

12V TO 3.3V / 3A CONVERSION

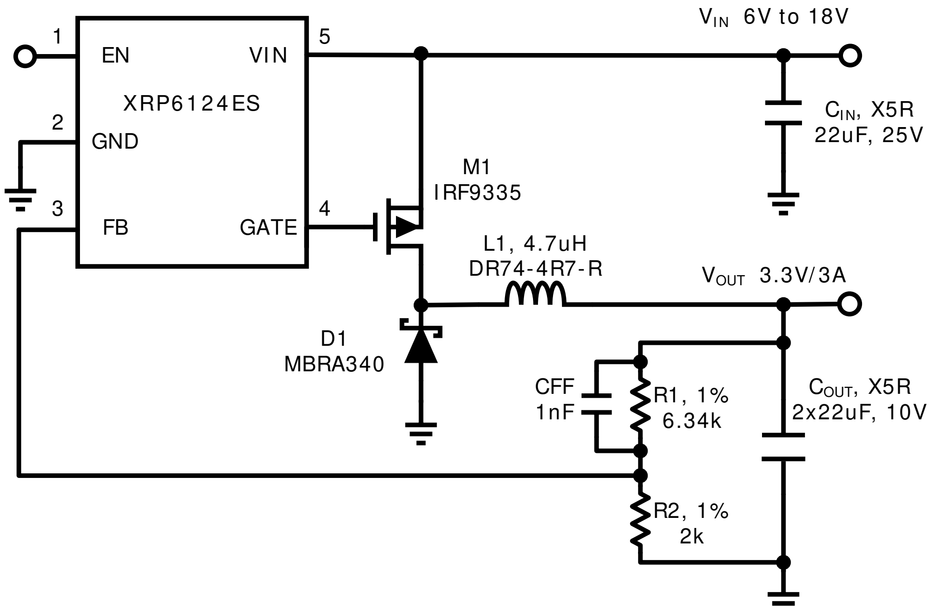


Fig. 20: 12V to 3.3V/3A regulator

24V TO 5V / 3A CONVERSION

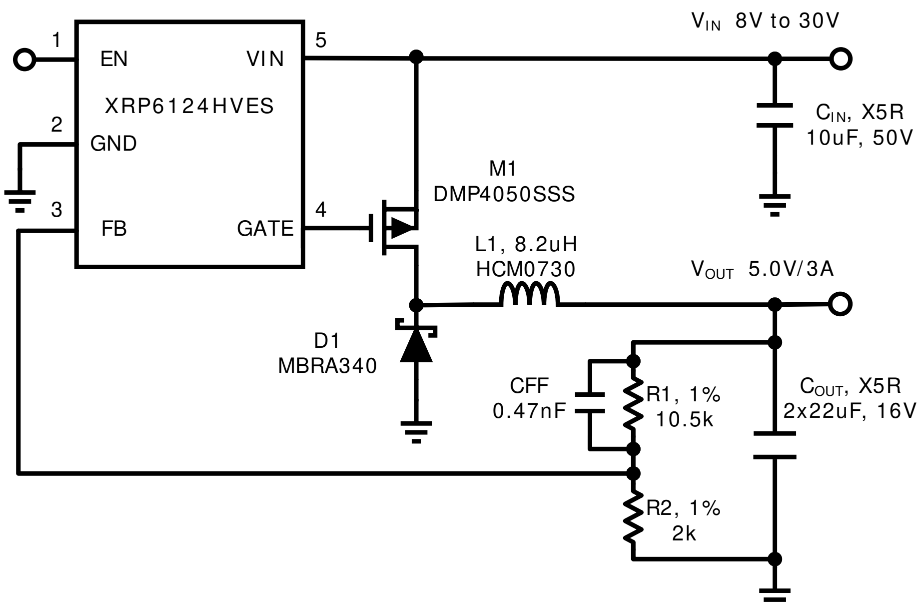
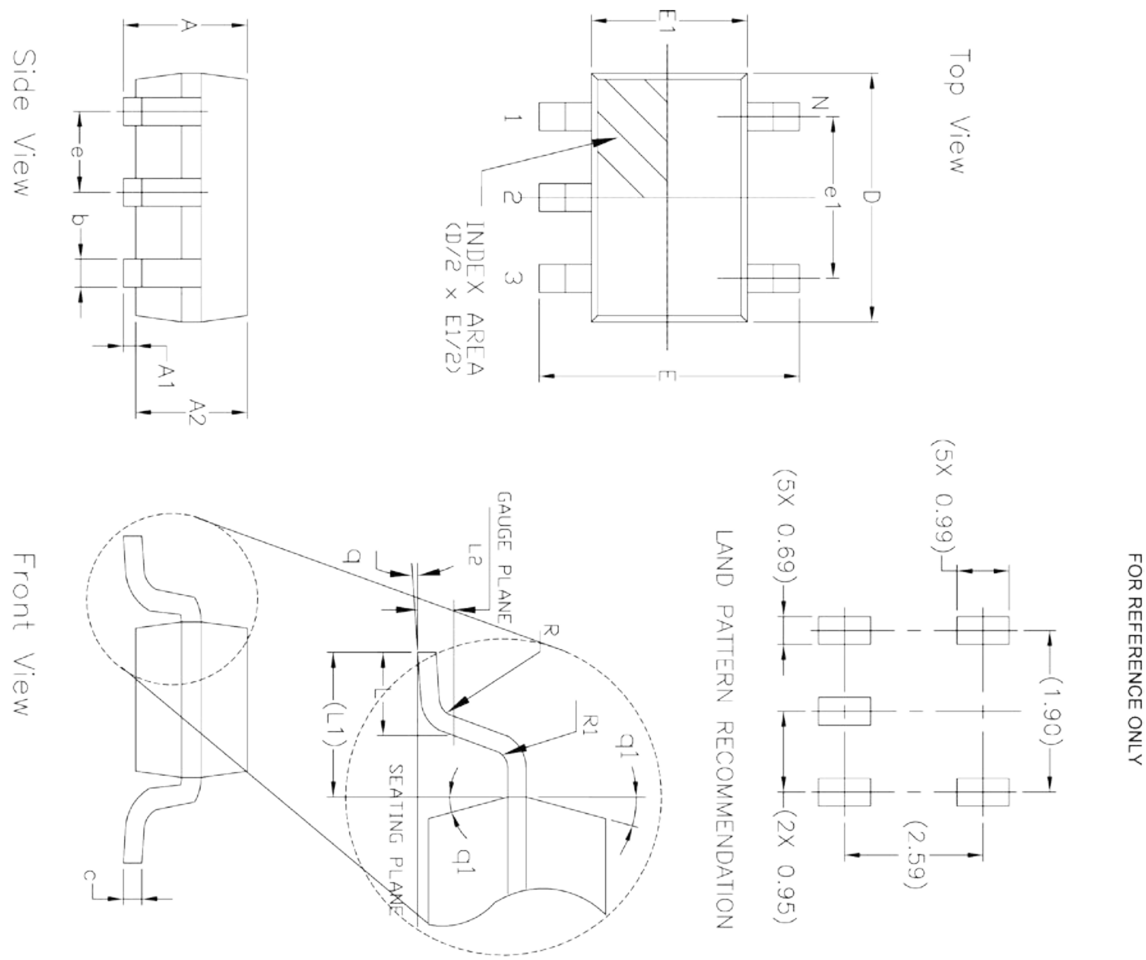


Fig. 21: 24V to 5V/3A regulator

MECHANICAL DIMENSIONS

5-PIN SOT23



5 Pin SOT-23 JEDEC MO-178 Variation AA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.45	—	—	0.057
A1	0.00	—	0.15	0.000	—	0.006
A2	0.90	1.15	1.30	0.036	0.045	0.051
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.22	0.003	—	0.009
D	2.90 BSC			0.115 BSC		
E	2.80 BSC			0.111 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
q	0°	4°	8°	0°	4°	8°
q1	5°	10°	15°	5°	10°	15°
N	5			5		

Drawing No: POD-00000025
Revision: B

REVISION HISTORY

Revision	Date	Description
1.0.0	01/26/2011	Initial release of datasheet
1.1.0	01/31/2011	Corrected typo (changed V to I) on formula under Input Capacitor C_{IN} paragraph
1.1.1	05/24/2018	Updated to MaxLinear logo. Updated format and Ordering Information.

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