User's Guide
SLVU273–September 2008

Using the TPS55386EVM-363 A 12V Input, 5.0V & 3.3V Output, 3A Non-Synchronous Buck Converter

Contents

1 Introduction 2
1.1 Description 2
1.2 Applications 2
1.3 Features 2
2 TPS55386EVM-363 Electrical Performance Specifications 3
3 Schematic 4
3.1 Sequencing Jumper (JP3) 5
3.2 Enable Jumpers (JP1 and JP2) 5
3.3 Error Amplifier Outputs 5
3.4 Test Point Descriptions 5
4 Test Set UP 7
4.1 Equipment 7
4.2 Equipment Setup 8
4.3 Start Up / Shut Down Procedure 10
4.4 Output Ripple Voltage Measurement Procedure 10
4.5 Control Loop Gain and Phase Measurement Procedure 11
4.6 Equipment Shutdown 11
5 TPS55386EVM-363 Typical Performance Data and Characteristic Curves 11
5.1 Efficiency 12
5.2 Line and Load Regulation 12
5.3 Switch Node and Output Ripple Voltage 13
5.4 Output Ripple Voltage 13
5.5 CONTROL LOOP BODE PLOT 14
6 EVM Assembly Drawings and Layout 15
7 List of Materials 18

List of Figures

1 TPS55386EVM-363 Schematic (For Reference Only, See Table 4: Bill of Materials for Specific Values) 4
2 TPS55386EVM-363 Recommended Test Set-Up 9
3 Output Ripple Measurement – Tip and Barrel using TP3 and TP4 or TP18 and TP19 9
4 Control Loop Measurement Setup 10
5 TPS55386EVM-363 Efficiency vs Load Current 12
6 TPS55386EVM-363 Output Voltage vs Load Current 12
7 TPS55386EVM-363 Output Voltage Ripple 13
8 Output Ripple Voltage Measured at Test Points 13
9 Output Ripple Voltage Measured at Test Points 14
10 TPS55386EVM-363 Gain and Phase vs Frequency 14
11 TPS55386EVM-363 Component Placement (Viewed from Top) 15
12 TPS55386EVM-363 Silkscreen (Viewed from Top) 15
13 TPS55386EVM-363 Top Copper (Viewed from Top) 16
14 TPS55386EVM-363 Bottom Copper (X-Ray View from Top) 16
15 TPS55386EVM-363 Internal 1 (X-Ray View from Top) 17
16 TPS55386EVM-363 Internal 2 (X-Ray View from Top) 17

List of Tables

1 TPS55386EVM-363 Electrical and Performance Specifications 3
2 Test Point Descriptions 5
3 TPS55386EVM-363 Bill of Materials 18

1 Introduction

The TPS55383EVM-363 evaluation module (EVM) is a dual non-synchronous buck converter providing fixed 5.0V and 3.3V output at up to 3A each from a 12-V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS55386 600kHz Dual Non-Synchronous Buck Converter with integral high-side FET.

1.1 Description

TPS55386EVM-363 is designed to use a regulated 12V (+10% /–20%) bus to produce two regulated power rails, 5.0V and 3.3V at up to 3A of load current each. TPS55386EVM-363 is designed to demonstrate the TPS55386 in a typical 12-V bus system while providing a number of test points to evaluate the performance of the TPS55386 in a given application. The EVM can be modified to other input or output voltages by changing some of the components.

1.2 Applications

- Non-Isolated Low Current Point of Load and Voltage bus converters.
- Consumer Electronics
- LCD TV
- Computer Peripherals
- Digital Set Top Box

1.3 Features

- 12 V +10% /–20% input range
- 5.0 V and 3.3 V fixed output voltage, adjustable with resistor change
- 3Adc Steady State Output Current (3A Peak)
- 600kHz switching frequency (Fixed by TPS55386)
- Internal switching MOSFET and external Rectifier Diode.
- Double Sided 2 Active Layer PCB with all components on top side (Test Point signals routed on internal layers)
- Active Converter area of less than 2.5 square inch < 1.15” × 2.15”
- Convenient test points for probing switching waveforms and non-invasive loop response testing

2 TPS55386EVM-363 Electrical Performance Specifications

Table 1. TPS55386EVM-363 Electrical and Performance Specifications

Parameter		Notes and Conditions	Min	Nom	Max	Units
INPUT CHARACTERSTICS						
V_{IN}	Input Voltage		9.6	12	13.2	V
I_{IN}	Input Current	V_{IN} = Nom, I_{OUT} = Max	–	2.4	2.6	A
	No Load Input Current	V_{IN} = Nom, I_{OUT} = 0 A	–	12	20	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = Min to Max	4.0	4.2	4.4	V
OUTPUT CHARACTERSTICS						
V_{OUT1}	Output Voltage 1	V_{IN} = Nom, I_{OUT} = Nom	4.95	5.1	5.25	V
V_{OUT2}	Output Voltage 2	V_{IN} = Nom, I_{OUT} = Nom	3.20	3.3	3.40	V
	Line Regulation	V_{IN} = Min to Max	–	–	1%	
	Load Regulation	I_{OUT} = Min to Max	–	–	1%	
V_{OUT_ripple}	Output Voltage Ripple	V_{IN} = Nom, I_{OUT} = Max	–	–	50	mVpp
I_{OUT1}	Output Current 1	V_{IN} = Min to Max	0		3.0	A
I_{OUT2}	Output Current 2	V_{IN} = Min to Max	0		3.0	A
I_{OCP1}	Output Over Current Channel 1	V_{IN} = Nom, V_{OUT} = V_{OUT1}–5%	3.1	3.7	4.5	A
I_{OCP2}	Output Over Current Channel 2	V_{IN} = Nom, V_{OUT} = V_{OUT2}–5%	3.1	3.7	4.5	A
SYSTEMS CHARACTERSTICS						
F_{SW}	Switching Frequency		500	600	700	kHz
ηpk	Peak Efficiency	V_{IN} =Nom	–	90%	–	
η	Full Load Efficiency	V_{IN} =Nom, I_{OUT1} = I_{OUT1} = Max	–	85%	–	
Top	Operating Temperature Range	VI_{N} = Min to Max, I_{OUT} = Min to Max	0	25	60	°C

3 Schematic

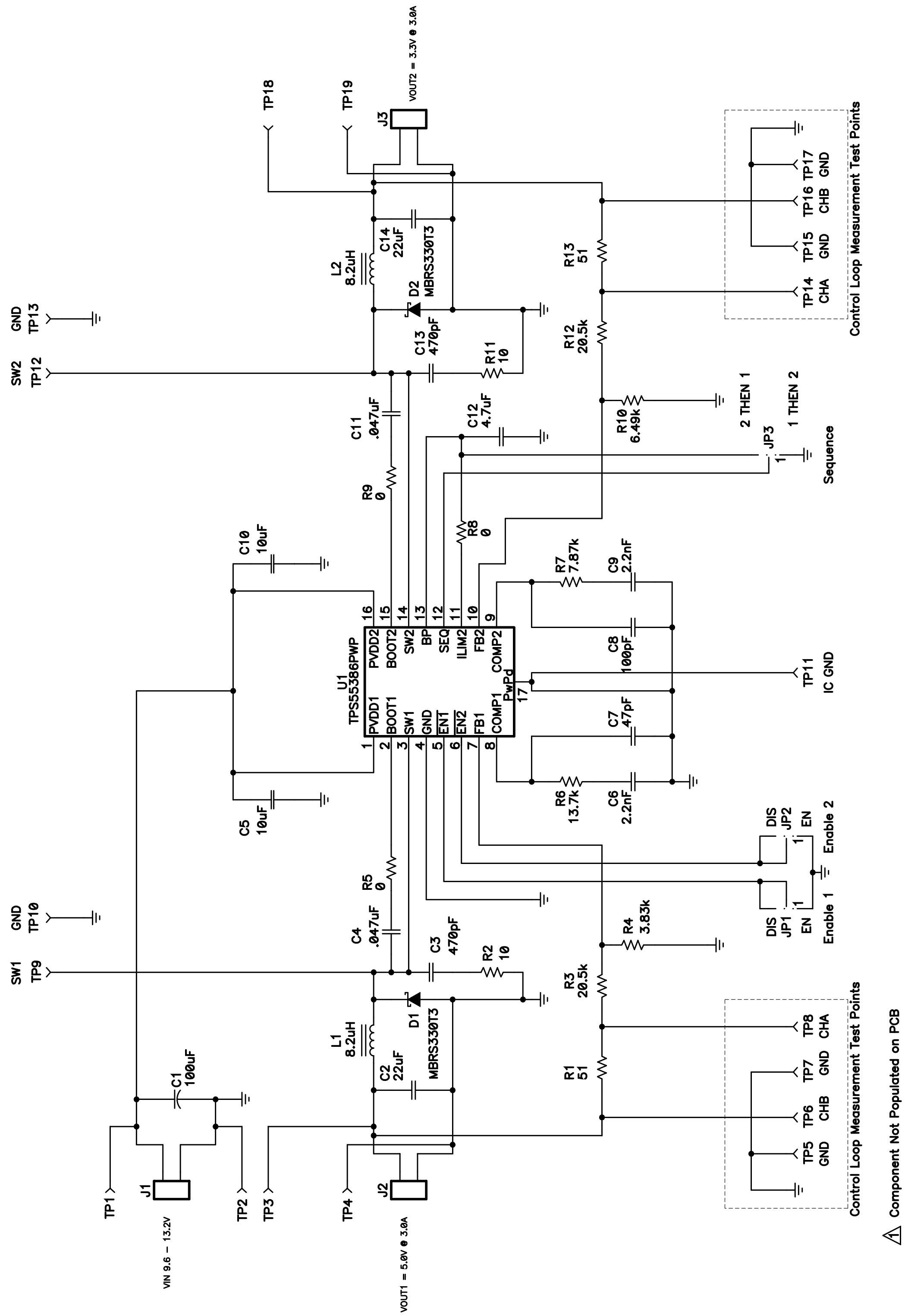


Figure 1. TPS55386EVM-363 Schematic
(For Reference Only, See Table 4: Bill of Materials for Specific Values)

3.1 Sequencing Jumper (JP3)

The TPS55386EVM-363 provides a 3 pin 100-mil header and shunt for programming the TPS55386's sequencing function. Placing the JP3 shunt in the Left Position connects the sequence pin to BP and sets the TPS55386 controller to sequence Channel 2 prior to Channel 1 when Enable 2 is activated. Placing the JP3 shunt in the Right Position connects the sequence pin to GND and sets the TPS55386 converter to sequence Channel 1 prior to Channel 1 when Enable 1 is activated. Removing the JP3 shunt disables sequencing and allows Channel 1 and Channel 2 to be enabled independently.

3.2 Enable Jumpers (JP1 and JP2)

TPS55386EVM-363 provides separate 3 pin 100-mil headers and shunts for exercising the TPS55386 Enable functions. When JP3 is removed placing the JP1 shunt in the Left Position connects EN1 to ground and turns on Output 1 and placing the JP2 shunt in the Left Position connects EN2 to ground and turns on Output 2.

When the JP3 shunt is in the LEFT position, placing the JP2 shunt in the LEFT position connects EN2 to ground and turns on first Output 2 and then Output 1.

When the JP3 shunt is in the RIGHT position, placing the JP1 shunt in the LEFT position connects EN1 to ground and turns on first Output 1 and then Output 2.

3.3 Error Amplifier Outputs

The output of the TPS55386 transconductance error amplifiers (COMP1 and COMP2) are sensitive to capacitive loading, including the typical 8-15pF capacitance added by an oscilloscope probe. No direct measurements of these signals should be attempted without using an external buffer to prevent loading of the control voltage.

3.4 Test Point Descriptions

Table 2. Test Point Descriptions

Test Point	Lable	Use	Section
TP1	VIN	Monitor Input Voltage	3.3.1
TP2	GND	Ground for Input Voltage	3.3.1
TP3	VOUT1	Monitor VOUT1 Voltage	3.3.2
TP4	GND	Ground for VOUT1 Voltage	3.3.2
TP5	GND	Ground for VOUT1 Channel B Loop Monitoring	3.3.3
TP6	CHB	VOUT1 Channel B for Loop Monitoring	3.3.3
TP7	GND	Ground for VOUT1 Channel A Loop Monitoring	3.3.3
TP8	CHA	VOUT1 Channel B for Loop Monitoring	3.3.3
TP9	SW1	Monitor Switching Node of Channel 1	3.3.4
TP10	GND	Ground for Switch Node of Channel 1	3.3.4
TP11	IC_GND	Monitor IC Ground	3.3.5
TP12	SW2	Monitor Switching Node of Channel 2	3.3.6
TP13	GND	Ground for Switch Node of Channel 2	3.3.6
TP14	CHA	VOUT2 Channel A for Loop Monitoring	3.3.7
TP15	GND	Ground for VOUT2 Channel A Loop Monitoring	3.3.7
TP16	CHB	VOUT2 Channel B for Loop Monitoring	3.3.7
TP17	GND	Ground for VOUT2 Channel B Loop Monitoring	3.3.7
TP18	VOUT2	Monitor VOUT2 Voltage	3.3.8
TP19	GND	Ground for VOUT2 Voltage	3.3.8

3.4.1 Input Voltage Monitoring (TP1 and TP2)

TPS55386EVM-363 provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and negative terminal to TP2.

3.4.2 Channel 1 Output Voltage Monitoring (TP3 and TP4)

TPS55386EVM-363 provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connectors. All output voltage measurements should be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive terminal to TP3 and negative terminal to TP4. For Output ripple measurements, TP3 and TP4 allow a user to limit the ground loop area by using the Tip and Barrel measurement technique shown in Figure 3. All output ripple measurements should be made using the Tip and Barrel measurement. . Even this Tip and Barrel measurement technique increases the measured switch edge noise. For improved output ripple measurement, measure the output ripple at the output capacitor (C5)

3.4.3 Channel 1 Loop Analysis (TP5, TP6, TP7 and TP8)

TPS55386EVM-363 contains a 51Ω series resistor (R1) in the feedback loop to allow for matched impedance signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (30mV or less) signal across R1 through TP6 and TP8. By monitoring the AC injection level at TP8 and the returned AC level at TP6, the power supply loop response can be determined.

3.4.4 Channel 1 Switching Waveforms (TP9 and TP10)

TPS55386EVM-363 provides a surface test pad and a local ground connection (TP10) for the monitoring of the channel 1 power stage switching waveform. Connect an Oscilloscope probe to TP9 to monitor the Switch Node voltage for channel 1. Test pads are used on the switch nodes to minimize radiated noise from the switch node.

3.4.5 TPS55386 IC Ground (TP11)

TPS55386EVM-363 provides a test point for the IC ground. To measure IC pin voltages, connect the ground of the oscilloscope probe to TP11.

3.4.6 Channel 2 Switching Waveforms (TP12 and TP13)

TPS55386EVM-363 provides a surface test pad and a local ground connection (TP13) for the monitoring of the channel 1 power stage switching waveform. Connect an Oscilloscope probe to TP12 to monitor the Switch Node voltage for channel 1. Test pads are used on the switch nodes to minimize radiated noise from the switch node.

3.4.7 Channel 2 Loop Analysis (TP14, TP15, TP16 and TP17)

TPS55386EVM-363 contains a 51 series resistor (R13) in the feedback loop to allow for matched impedance signal injection into the feedback for loop response analysis. An isolation transformer should be used to apply a small (30mV or less) signal across R13 through TP14 and TP16. By monitoring the AC injection level at TP14 and the returned AC level at TP16, the power supply loop response can be determined.

3.4.8 Output Voltage Monitoring (TP18 and TP19)

TPS55386EVM-363 provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connector losses. All output voltage measurements should be made between TP18 and TP19. To use TP18 and TP19, connect a voltmeter positive terminal to TP18 and negative terminal to TP19. For Output ripple measurements, TP18 and TP19 allow a user to limit the ground loop area by using the Tip and Barrel measurement technique shown in Figure 3 All output ripple measurements should be made using the Tip and Barrel measurement. Even this Tip and Barrel measurement technique increases the measured switch edge noise. For improved output ripple measurement, measure the output ripple at the output capacitor (C17)

4 Test Set UP

4.1 Equipment

4.1.1 Voltage Source

V_{IN}
The input voltage source (V_{IN}) should be a 0-15V variable DC source capable of 5Adc. Connect V_{IN} to J1 as shown in Figure 3.

4.1.2 Meters

A1: 0-3Adc, ammeter
V1: VIN, 0-15V voltmeter
V2: VOUT1 0-6V voltmeter
V3: VOUT2 0-4V voltmeter

4.1.3 Loads

LOAD1
The Output1 Load (LOAD1) should be an Electronic Constant Current Mode Load capable of 0-2Adc at 5.0V

LOAD2
The Output2 Load (LOAD2) should be an Electronic Constant Current Mode Load capable of 0-2Adc at 3.3V

4.1.4 Oscilloscope

OSCILLOSCOPE
A Digital or Analog Oscilloscope can be used to measure the ripple voltage on VOUT1 or VOUT2. The Oscilloscope should be set for 1MΩ impedance, 20MHz Bandwidth, AC coupling, 1μs/division horizontal resolution, 10mV/division vertical resolution for taking output ripple measurements. TP3 and TP4 or TP18 and TP19 can be used to measure the output ripple voltages by placing the oscilloscope probe tip through TP3 or TP18 and holding the ground barrel to TP4 or TP19 as shown in Figure 3. For a hands free approach, the loop in TP4 or TP19 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge

V_{IN} to J1
The connection between the source voltage, VIN and J1 of HPA241 can carry as much as 5 Adc. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J2 to LOAD1

The power connection between J2 of HPA241 and LOAD1 can carry as much as 2Adc. The minimum recommended wire size is AWG #18, with the total length of wire less than 2 feet (1 foot output, 1 foot return).

J3 to LOAD2
The power connection between J3 of HPA241 and LOAD2 can carry as much as 2Adc. The minimum recommended wire size is AWG #18, with the total length of wire less than 2 feet (1 foot output, 1 foot return).

4.1.6 Other

FAN
This evaluation module includes components that can get hot to the touch, because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is recommended to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered. The EVM should not be probed while the fan is not running.

4.2 Equipment Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the TPS55386EVM-363. Note that although the return for J1, J2 and JP3 are the same system ground, the connections should remain separate as shown in Figure 2.

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 5.0A maximum. Make sure V_{IN} is initially set to 0V and connected as shown in Figure 2.
3. Connect the ammeter A1 (0-5A range) between V_{IN} and J1 as shown in Figure 2.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
5. Connect LOAD1 to J2 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0Adc before V_{IN} is applied.
6. Connect voltmeter, V2 across TP3 and TP4 as shown in Figure 2.
7. Connect LOAD2 to J3 as shown in Figure 2. Set LOAD2 to constant current mode to sink 0Adc before V_{IN} is applied.
8. Connect voltmeter, V3 across TP18 and TP19 as shown in Figure 2.
9. Place Fan as shown in Figure 3 and turn on, making sure air is flowing across the EVM.

4.2.2 Diagram

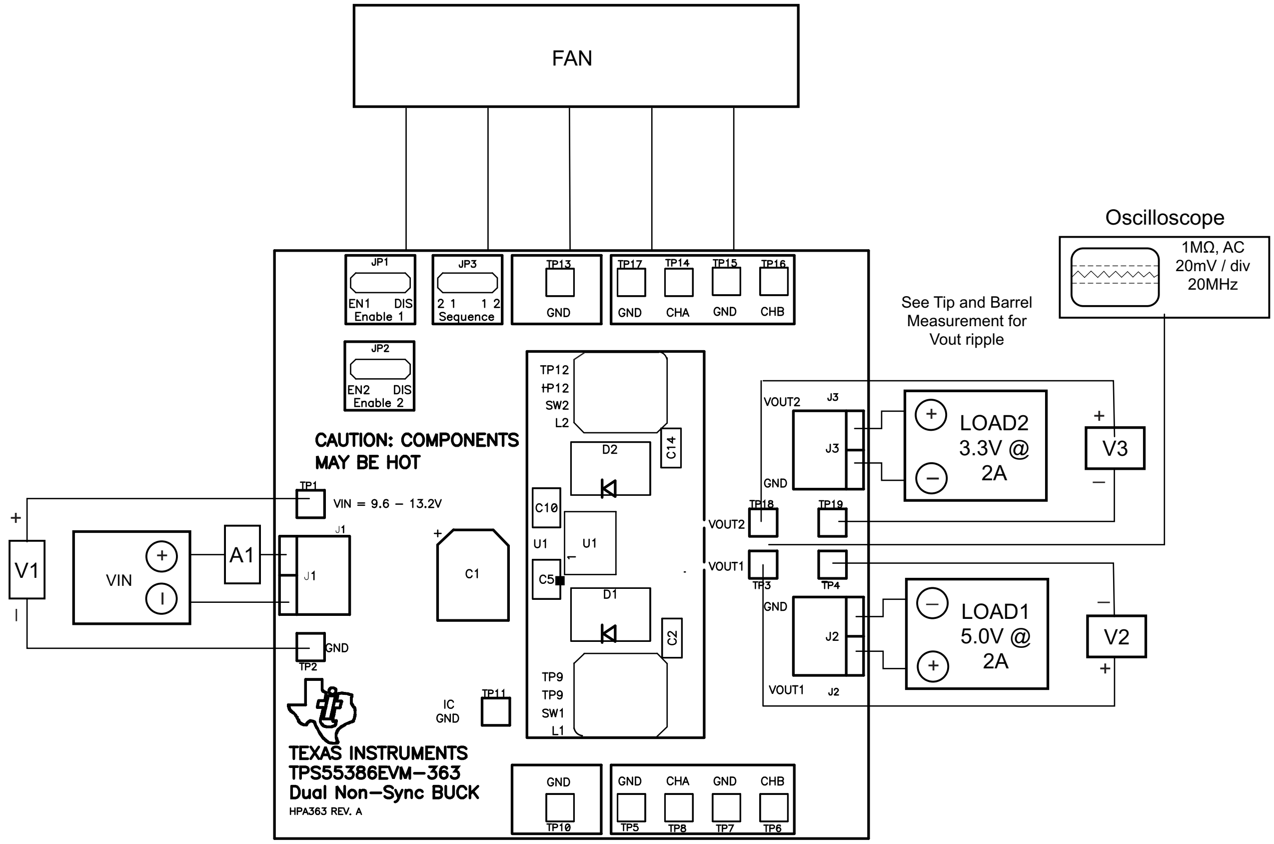


Figure 2. TPS55386EVM-363 Recommended Test Set-Up

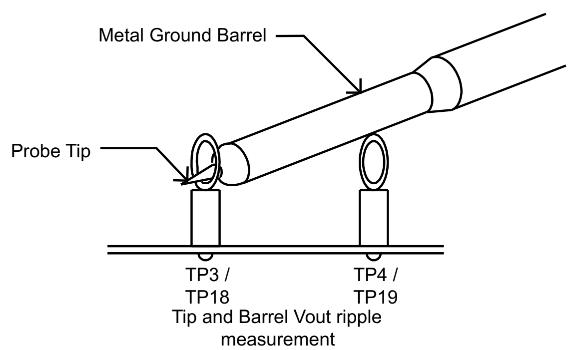


Figure 3. Output Ripple Measurement – Tip and Barrel using TP3 and TP4 or TP18 and TP19

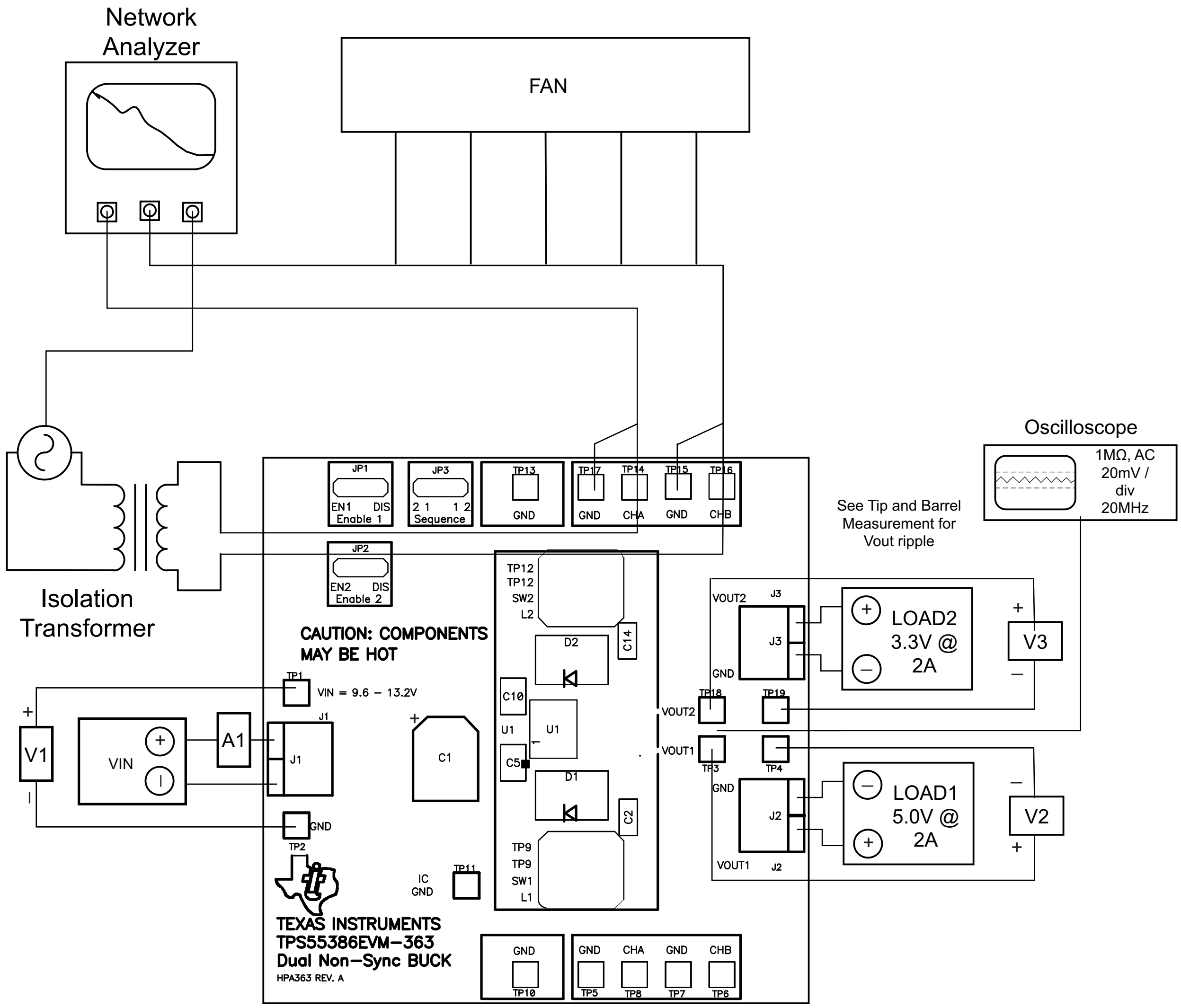


Figure 4. Control Loop Measurement Setup

4.3 Start Up / Shut Down Procedure

1. Increase V_{IN} from 0V to 12Vdc
2. Vary LOAD1 from 0 – 3Adc
3. Vary LOAD2 from 0 – 3Adc
4. Vary V_{IN} from 9.6Vdc to 13.2Vdc
5. Decrease V_{IN} to 0Vdc
6. Decrease LOAD1 to 0A
7. Decrease LOAD2 to 0A

4.4 Output Ripple Voltage Measurement Procedure

See Section 5.4 for more information on measuring output ripple.

1. Increase V_{IN} from 0V to 12Vdc
2. Adjust LOAD1 to desired load between 0Adc and 3Adc
3. Adjust LOAD2 to desired load between 0Adc and 3Adc
4. Adjust V_{IN} to desired load between 9.6Vdc and 13.2Vdc

5. Connect Oscilloscope Probe to TP3 and TP4 or TP18 and TP19 as shown in Figure 3
6. Measure Output Ripple
7. Decrease V_{IN} to 0Vdc
8. Decrease LOAD1 to 0A
9. Decrease LOAD2 to 0A

4.5 Control Loop Gain and Phase Measurement Procedure

1. Connect 1kHz–1MHz Isolation Transformer to TP6 and TP8 as show in Figure 4
2. Connect Input Signal Amplitude Measurement Probe (Channel A) to TP8 as shown in Figure 4
3. Connect Output Signal Amplitude Measurement Probe (Channel B) to TP6 as shown in Figure 4
4. Connect Ground Lead of Channel A and Channel B to TP5 and TP7 as shown in Figure 4
5. Inject 30mV or less signal across R1 through Isolation Transformer
6. Sweep Frequency from 1kHz to 1MHz with 10Hz or lower post filter
7. Control Loop Gain can be measured by $20 \times \mathrm{LOG}\left(\frac{\mathrm{ChannelB}}{\mathrm{ChannelA}}\right)$
8. Control Loop Phase is measured by the Phase difference between Channel A and Channel B
9. Control Loop for Channel 2 can be measured by making the following substitutions
   a. Change TP6 to TP16
   b. Change TP8 to TP14
   c. Change TP5 to TP17
   d. Change TP7 to TP15
10. Disconnect Isolation Transformer before making any other measurements (Signal Injection into Feedback may interfere with accuracy of other measurements)

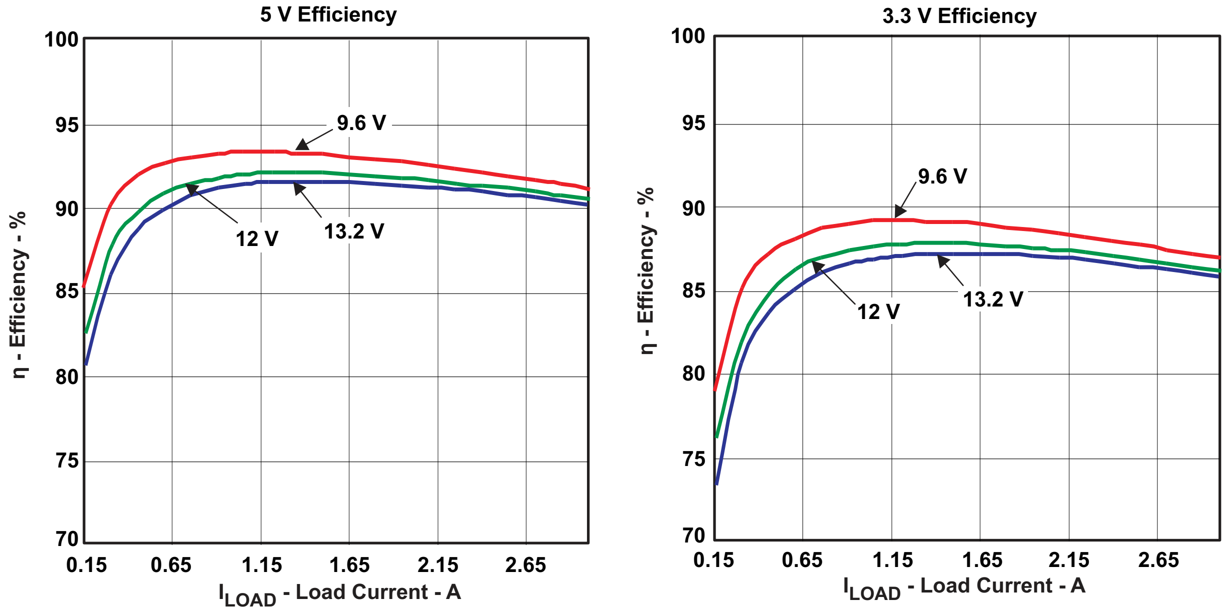
4.6 Equipment Shutdown

1. Shut Down Oscilloscope
2. Shut down V_{IN}
3. Shut down LOAD1
4. Shut down LOAD2
5. Shut down FAN

5 TPS55386EVM-363 Typical Performance Data and Characteristic Curves

Figure 5 through Figure 10 present typical performance curves for the TPS55386EVM-363. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

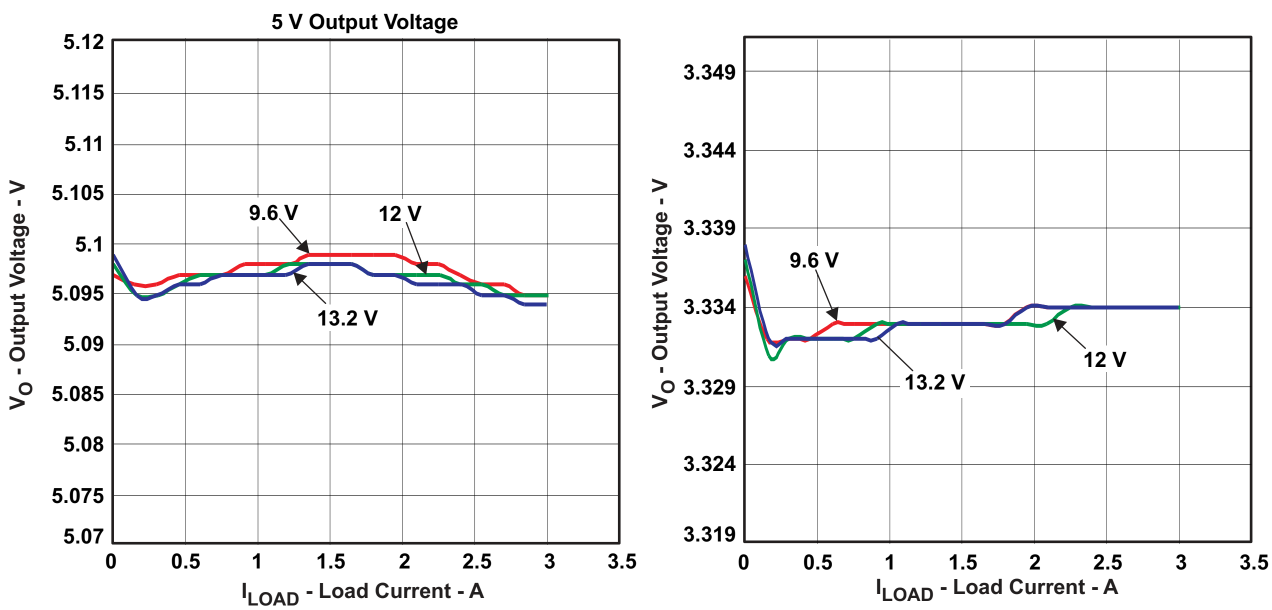
5.1 Efficiency



V_{IN} = 9.6-13.2V, V_{OUT1} = 5.0V I_{OUT1} = 0-3A, V_{OUT2} = 3.3V I_{OUT2} = 0-3A

Figure 5. TPS55386EVM-363 Efficiency vs Load Current

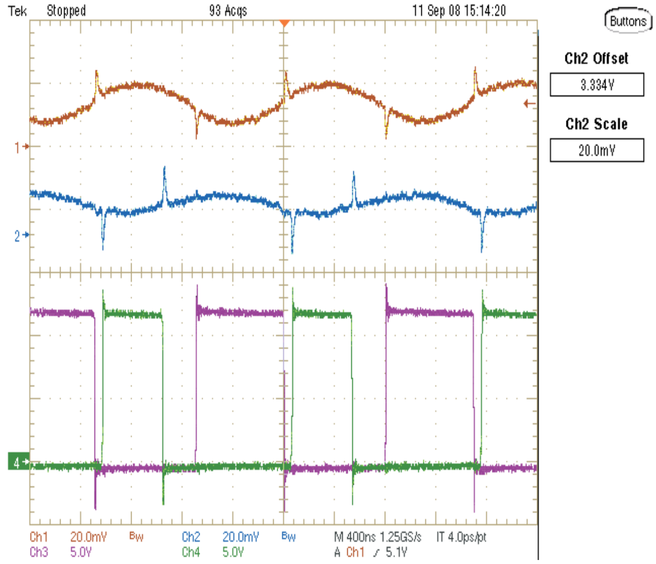
5.2 Line and Load Regulation



V_{IN} = 9.6-13.2V, V_{OUT1} = 5.0V I_{OUT1} = 0-3A, V_{OUT2} = 3.3V I_{OUT2} = 0-3A

Figure 6. TPS55386EVM-363 Output Voltage vs Load Current

5.3 Switch Node and Output Ripple Voltage



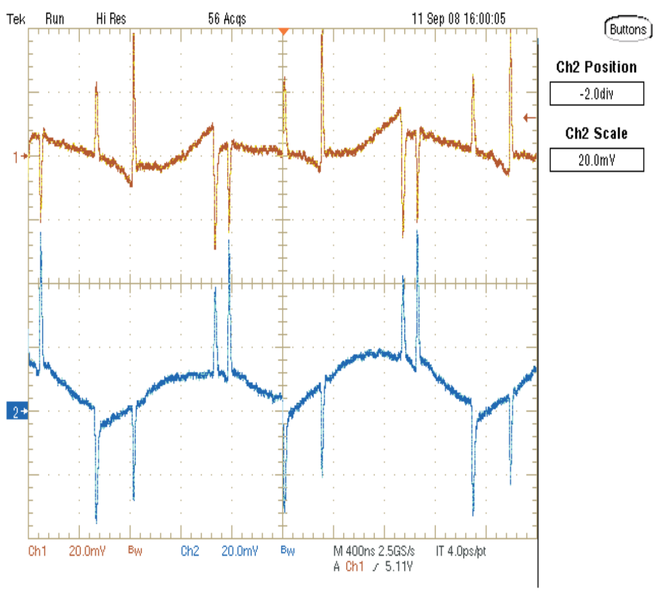
V_{IN} = 13.2V, = 5.0V I_{OUT1} = 3A, V_{OUT2} = 3.3V I_{OUT2} = 3A

Ch1: TP3 (VOUT1), Ch2: TP18 (VOUT2) Ch3: TP9 (SW1), Ch4: TP12 (SW2)

Figure 7. TPS55386EVM-363 Output Voltage Ripple

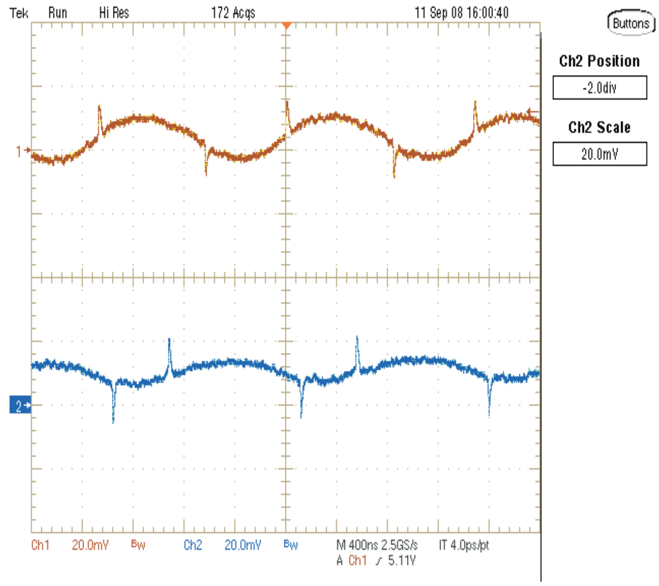
5.4 Output Ripple Voltage

The output ripple voltage measured at the output test points (TP3 and TP4 or TP18 and TP19) will include some high-frequency switch edge noise and offsets due to the ground loop area in this measurement. See Figure 8. A more accurate measurement of the output ripple can be taken by soldering a bare wire directly to the output capacitor (C5 or C17) and connecting this wire directly to the ground barrel of the oscilloscope probe. This produces truer oscillograms of the output ripple. See Figure 9.



CH1: V_{OUT1} CH2: V_{OUT2}

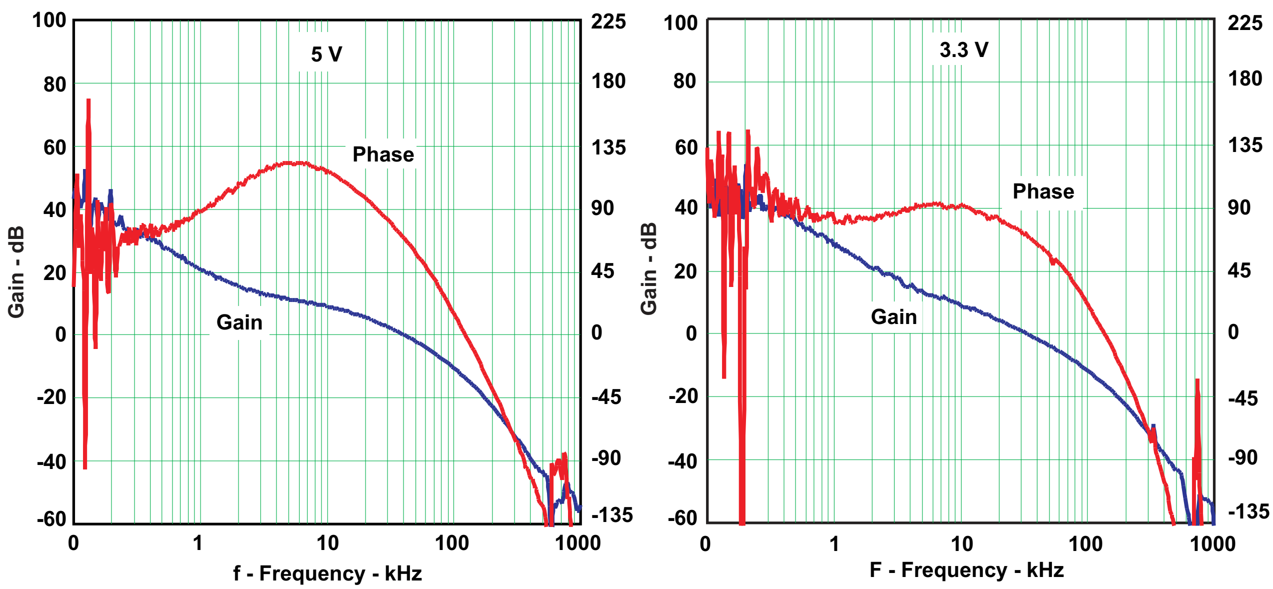
Figure 8. Output Ripple Voltage Measured at Test Points



CH1: V_{OUT1} CH2: V_{OUT2}

Figure 9. Output Ripple Voltage Measured at Test Points

5.5 CONTROL LOOP BODE PLOT



V_{IN} = 12V, V_{OUT1} = 5.0V, V_{OUT2} = 3.3V, I_{OUT1} = I_{OUT2} = 3A

V_{OUT1}: Bandwidth: 40 kHz Phase Margin: 69°

V_{OUT2}: Bandwidth: 33 kHz Phase Margin: 71°

Figure 10. TPS55386EVM-363 Gain and Phase vs Frequency

6 EVM Assembly Drawings and Layout

Figure 11 through Figure 16 show the designs of the TPS55386EVM-363 printed circuit board. The EVM has been designed using a 4-Layer, 2oz copper-clad circuit board 3.0” × 3.0” with all components in a 1.15” × 2.15” active area on the top side and all active traces to the top and bottom layers to allow the user to easily view, probe and evaluate the TPS55386 control IC in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems

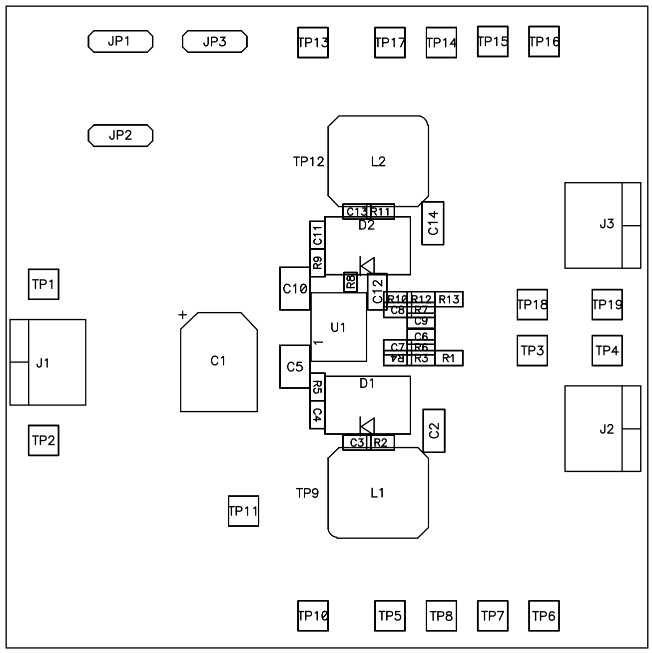


Figure 11. TPS55386EVM-363 Component Placement (Viewed from Top)

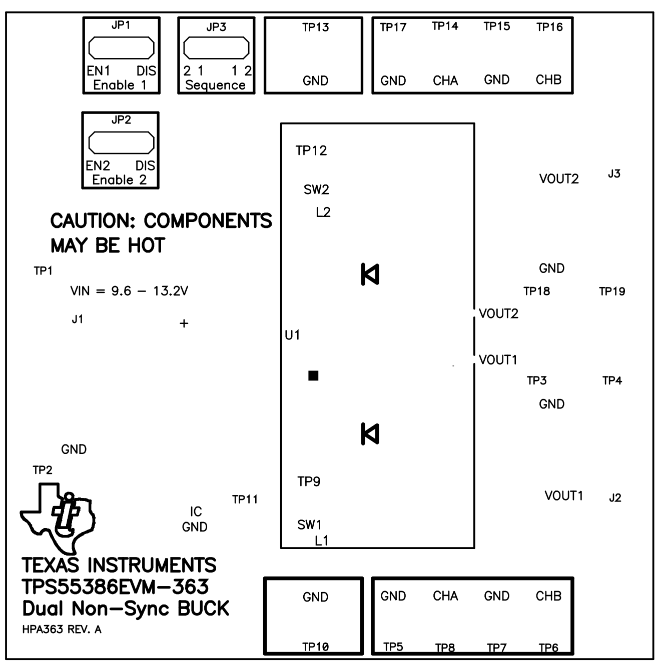


Figure 12. TPS55386EVM-363 Silkscreen (Viewed from Top)

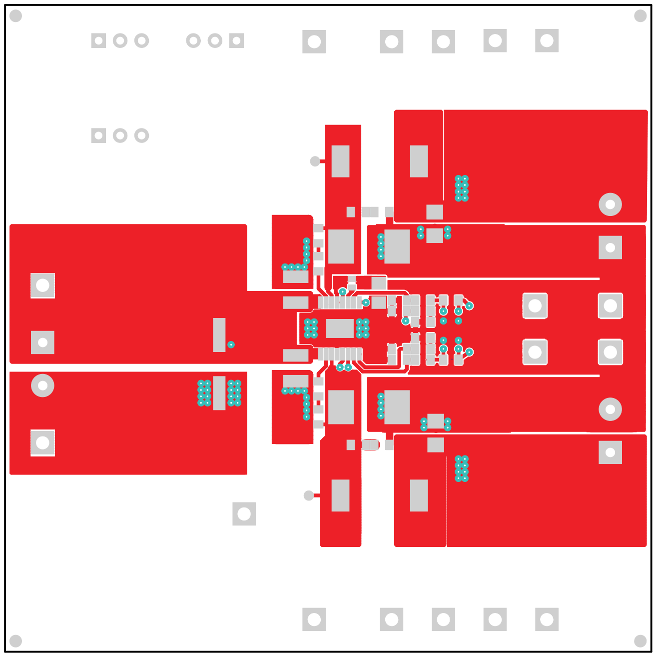


Figure 13. TPS55386EVM-363 Top Copper (Viewed from Top)

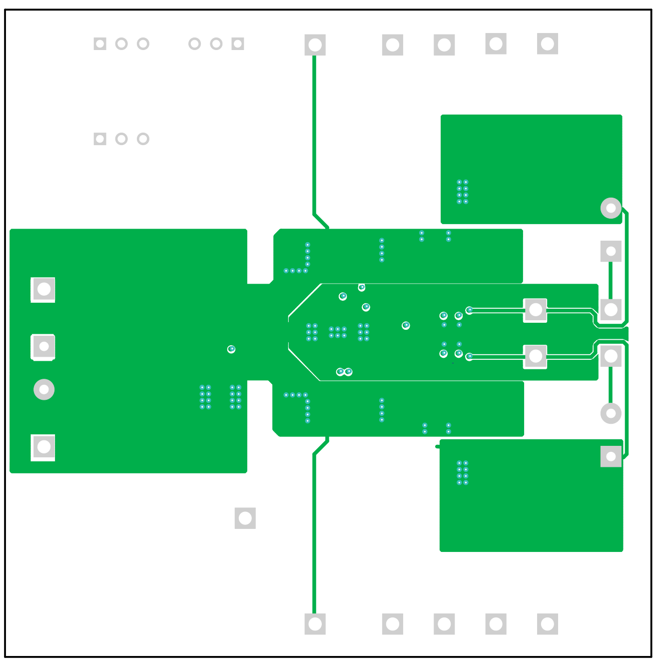


Figure 14. TPS55386EVM-363 Bottom Copper (X-Ray View from Top)

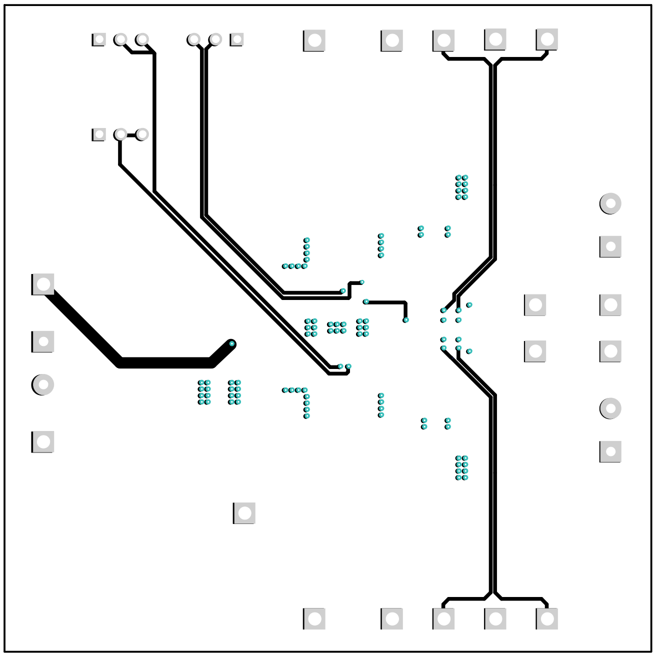


Figure 15. TPS55386EVM-363 Internal 1 (X-Ray View from Top)

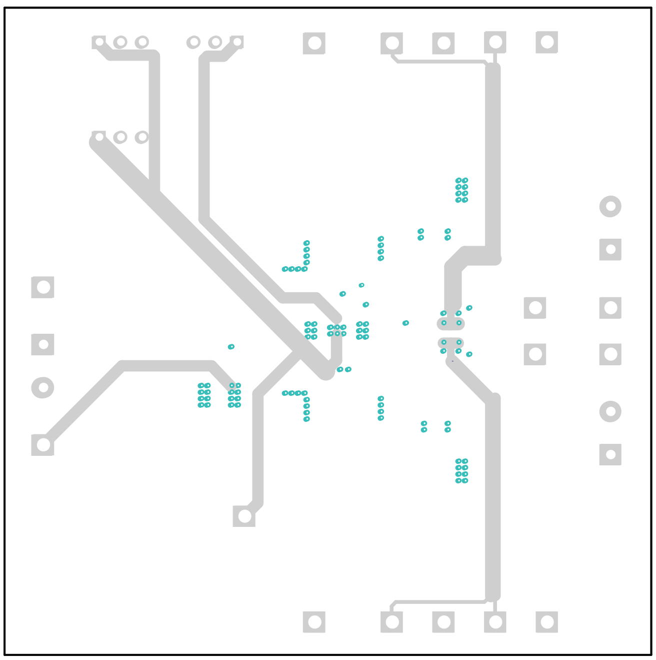


Figure 16. TPS55386EVM-363 Internal 2 (X-Ray View from Top)

7 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 3. TPS55386EVM-363 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C1	100 µF	Capacitor, Aluminum, 25V, 20%	0.328 x 0.390 inch	EEEFC1E101P	Panasonic
1	C12	4.7 µF	Capacitor, Ceramic, 10V, X5R, 20%	0805	Std	Std
2	C2, C14	22 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	C3216X5R0J226M	TDK
2	C3, C13	470 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	C4, C11	.047 µF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	C5, C10	10 µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	C3225X5R1E106M	TDK
2	C6, C9	2.2 nF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C7	47 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C8	100 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	D1, D2	MBRS330T3	Diode, Schottky, 3-A, 30-V	SMC	MBRS330T3	On Semi
3	J1, J2, J3	ED1609-ND	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED1609	OST
3	JP1, JP2, JP3	PTC36SAAN	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 inch x 3	PTC36SAAN	Sullins
2	L1, L2	8.2 µH	Inductor, SMT, 4.38A, 20 mΩ	0.402 x 0.394 inch	MSS1048-822L	Coilcraft
2	R1, R13	51 Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R10	6.49 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R11	10 Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
2	R3, R12	20.5 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	3.83 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R5, R9	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R6	13.7 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	8.87 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	0	Resistor, Chip, 1/16W, 5%	0402	Std	Std
3	TP1, TP3, TP18 TP2, TP4, TP5, TP7, TP10, TP13	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
9	TP15, TP17, TP19 TP6, TP8, TP11	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
5	TP14, TP16	5012	Test Point, White, Thru Hole	0.125 x 0.125 inch	5012	Keystone
2	TP9, TP12	None	Test point, 40 mil SMT	None	None	None
1	U1**	TPS55386PWP	IC, Dual 600kHz Non-Sync BUCK with Interal FET	HTSSOP-16	TPS55386PWP	TI
3	--		Shunt, 100-mil, Black	0.100	929950-00	3M

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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