TSH343

280MHz single-supply triple video buffer

Features

- Bandwidth: 280MHz
- 5V single-supply operation
- Internal input DC level shifter
- No input capacitor required
- 6dB internal gain for a matching between 3 channels
- Very low harmonic distortion
- Slew rate: 780V/µs
- Specified for 150Ω and 100Ω loads
- Min. and max. data tested during production

Applications

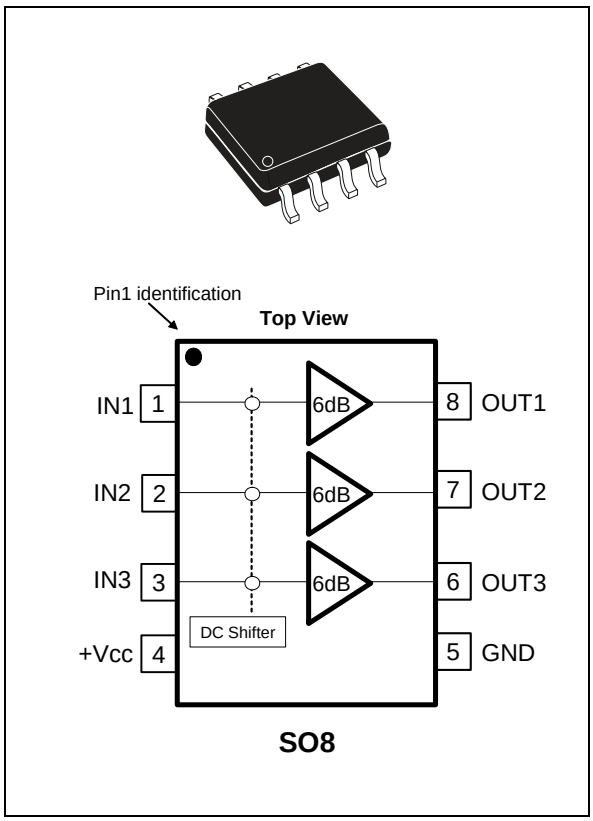
- High-end video systems
- High definition TV (HDTV)
- Broadcast and graphic video
- Multimedia products

Description

The TSH343 is a triple single-supply video buffer featuring an internal gain of 6dB and a large 280MHz bandwidth.

The main advantage of this circuit is that its input DC level shifter allows for video signals on 75Ω video lines without damage to the synchronization tip of the video signal, while using a single 5V power supply with no input capacitor. The DC level shifter is internally fixed and optimized to keep the output video signals between low and high output rails in the best position for the greatest linearity.

This datasheet provides information on using the TSH343 as a Y-Pb-Pr driver for video DAC output on a video line. See the TSH344 datasheet for R-G-B signals.



SO8

The TSH343 is available in the compact SO8 plastic package for optimum space-saving.

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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{in}	Input voltage range (2)	0 to +1.4	V
T_{oper}	Operating free air temperature range	-40 to +85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thjc}	SO8 thermal resistance junction to case	28	°C/W
R_{thja}	SO8 thermal resistance junction to ambient area	157	°C/W
P_{max}	Maximum power dissipation (@T_{amb}=25°C) for T_j=150°C	800	mW
ESD	CDM: charged device model HBM: human body model MM: machine model	2 1.5 200	kV kV V

1. All voltage values, except differential voltage, are with respect to network terminal.
2. The magnitude of input and output voltages must never exceed V_{CC} +0.3V.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	3 to 5.5(1)	V

1. Tested in full production at 0V/5V single power supply.

2 Electrical characteristics

Table 3. V_{CC} = +5V single supply, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{DC}	Input DC shift (see *Figure 16* for the behaviour in temperature)	R_L = 150Ω, T_{amb}	400	600	670	mV
		-40°C < T_{amb} < +85°C		530		
I_{ib}	Input bias current	T_{amb} , input to GND		18.2	35	µA
		-40°C < T_{amb} < +85°C		20.7		
R_{in}	Input resistance	T_{amb}		4		GΩ
C_{in}	Input capacitance	T_{amb}		1		pF
I_{CC}	Supply current per buffer	no load, input to GND		14.4	18	mA
		-40°C < T_{amb} < +85°C		14.9		
PSRR	Power supply rejection ratio(1) 20 log ($\Delta V_{out}/\Delta V_{CC}$)	F = 1MHz		-45		dB
G	DC voltage gain	R_L = 150Ω, V_{in} = 1V	1.92	1.99	2.05	V/V
DG	Variation of the DC voltage gain between inputs of 0.3V and 1V	Input step from 0.3V to 1V		0.26	0.8	%
MG_1	Gain matching between 3 channels	Input = 1V		0.5	2	%
$MG_{0.3}$	Gain matching between 3 channels	Input = 0.3V		0.5	2	%
Dynamic performance and output characteristics						
Bw	-3dB bandwidth	Small signal V_{out} = 20mVp R_L = 150Ω	160	280		MHz
	Gain flatness @ 0.1dB	Small signal V_{out} = 20mVp R_L = 150Ω		65		
FPBW	Full power bandwidth	V_{out} = $2V_{p-p}$, V_{ICM} = 0.5V, R_L = 150Ω	130	200		MHz
D	Delay between each channel(2)	0 to 30MHz		0.5		ns
SR	Slew rate (3)	Input step from 0V to 1V, R_L = 150Ω	500	780		V/µs
V_{OH}	High level output voltage	$V_{in\ DC}$ = +1.5V, R_L = 150Ω	3.7	3.9		V
V_{OL}	Low level output voltage	R_L = 150Ω		40		mV
I_{OUT}	Output current	V_{out} = 2V, T_{amb}	45	90		mA
		-40°C < T_{amb} < +85°C		82		
	Output short-circuit current (I_{source})			100		mA

Table 3. V_{CC} = +5V single supply, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Noise and distortion						
eN	Total input voltage noise	F = 100kHz, R_{IN} = 50Ω		29		nV/√Hz
		10kHz to 30MHz 10kHz to 100MHz		158 290		µVrms
HD2	2nd harmonic distortion	V_{out} = 2V_{p-p}, R_L = 150Ω F= 10MHz F= 30MHz		 -58 -45		dBc
HD3	3rd harmonic distortion	V_{out} = 2Vp-p, R_L = 150Ω F= 10MHz F= 30MHz		 -72 -50		dBc

1. See *Figure 28* and *Figure 29*.
2. See *Figure 30* and *Figure 31*.
3. Non-tested value, guaranteed by design.

Figure 1. Frequency response

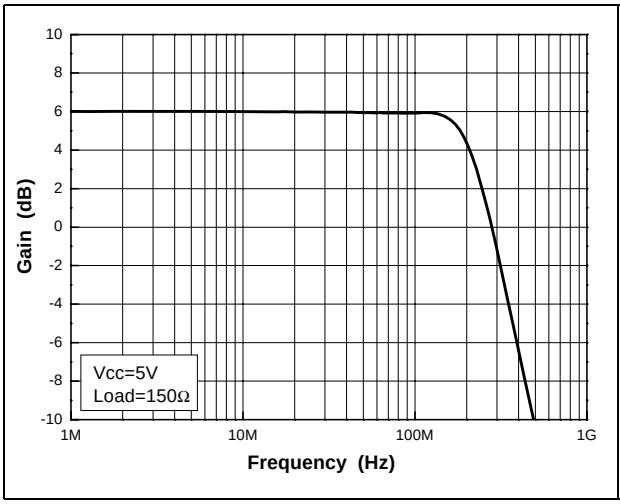


Figure 2. Gain flatness

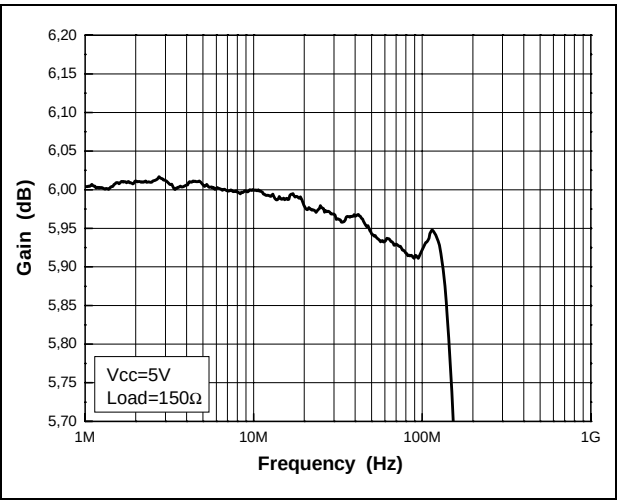


Figure 3. Cross-talk vs. frequency (amp1)

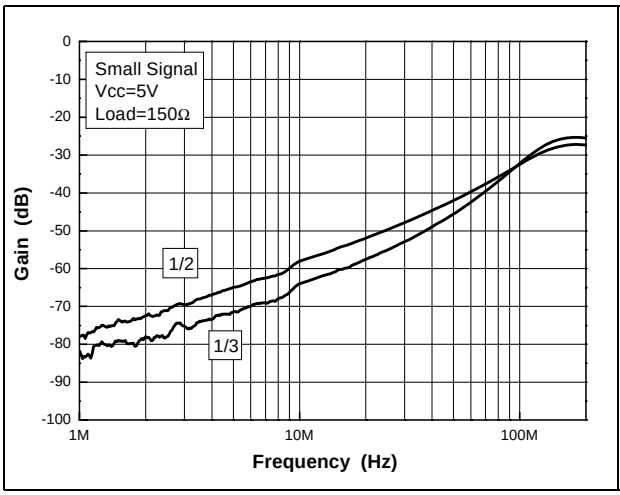


Figure 4. Cross-talk vs. frequency (amp2)

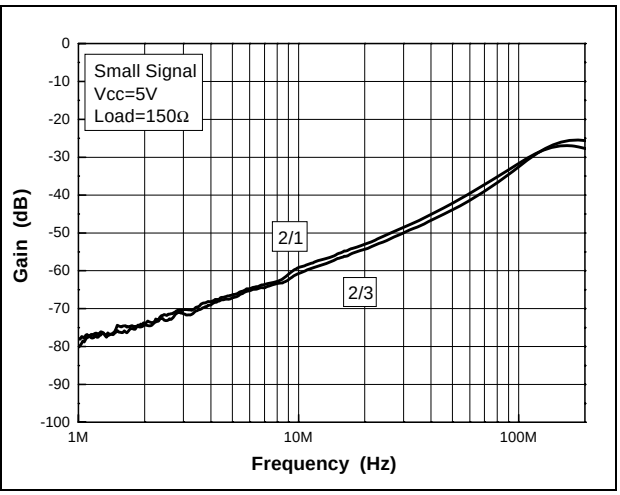


Figure 5. Cross-talk vs. frequency (amp3)

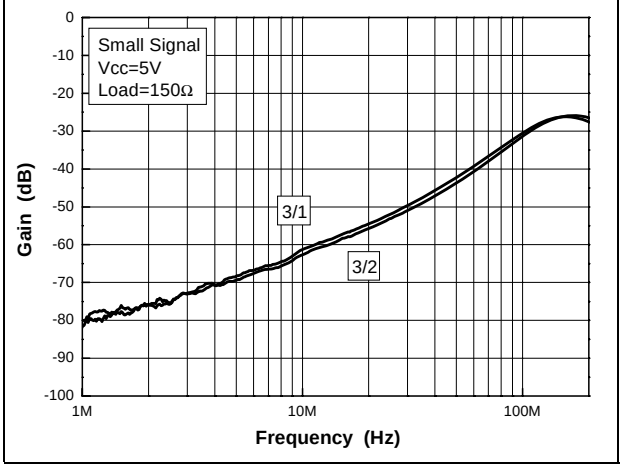


Figure 6. Input noise vs. frequency

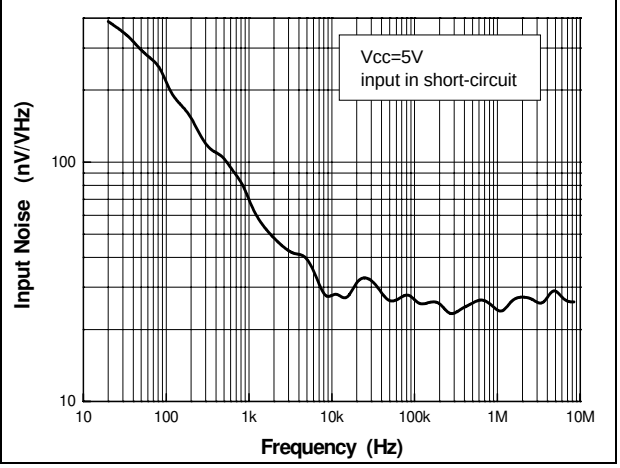


Figure 7. Distortion on 150Ω load - 10MHz

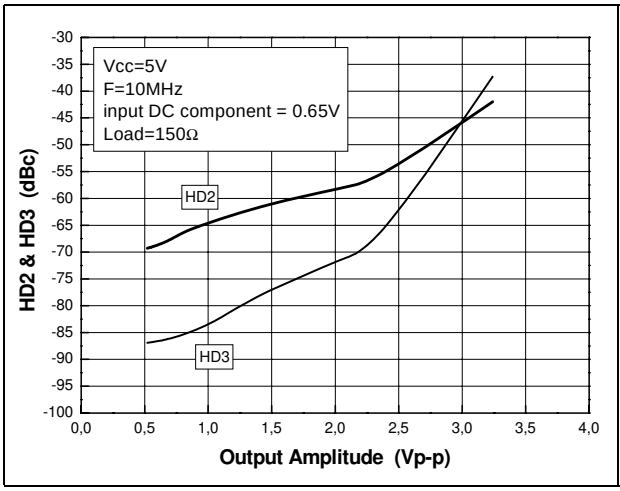


Figure 8. Distortion on 100Ω load - 10MHz

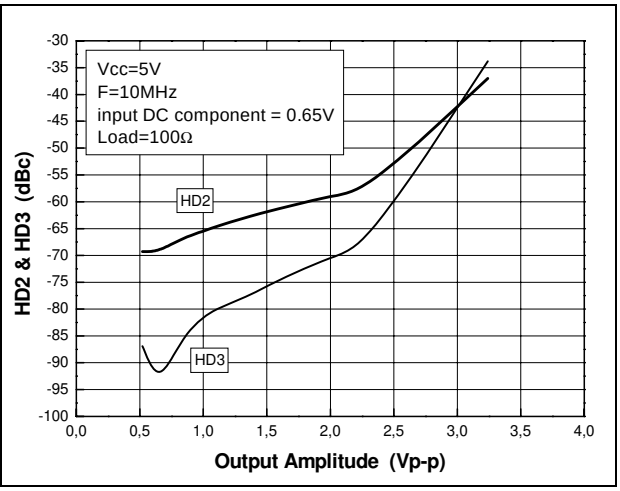


Figure 9. Distortion on 150Ω load - 30MHz

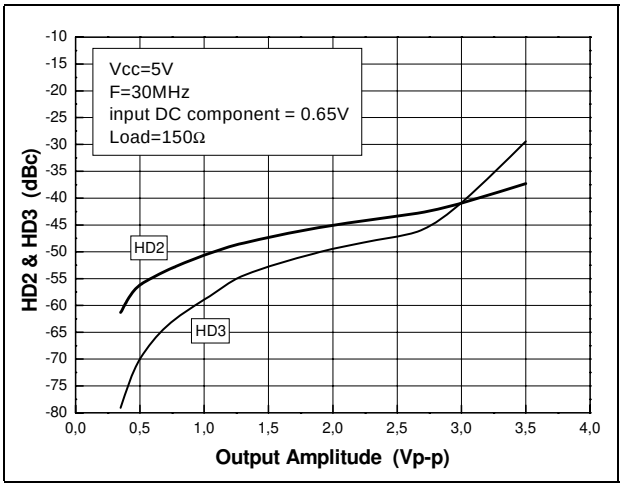


Figure 10. Distortion on 100Ω load - 30MHz

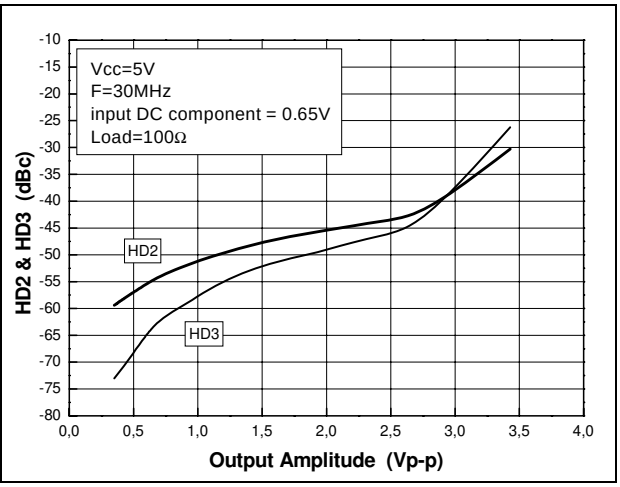


Figure 11. Output DC shift vs. frequency

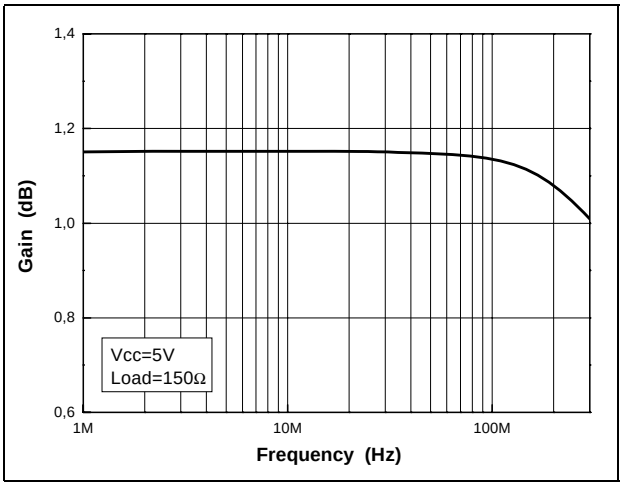


Figure 12. Slew rate

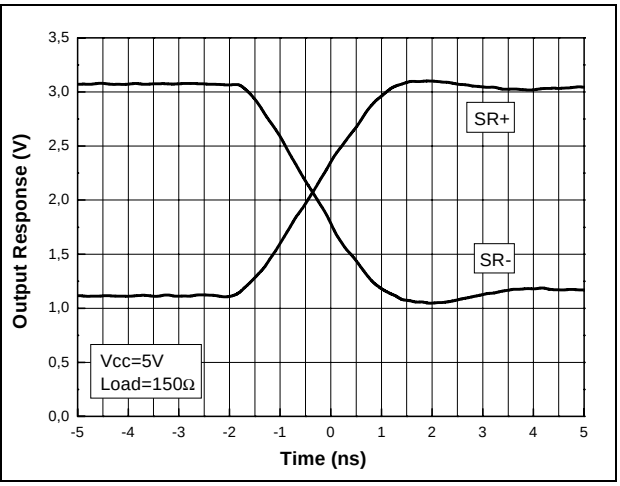


Figure 13. Reverse isolation vs. frequency

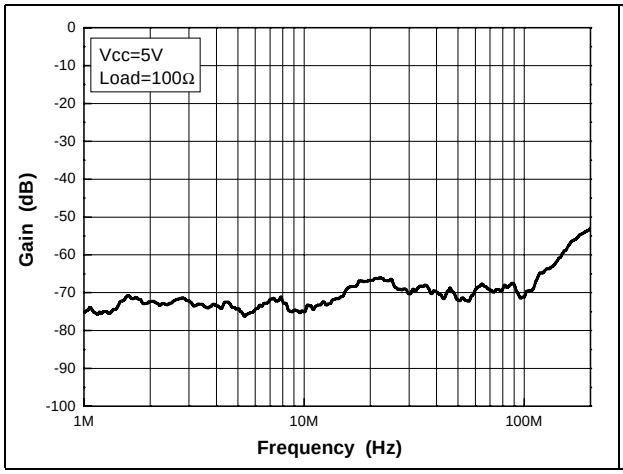


Figure 14. Bandwidth vs. temperature

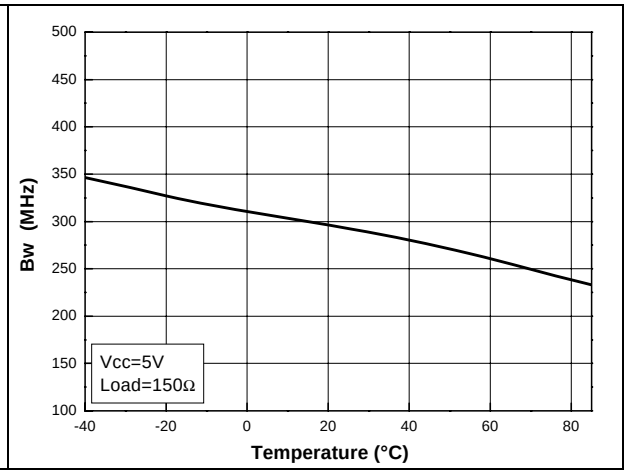


Figure 15. Quiescent current vs. supply

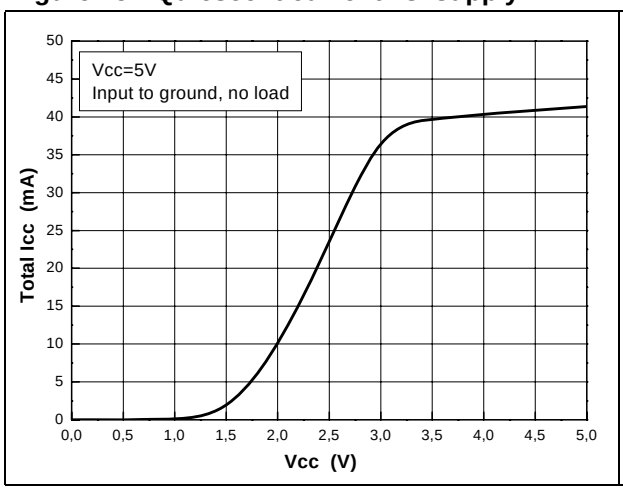


Figure 16. Input DC shift vs. temperature

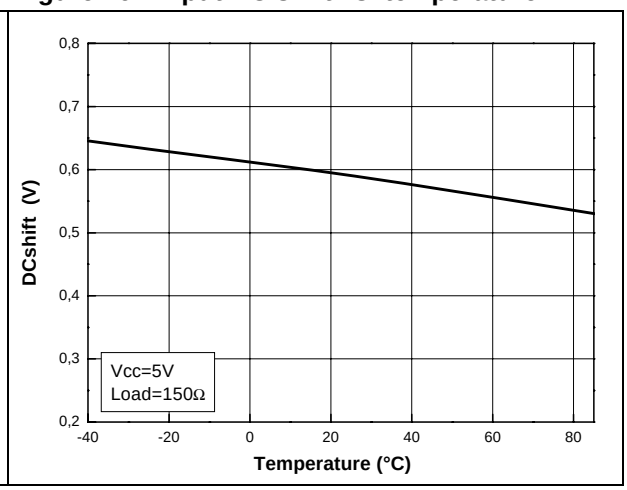


Figure 17. I_{source} vs. output voltage

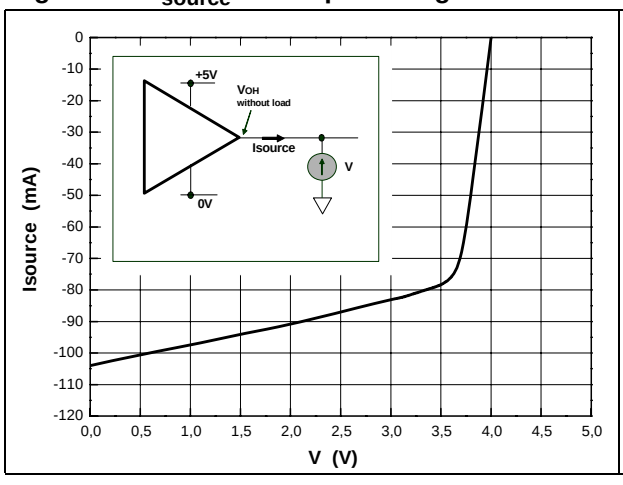


Figure 18. Voltage gain vs. temperature

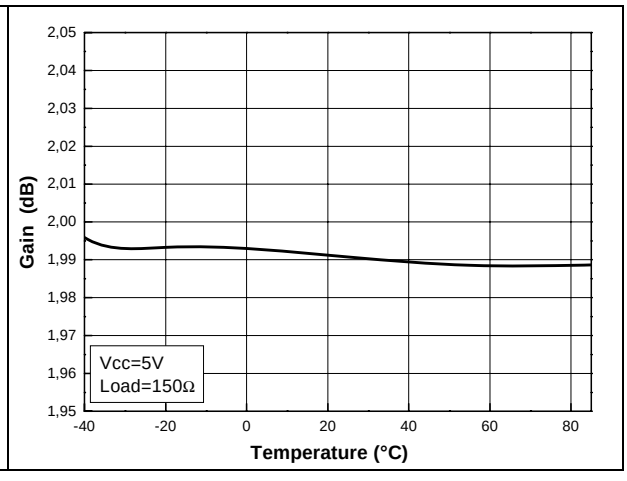


Figure 19. I_{bias} vs. temperature

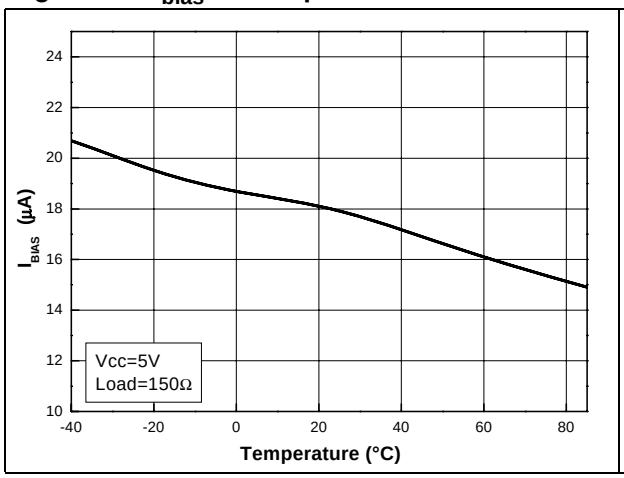


Figure 20. Gain deviation vs. temperature

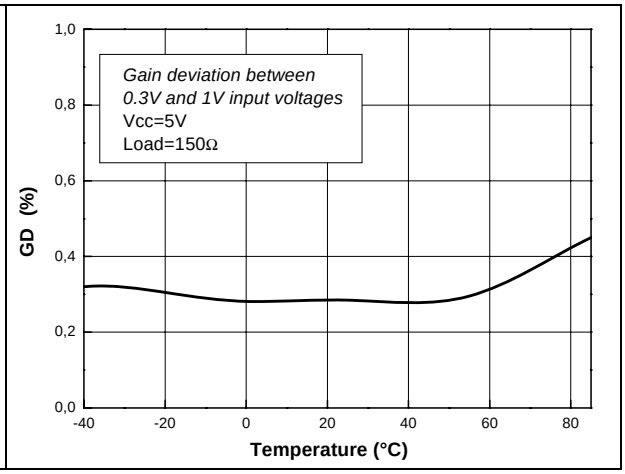


Figure 21. Supply current vs. temperature

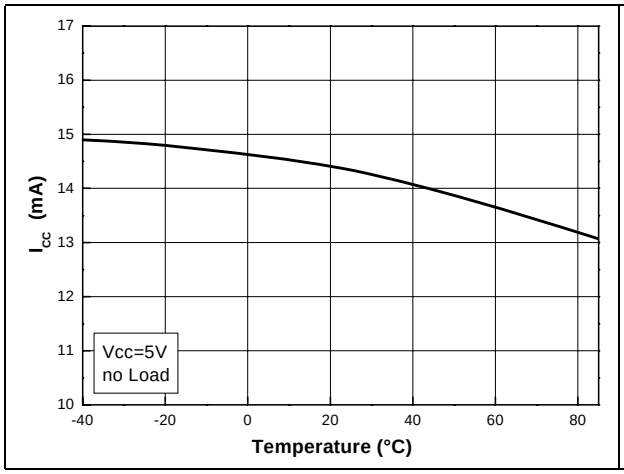


Figure 22. Output current vs. temperature

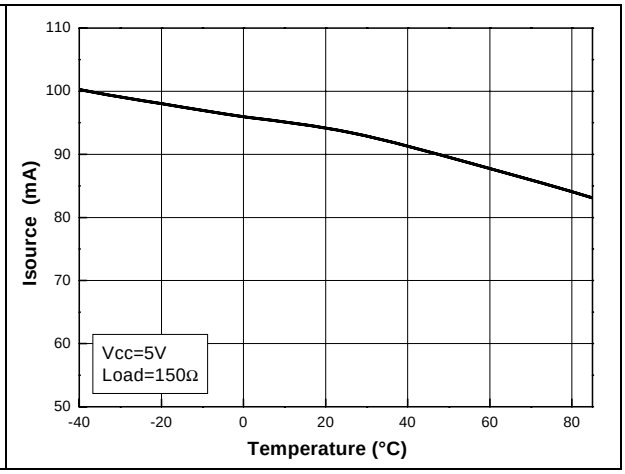


Figure 23. Output higher rail vs. temperature

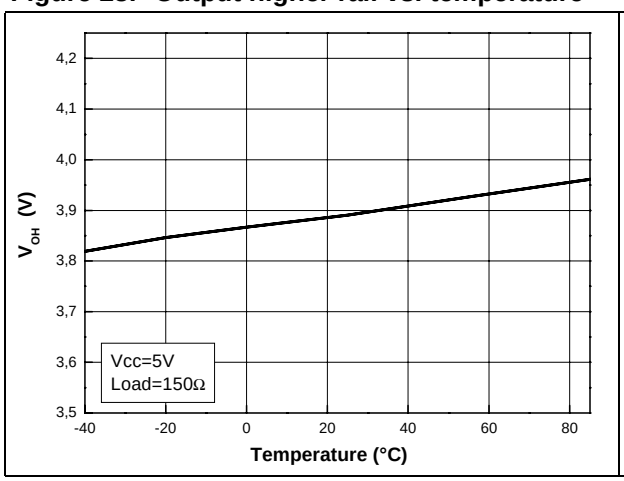
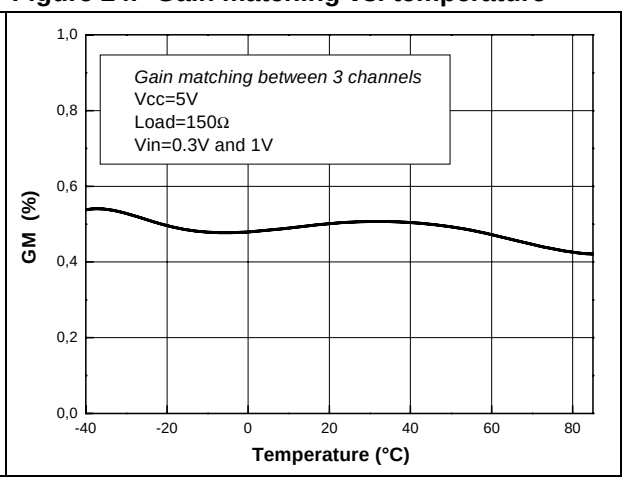


Figure 24. Gain matching vs. temperature



3 Application information

3.1 Using the TSH343 to drive Y-Pb-Pr video components

Figure 25. Shapes of video signals coming from DACs

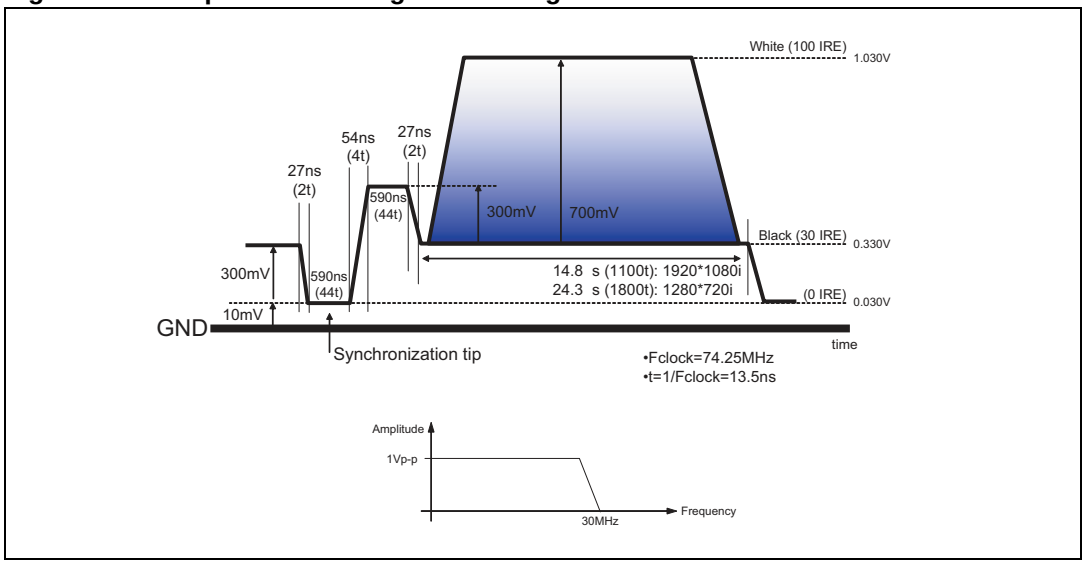
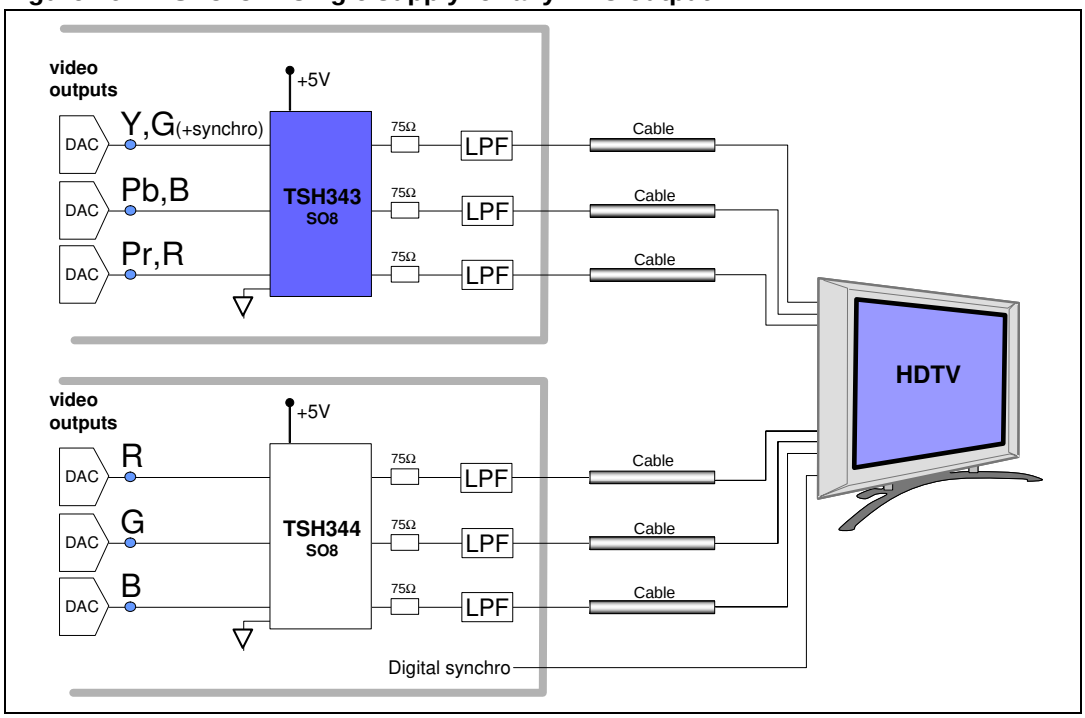
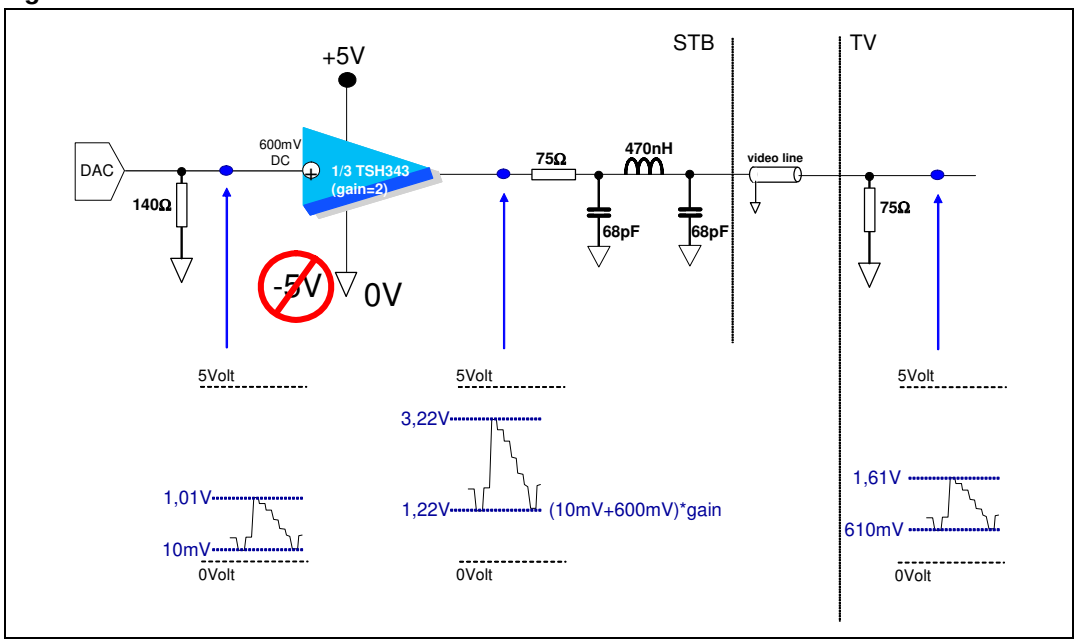


Figure 26. TSH343 in single supply for any DAC output



1. See the TSH344 datasheet on st.com for more information. It is possible to drive RGB signals with the TSH344.

Figure 27. Detailed view of one TSH343 channel



Because of the shape of the signal shown in *Figure 25*, we use a very low output rail triple high-speed buffer. The TSH343 supplied in 5V single power supply, features a low output rail of 40mV on 150-ohm load. The TSH343 is used to drive high definition video signals up to 30MHz on 75-ohm video lines. It is dedicated to driving YPbPr signals where the synchronization tip—close to zero volt—is included in the Y signal.

Figure 27 shows a solution used on the STMicroelectronics reference design of STi7100 or STi7200 where the DAC output is loaded by 140Ω and the bottom of the synchronization tip is set at 10mV. Using the TSH343, an internal input DC value of 600mV is added to the video signal in order to shift the bottom from 10mV to 610mV. The shift is not based on the average of the signal, but is an analog summation of a DC component to the video signal. Therefore, no input capacitors are required which provides a real advantage in terms of cost and board space.

The internal gain of 2 obtained makes it possible to remove two resistors on the BOM. To avoid any perturbation on matching from the DACs output impedance along a large band of 30MHz in HD, a discrete reconstruction filtering is implemented after the driver. This filter is matched on 75-ohms. Note that the TSH343 cannot be AC output coupled (it cannot sink an output current, therefore it is not possible to implement an output series capacitor).

3.2 PSRR and improvement of power supply noise rejection

Figure 28. Circuit for power supply bypassing

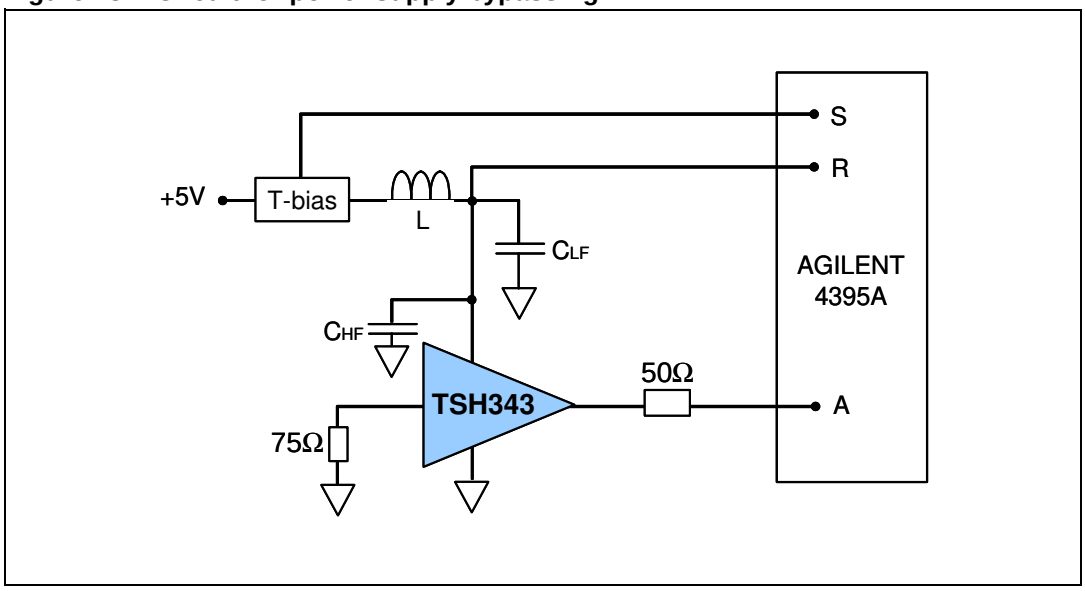
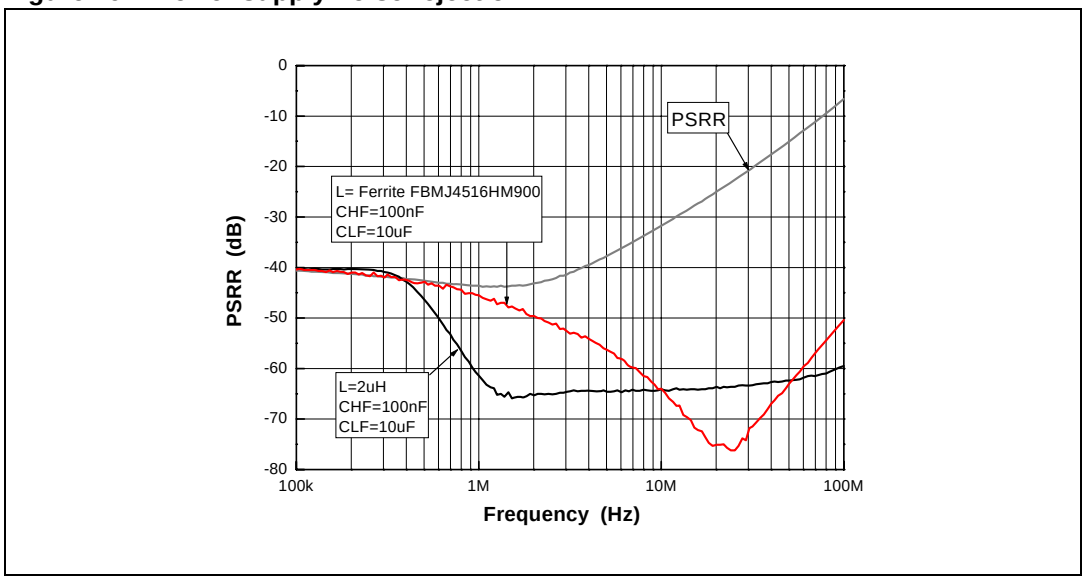


Figure 29 shows how the power supply noise rejection evolves versus frequency depending on how carefully the power supply decoupling is achieved.

Figure 29. Power supply noise rejection

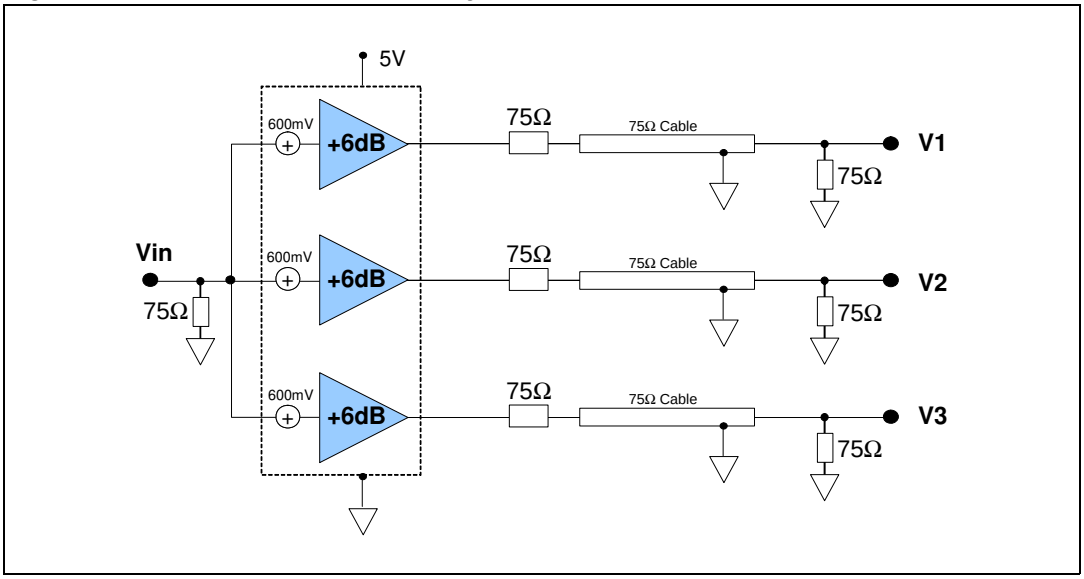


Criteria for choosing the ferrite:

- In DC, the resistance (R) of the ferrite must be as low as possible to keep +5V power supply on the chip.
- In AC, along a 30MHz bandwidth (HD spectrum), the equivalent impedance (Z=R+jX) must be as high as possible to optimize rejection of the noise generated by the power supply.

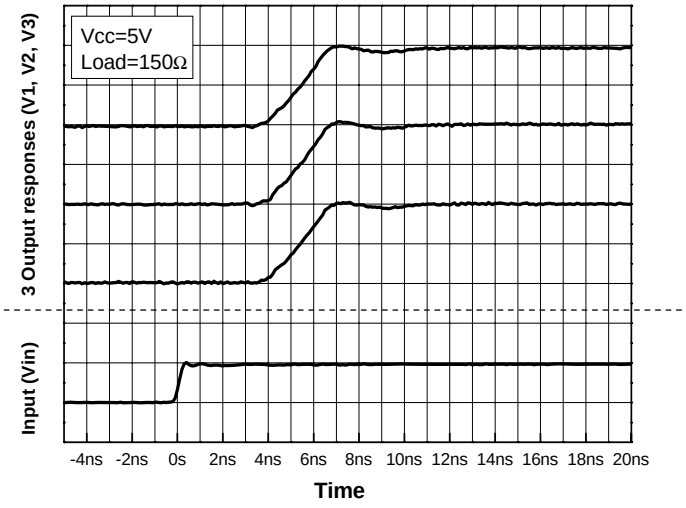
3.3 Delay between channels

Figure 30. Measurement of the delay between each channel



The delay between each video component is an important aspect in high definition video systems. To properly drive the three video components without any relative delay, the TSH343 dice layout has a very symmetrical geometry. The effect is direct on the synchronization of each channel, as shown in *Figure 31*. There is no delay between channels when the same V_{in} signal is applied on the three inputs. Note that the delay between the inputs and the outputs is 4ns.

Figure 31. Relative delay between each channel

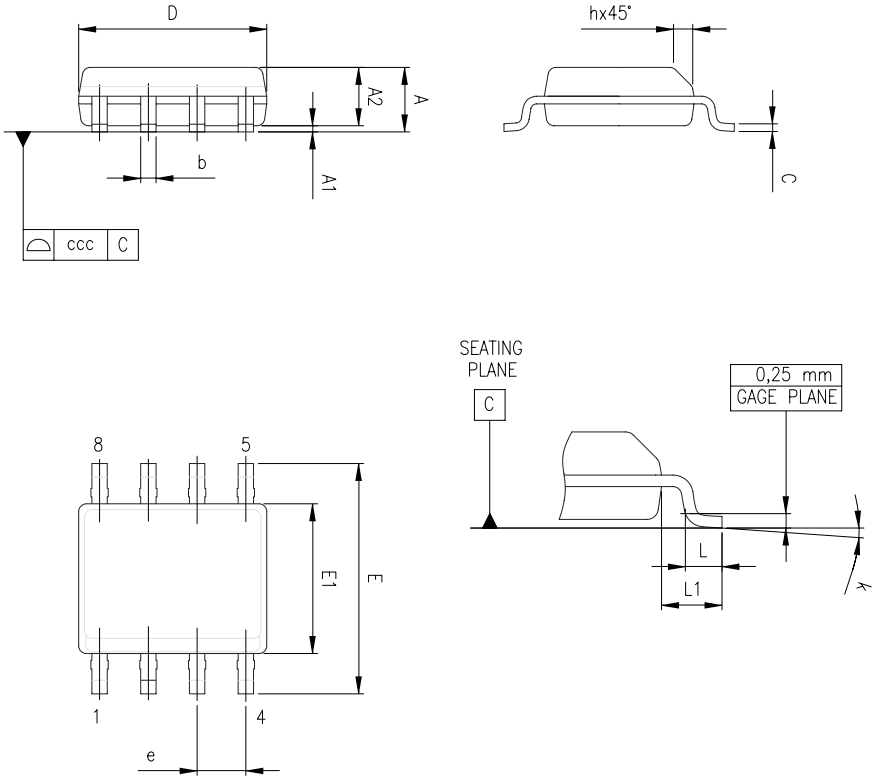


4 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 32. SO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004



5 Ordering information

Table 4. Order codes

Part number	Temperature range	Package	Packing	Marking
TSH343ID	-40°C to +85°C	SO-8	Tube	TSH343I
TSH343IDT			Tape & reel	TSH343I

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
1-Dec-2005	1	First release of datasheet.
2-Jan-2006	2	Capa-load option paragraph deleted on page 11.
10-Jul-2006	3	Application information.
7-Mar-2007	4	Max limit for input DC shift reduced from 800mV to 670mV. Updated *Section 3.2: PSRR and improvement of power supply noise rejection on page 12*.

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