

IGBT

TRENCHSTOP™ IGBT3 Chip SIGC10T60E

**Data Sheet** 

Industrial Power Control



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### TRENCHSTOP<sup>™</sup> IGBT3 Chip

#### Features:

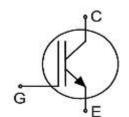
- 600V trench & field stop technology
- Low V<sub>CEsat</sub>
- Low turn-off losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling

#### Recommended for:

- Power modules
- Discrete components

### **Applications:**

- Drives
- White goods
- Resonant applications



Chip Type	V <sub>CE</sub>	<b>I</b> Cn	Die Size	Package
SIGC10T60E	600V	20A	3.19mm x 3.21mm	Sawn on foil

Die size		3.19 x 3.21		
Emitter pad size		See chip drawing	2	
Gate pad size		0.36 x 0.51	mm <sup>2</sup>	
Area total		10.24		
Silicon thickness		70	μm	
Wafer size		200	mm	
Maximum possible ch	ips per wafer	2693		
Passivation frontside		Photoimide		
Pad metal		3200nm AlSiCu		
Backside metal		Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process		
Die bond Electrically conductive epoxy glue and sof			older	
Wire bond		AI, ≤500μm		
Reject ink dot size		Ø 0.65mm; max. 1.2mm		
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C –	-25°C	
(<6 months)	for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Enviro	nment.	



#### **Maximum Ratings**

In general, from reliability and lifetime point of view, the lower the operation junction temperature and/or the applied voltage, the greater the expected lifetime of any semiconductor device.

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}$ =25°C	$V_{CE}$	600	V
DC collector current, limited by $T_{\rm vj\;max}^{\;\;\;1}$	I <sub>C</sub>	-	Α
Pulsed collector current, $t_p$ limited by $T_{vj max}^2$	I <sub>C,puls</sub>	60	Α
Gate-emitter voltage	$V_{GE}$	±20	٧
Virtual junction temperature	$T_{\rm vj}$	-40 +175	°C
Short circuit data $^{1/2/3}$ $V_{GE}=15V$ , $V_{CC}=360V$ , $T_{vj}=150$ °C	t <sub>sc</sub>	6	μs
Reverse bias safe operating area (RBSOA) <sup>2</sup>	$I_{C,max} = 40A, \ V_{CEmax} = 600V, \ T_{vj} \le 150^{\circ}C$		

### Static Characteristics (tested on wafer), T<sub>vi</sub>=25°C

Parameter	Cymbol	Conditions	Value			Unit
Parameter	Symbol Conditions		min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{\text{GE}}=0\text{V}, I_{\text{C}}=2\text{mA}$	600	-	-	
Collector-emitter saturation voltage	V <sub>CEsat</sub>	V <sub>GE</sub> =15V, I <sub>C</sub> =20A	1.1	1.5	1.9	V
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_{\rm C} = 290 \mu {\rm A}, \ V_{\rm GE} = V_{\rm CE}$	5.0	5.8	6.5	
Zero gate voltage collector current	I <sub>CES</sub>	$V_{CE} = 600 \text{V}, \ V_{GE} = 0 \text{V}$	-	-	1.1	μΑ
Gate-emitter leakage current	I <sub>GES</sub>	$V_{CE} = 0V, V_{GE} = 20V$	-	-	300	nA
Integrated gate resistor	r <sub>G</sub>			none		Ω

### **Electrical Characteristics 2**

Parameter	Symbol	Conditions		Value		Unit
Parameter	Syllibol	Conditions	min.	typ.	max.	Ullit
Input capacitance	C <sub>ies</sub>	V <sub>CE</sub> =25V, V <sub>GE</sub> =0V, f=1MHz	-	1100	1	
Output capacitance	$C_{oes}$		-	71	-	pF
Reverse transfer capacitance	$C_{res}$	<i>T</i> <sub>vj</sub> =25°C	-	32	-	

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<sup>&</sup>lt;sup>1</sup> Depending on thermal properties of assembly.

<sup>&</sup>lt;sup>2</sup> Not subject to production test - verified by design/characterization.

<sup>&</sup>lt;sup>3</sup> Allowed number of short circuits: <1000; time between short circuits: >1s.



### **Further Electrical Characteristics**

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

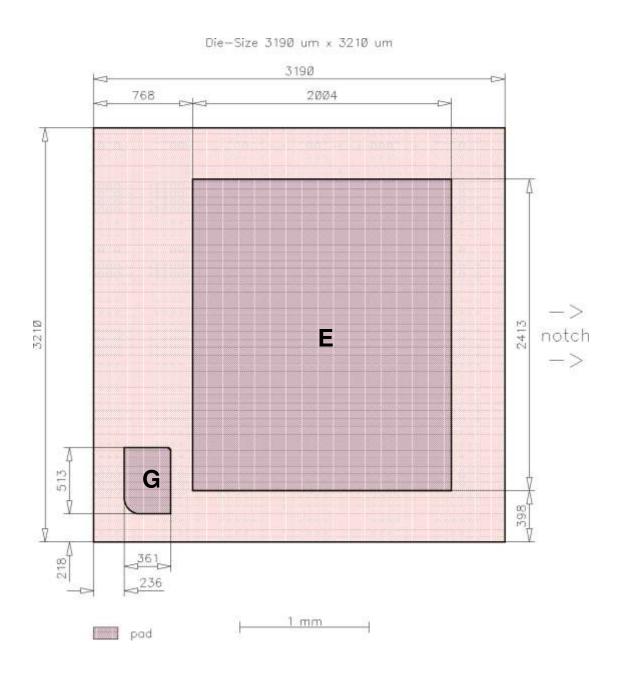
Application example	-	-
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### **Chip Drawing**



**E** = Emitter

**G** = Gate



### **Bare Die Product Specifics**

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

### **Description**

AQL 0.65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

### **Revision History**

Revision	Subjects (major changes since last revision)	Date
2.1	Wafer diameter changed to 200 mm	06.07.2010
2.2	Additional Basic Type, editorial changes	19.07.2017

Relevant App	olication Notes

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