CS4222

20-Bit Stereo Audio Codec with Volume Control

Features

- 99 dB Dynamic Range
- 110 dB DAC Signal-to-Noise Ratio (EIAJ)
- Analog Volume Control
  - 0.5 dB Step Resolution
  - 113.5 dB Attenuation
- Soft Mute Capability
- Differential Inputs/Outputs
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32, 44.1 and 48 kHz
- Stand-Alone or Control Port Mode
- Single +5 V power supply

Description

The CS4222 is a highly integrated, high performance, 20-bit, audio codec providing stereo analog-to-digital and stereo digital-to-analog converters using delta-sigma conversion techniques. The device operates from a single +5 V power supply, and features low power consumption. A selectable de-emphasis filter for 32, 44.1, and 48 kHz sample rates is also included.

The CS4222 also includes an analog volume control capable of 113.5 dB attenuation in 0.5 dB resolution. The analog volume control architecture preserves dynamic range during attenuation. Volume control changes are implemented using a "soft" ramping or zero crossing technique.

Applications include reverb processors, musical instruments, DAT, and multitrack recorders.

The CS4222 is packaged in a 28-pin plastic SSOP.

ORDERING INFORMATION

CS4222-KS	-10° to +70° C	28-pin SSOP
CS4222-BS	-40° to +85° C	28-pin SSOP
CS4222-DS	-40° to +85° C	28-pin SSOP
CDB4222		Evaluation Board

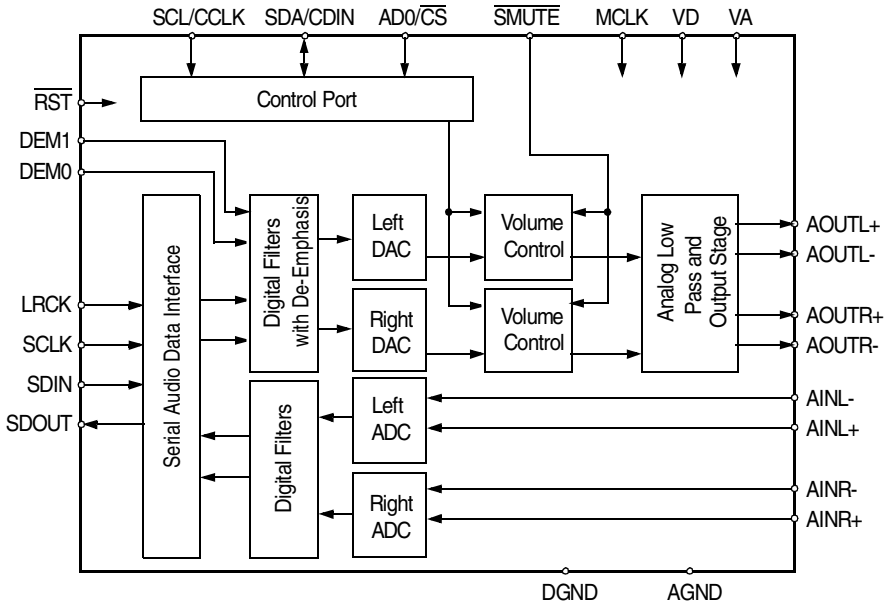


TABLE OF CONTENTS

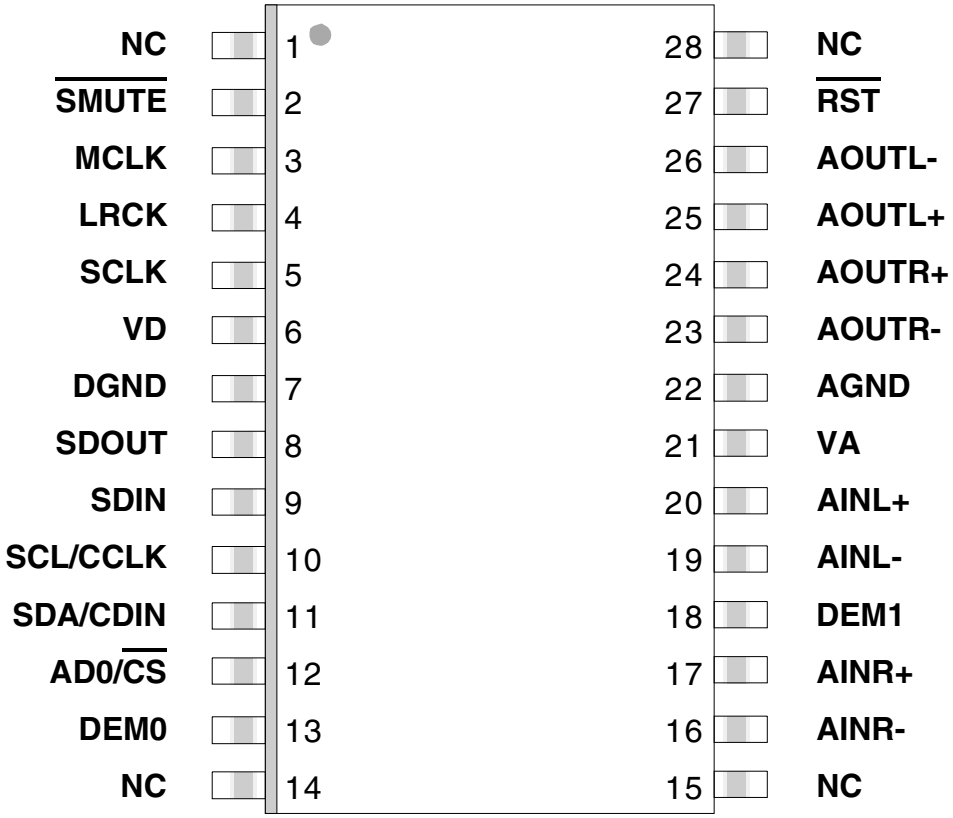
Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **http://www.cirrus.com/corporate/contacts/sales.cfm**

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTION



Pin Name	#	Pin Description
NC	1,14, 15, 28	**No Connect -** These pins are not connected internally and should be tied to DGND to minimize noise coupling.
$\overline{\text{SMUTE}}$	2	**Soft Mute (*Input*) -** Activates a muting function for both the left and right channel D/A converter outputs. Soft muting is achieved by ramping down the volume in 0.5 dB steps until achieving mute if SOFT bit (DAC Control Byte #2) is set to 0 (default).
LRCK	4	**Left/Right Clock (*Input*) -** Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs.
SCLK	5	**Serial Data Clock (*Input*) -** Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin.
VD	6	**Digital Power (*Input*) -** Positive power supply for the digital section. Nominally 5.0 VDC.
DGND	7	**Digital Ground (*Input*) -** Digital ground for the digital section.
SDOUT	8	**Serial Data Output (*Output*) -** Two's complement MSB-first serial data is output on this pin.
SDIN	9	**Serial Data Input (*Input*) -** Two's complement MSB-first serial data is input on this pin.
SCL/CCLK	10	**Serial Control Port Clock (*Input*) -** Serial clock for the control port interface. This pin should be tied to DGND in stand-alone mode.
SDA/CDIN	11	**Serial Control Port Data (*Input/Output*) -** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor according to the I^2C specification. CDIN in the input data line for the serial control port in SPI mode. This pin should be tied to DGND in stand-alone mode.
AD0/$\overline{\text{CS}}$	12	**Address Bit/Control Chip Select (*Input*) -** In I^2C mode, AD0 is a chip address bit. In SPI mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4222. The CS4222 will enter SPI mode if a negative transition is ever seen on this pin after power up. This pin should be tied to DGND in stand-alone mode.
DEM0 **DEM1**	13 18	**De-emphasis Control (*Input*)** - Selects the standard 15µs/50µs digital de-emphasis filter response for 32, 44.1 and 48 kHz sample rate.
AINR-, AINR+	16,17	**Differential Right Channel Analog Input (*Input*) -** Analog input connections of the right channel differential inputs. Typically 2 Vrms differential (1 Vrms for each input pin) for a fullscale analog input signal.
AINL-, AINL+	19,20	**Differential Left Channel Analog Input (*Input*) -** Analog input connections of the left channel differential inputs. Typically 2 Vrms differential (1 Vrms for each input pin) for a fullscale analog input signal.
VA	21	**Analog Power (*Input*) -** Positive power supply for the analog section. Typically 5.0 VDC.
AGND	22	**Analog Ground (*Input*) -** Analog ground reference.
AOUTR-, AOUTR+	23, 24	**Differential Right Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
AOUTL-, AOUTL+	25, 26	**Differential Left Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
$\overline{\text{RST}}$	27	**Reset (*Input*)** - When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

2. CHARACTERISTICS AND SPECIFICATIONS.

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Nom	Max	Units
Analog Supply Voltage	VA	4.75	5.0	5.25	V
Digital Supply Voltage	VD	4.75	5.0	5.25	V
Ambient Operating Temperature (Power Applied) -KS	T_A	-10	-	+70	°C
-BS/-DS		-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters	Symbol	Min	Max	Units
DC Power Supply Analog	VA	-0.3	6.0	V
Digital	VD	-0.3	6.0	V
Input Current (Note 1)	I_{in}	-	±10	mA
Analog Input Voltage		-0.7	VA+0.7	V
Digital Input Voltage		-0.7	VD+0.7	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Note: 1. Any pin except supplies.

ANALOG INPUT CHARACTERISTICS (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; VD = VA, Fs=48kHz)

Parameter		CS4222-KS Min	CS4222-KS Typ	CS4222-KS Max	CS4222-BS/-DS Min	CS4222-BS/-DS Typ	CS4222-BS/-DS Max	Unit
Dynamic Range	A-weighted	95	99	-	95	99	-	dB
	unweighted	92	96	-	92	96	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
	-1 dB	-	-90	-86	-	-90	-86	dB
	-20 dB	-	-76	-	-	-76	-	dB
	-60 dB	-	-36	-	-	-36	-	dB
Interchannel Isolation	(1 kHz)	-	90	-	-	90	-	dB
DC Accuracy								
Offset Error	(HPF Enabled)	-	0	-	-	0	-	mV_{RMS}
	(HPF Disabled)	-	20	-	-	20	-	mV_{RMS}
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Input								
Full Scale Differential Input Voltage		1.82	2.0	2.18	1.82	2.0	2.18	V_{RMS}
Input Resistance		-	10	-	-	10	-	kΩ
Input Capacitance		-	15	-	-	15	-	pF
Common Mode Input Voltage		-	2.3	-	-	2.3	-	V

ADC Digital Decimation Filter Characteristics (Note 3)					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Passband	to -0.01 dB corner	0	-	0.4535	Fs
Passband Ripple		-0.01	-	+0.01	dB
StopBand		0.625	-	-	Fs
StopBand Attenuation	(Note 4)	80	-	-	dB
Group Delay		-	15/Fs	-	s
Group Delay Variation		-	-	0	s
HPF Characteristics					
Frequency Response	-3 dB	-	3.7	-	Hz
	-0.1 dB	-	20	-	Hz
Phase Deviation	@ 20 Hz	-	10	-	Degree
Passband Ripple		-	-	0	dB

Notes: 2. Referenced to typical fullscale differential input voltage.

3. The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.

4. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz +/- 21.8 kHz; n = 0, 1, ...).

ANALOG OUTPUT CHARACTERISTICS (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF; VD = VA, Fs=48kHz)

Parameter		CS4222-KS Min	CS4222-KS Typ	CS4222-KS Max	CS4222-BS/-DS Min	CS4222-BS/-DS Typ	CS4222-BS/-DS Max	Unit
Dynamic Range	A-weighted	93	99	-	93	99	-	dB
	unweighted	90	96	-	90	96	-	dB
Total Harmonic Distortion + Noise	0 dB	-	-88	-84	-	-88	-84	dB
	-20 dB	-	-76	-	-	-76	-	dB
	-60 dB	-	-36	-	-	-36	-	dB
Idle Channel Noise / Signal-to-noise ratio (Note 5)		-	110	-	-	110	-	dB
Interchannel Isolation	(1 kHz)	-	90	-	-	90	-	dB
Attenuation Step Size		0.35	0.5	0.65	0.35	0.5	0.65	dB
Programmable Output Attenuation Span		110	113.5	-	110	113.5	-	dB
DC Accuracy								
Differential Offset Voltage		-	±10	-	-	±10	-	mV
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Analog Output								
Full Scale Output Voltage		1.9	2.0	2.1	1.9	2.0	2.1	V_{RMS}
Common Mode Output Voltage		-	2.3	-	-	2.3	-	V
AC-Load resistance		10	-	-	10	-	-	kΩ
Load Capacitance		-	-	100	-	-	100	pF

DAC Combined Interpolation & On-Chip Analog Filter Response (Note 6)					
Parameter		**Min**	**Typ**	**Max**	**Unit**
Passband	to 0.01 dB corner	0	-	0.4535	Fs
Passband Ripple		-0.01	-	+0.01	dB
Frequency Response 10 Hz to 20 kHz		-0.1	-	+0.1	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 7)	70	-	-	dB
Group Delay		-	16/Fs	-	s
Deviation from Linear Phase		-	±0.5	-	Degree

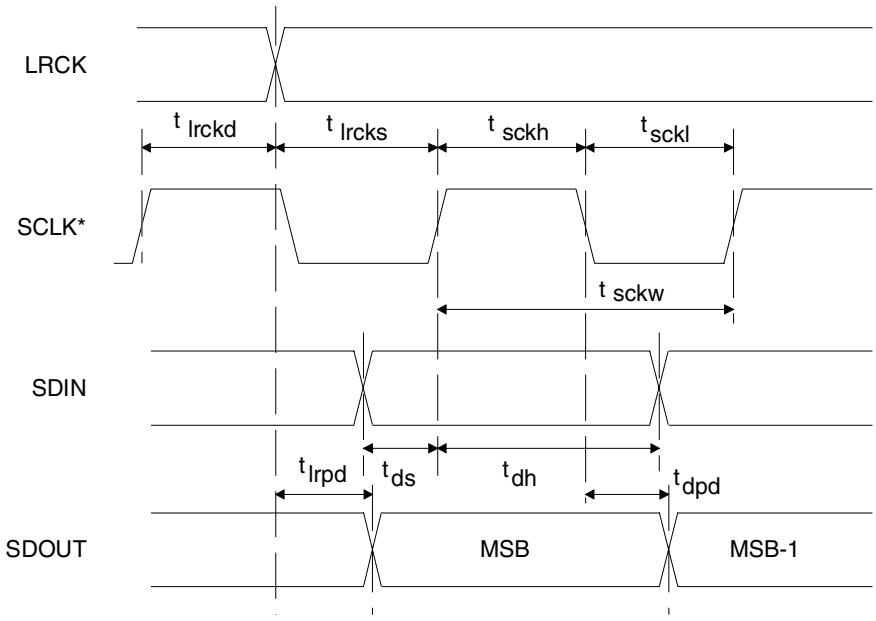
Notes: 5. DAC muted, A-weighted

6. The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.

7. Measurement bandwidth is 10 Hz to 3 Fs

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Parameters		Symbol	Min	Max	Units
$\overline{RST}$ Low Time			10	-	ms
MCLK Frequency			1.014	25.6	MHz
MCLK Pulse Width High	MCLK = 512 Fs MCLK = 384 Fs MCLK = 256 Fs		10 21 31	- - -	ns
MCLK Pulse Width Low	MCLK = 512 Fs MCLK = 384 Fs MCLK = 256 Fs		10 21 31	- - -	ns
Input Sample Rate		Fs	4	50	kHz
SCLK Frequency			-	128xFs	Hz
SCLK Pulse Width Low		t_{sckh}	40	-	ns
SCLK Pulse Width High		t_{sckl}	40	-	ns
SCLK rising to LRCK edge delay	(DSCK = 0)	t_{lrckd}	20	-	ns
SCLK rising to LRCK edge setup time	(DSCK = 0)	t_{lrcks}	40	-	ns
SDIN valid to SCLK rising setup time	(DSCK = 0)	t_{ds}	25	-	ns
SCLK rising to SDIN hold time	(DSCK = 0)	t_{dh}	25	-	ns
SCLK falling to SDOUT valid	(DSCK = 0)	t_{dpd}	-	$\frac{1}{(384)\ Fs} + 20$	s



*SCLK shown for DSCK = 0, SCLK inverted for DSCK = 1.

Figure 1. Serial Audio Interface Timing

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE (SPI) (Inputs: Logic 0 = DGND, Logic 1 = VD)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sck}	-	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 8)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 9)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 10)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 10)	t_{f2}	-	100	ns

Notes: 8. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

9. Data must be held for sufficient time to bridge the transition time of CCLK.

10. For f_{sclk} < 1 MHz.

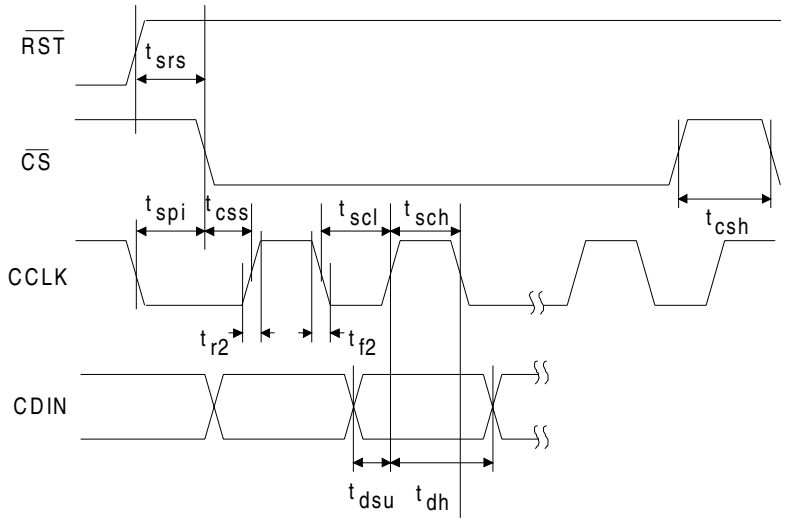


Figure 2. Control Port Timing - SPI Mode

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE (I^2C) (Continued)

Parameter	Symbol	Min	Max	Unit
I^2C Mode				
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 11)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_r	-	1	µs
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 11. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

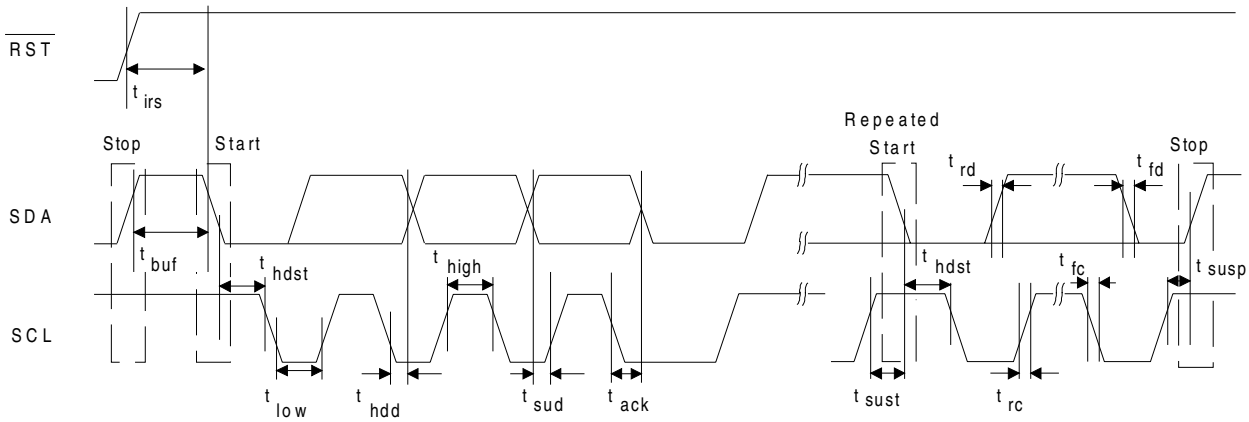


Figure 3. Control Port Timing - I^2C Mode

DC ELECTRICAL CHARACTERISTICS (AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power-down Mode (Note 12)						
Power Supply Current	All Supplies = 5.0 V		-	200	-	µA
Normal Operation (Note 13)						
Power Supply Current	VA = 5.0 V	I_A	-	30	40	mA
	VD = 5.0 V	I_D	-	20	26	mA
Power Supply Rejection Ratio	1 kHz, 10 mV_{RMS}	PSRR	-	50	-	dB

Notes: 12. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

13. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0dBFS digital input and a 1 kHz, -1 dB analog input sampled at F_s = 48 kHz, and open outputs, unless otherwise specified.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current		-	-	10	µA
Output Leakage Current		-	-	10	µA
MCLK Jitter Tolerance		-	500	-	ps_{RMS}

DIGITAL INTERFACE SPECIFICATIONS (AGND = DGND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Max	Units
High-Level Output Voltage (I_{OH} = -2.0 mA)	V_{OH}	VD - 1.0	-	V
Low-Level Output Voltage (I_{OL} = 2.0 mA)	V_{OL}	-	0.4	V
High-Level Input Voltage	V_{IH}	2.8	VD + 0.3	V
Low-Level Input Voltage	V_{IL}	-0.3	1.0	V

3. TYPICAL CONNECTION DIAGRAM

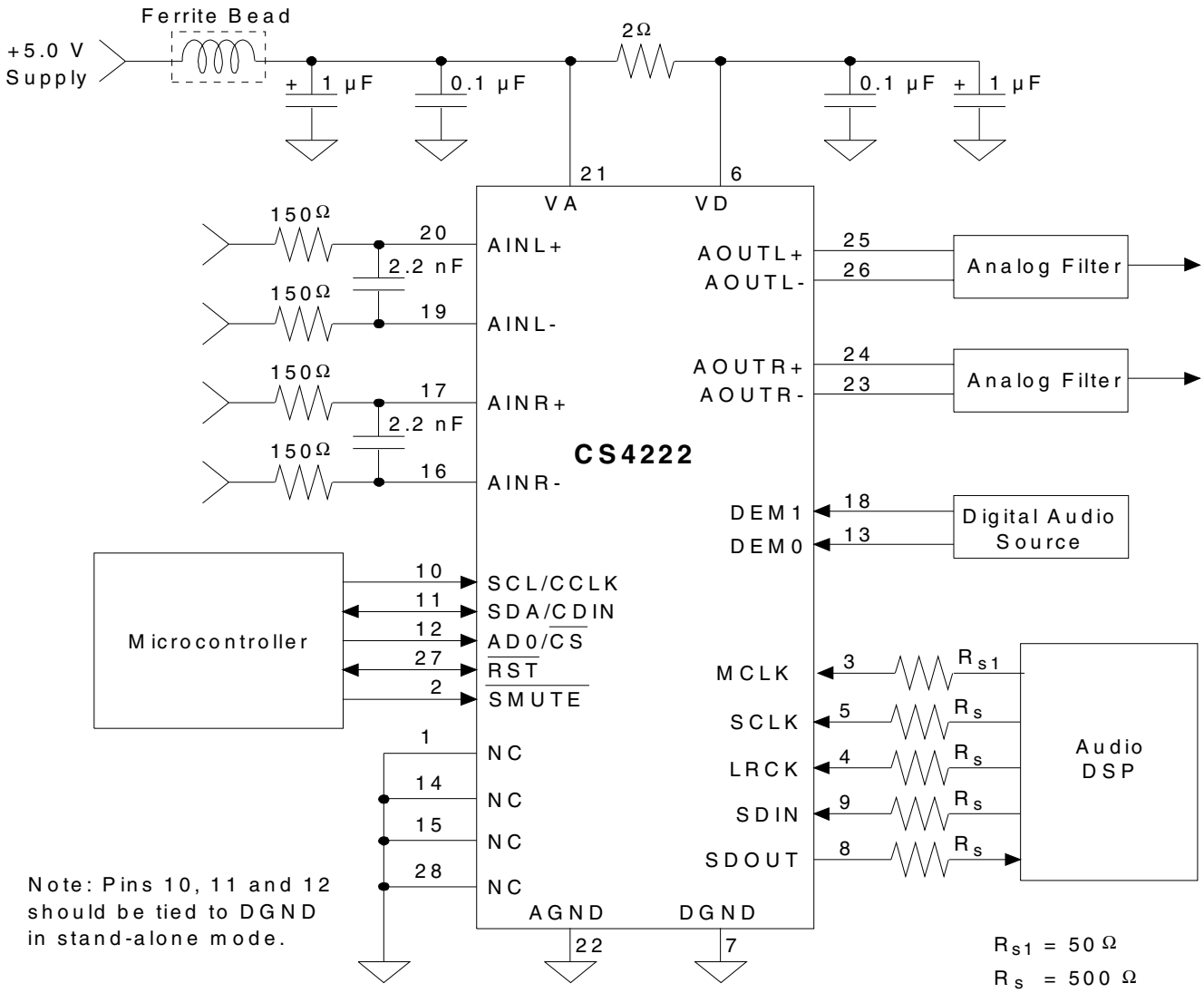


Figure 4. CS4222 Recommended Connection Diagram

4. APPLICATIONS

4.1 Overview

The CS4222 has 2 channels of 20-bit analog-to-digital conversion and 2 channels of 20-bit digital-to-analog conversion. All ADCs and DACs are delta-sigma converters. The DAC outputs on the CS4222 have adjustable output attenuation implemented in 0.5 dB step resolution. The device also includes digital de-emphasis for 32, 44.1, and 48 kHz.

Digital audio data for the DACs and from the ADCs is communicated over separate serial ports. This allows concurrent writing to and reading from the device. The CS4222 is a stand-alone device controlled via pins. Control for the functions available on the CS4222 are communicated over a serial microcontroller interface. Figure 4 shows the recommended connection diagram for the CS4222.

The device can be operated with or without the control port interface. Additional functions are available when the control port interface is used as outlined in Table 1.

Table 1. Control Port vs. Stand-Alone Mode

Control Port	Stand-Alone Mode
Volume control	-
Adjustable Mute ramp rate	Fixed Mute ramp rate
Enable zero crossing detect	Disabled
Enable/Disable mute on zero input	Enabled
De-emphasis	De-emphasis
Mute DAC outputs	Mute DAC outputs
ADC Input Peak Level Detect	-
16, 18, 20 bit Interface	20 bit I^2S Interface
Individual ADC/DAC power down	Codec power down
Cal on command	Cal on power-up
High pass enable/disable	High pass enabled

4.2 Analog Inputs

4.2.1 Line Level Inputs

AINR-, AINR+, AINL-, and AINL+ are the differential line level input pins (see Figure 4). Figure 5 shows an AC coupled optional input buffer which combines level shifting with single-ended to differential conversion. Analog inputs must be DC coupled into the CS4222 with a 2.3 V common mode input voltage. Any DC offset at the input to the CS4222 will be removed by the internal high-pass filters (see Figure 6 for the differential input signal description). The ADC outputs in the CS4222 may be muted (set to zero) by writing the ADMR and ADML bits, and can be independently powered down using the PDAD bit. ADMR, ADML, and PDAD are all located in the ADC control byte (#1).

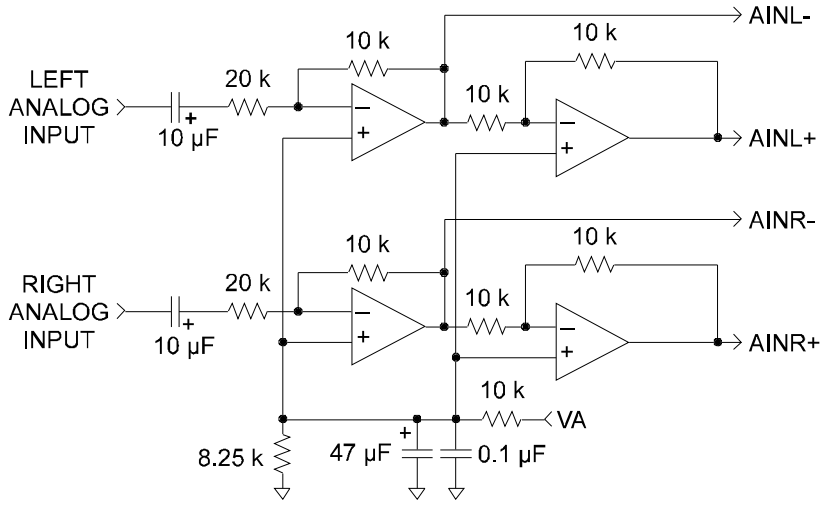


Figure 5. Optional Line Input Buffer

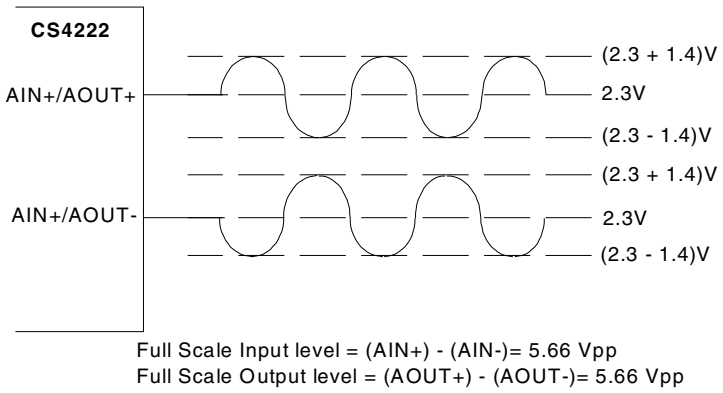


Figure 6. Full Scale Input/Output Voltage

4.2.2 Input Level Monitoring

The CS4222 includes independent Peak Input Level Monitoring for each channel. The analog-to-digital converter (ADC) continually monitors the peak digital signal for both channels, prior to the digital limiter, and records these values in the LVL2-0 (left channel) and LVR2-0 (right channel) bits in the Converter Status Report Byte (#6). These bits indicate whether the input level is clipping, -1 to -6 dB from full scale in 1 dB resolution, or below -6 dB from full scale. The LVL/LVR bits are "sticky" bits and are reset to zero when the DSP Port Mode Byte (#5) is read.

4.2.3 High Pass Filter

The operational amplifiers in the input circuitry driving the CS4222 may generate a small DC offset into the A/D converter. The CS4222 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multi-channel system. The characteristics of this first-order high pass filter are outlined below for Fs equal to 48 kHz. The filter response scales linearly with sample rate. The high pass filter in the CS4222 may be defeated independently for the left and right channels by writing HPDR and HPDL in the ADC control byte (#1).

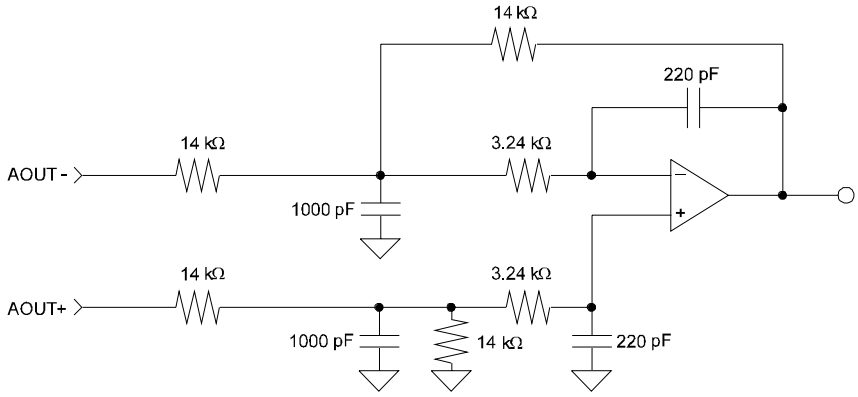
Table 2. High Pass Filter Characteristics

Frequency Response	**-3 dB @ 3.7 Hz -0.1 dB @ 20 Hz**
Phase Deviation	10 degrees @ 20 Hz
Passband Ripple	None

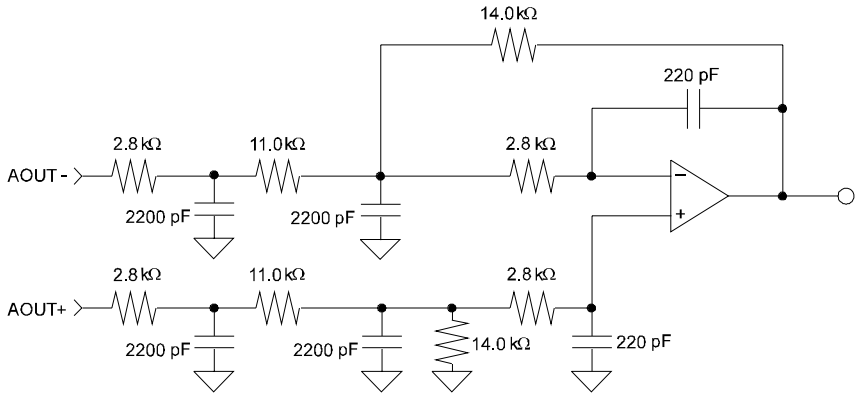
4.3 Analog Outputs

4.3.1 Line Level Outputs

The CS4222 contains an on-chip buffer amplifier producing differential outputs capable of driving 10 kΩ loads. Each output (AOUTL+, AOUTL-, AOUTR+, AOUTR-) will produce a nominal 2.83 Vpp (1 Vrms) output with a 2.3 volt common mode for a full scale digital input. This is equivalent to a 5.66 Vpp (2 Vrms) differential signal as shown in Figure 6. The recommended off-chip analog filter is either a 2nd order Butterworth or a 3rd order Butterworth, if greater out-of-band noise filtering is desired. The CS4222 DAC interpolation filter has been pre-compensated for an external 2nd order Butterworth filter with a 3 dB corner at Fs, or a 3rd order Butterworth filter with a 3 dB corner at 0.75 Fs to provide a flat frequency response and linear phase over the passband (see Figure 7 for Fs = 48 kHz). If the recommended filter is not used, small frequency response magnitude and phase errors will occur. In addition to providing out-of-band noise attenuation, the output filters shown in Figure 7 provide differential to single-ended conversion.



2-pole Butterworth Filter



3-pole Butterworth Filter

Figure 7. 2- and 3-Pole Butterworth Filters

4.3.2 Analog/Digital Volume Control (Control Port Mode only)

The DAC outputs are each routed through an attenuator which is adjustable in 0.5 dB steps. Output attenuation is available through the Output Attenuator Data Bytes (#3 & #4). Level changes are implemented with an analog volume control until the residual output noise is equal to the noise floor in the mute state at which point volume changes are performed digitally. This technique is superior to purely digital volume control techniques as the noise is attenuated by the same amount as the signal, thus preserving dynamic range (see Figure 8).

The CS4222 implements a "soft" volume control whereby level changes are achieved by ramping from the current level to the new level in 0.5 dB steps. The default rate of volume change is 8 LRCK cycles for each 0.5 dB step (equivalent to 647 µs at Fs = 48 kHz). The rate of volume change is adjustable to 4, 16, or 32 LRCK cycles with the RMP1/0 bits in the DAC control byte (#2).

"Soft" volume control may be disabled through the SOFT bit in the DAC bit Control Byte (#2). When "soft" volume control is defeated, level changes step from the current level to the new level in a single step. The volume change takes effect on a zero crossing to minimize audible artifacts. If there is no zero crossing, then the requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate). There is a separate zero crossing detector for each channel. ACCR and ACCL bits in the Converter Status Report Byte (#6) give feedback when a volume control change has taken effect for the right and left channel. This bit goes high when a new setting is loaded and returns low when it has taken effect.

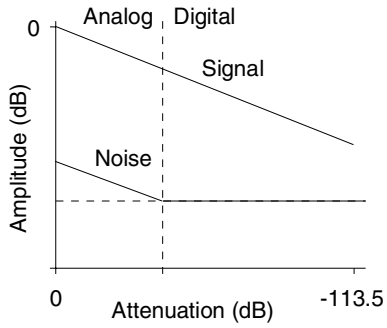


Figure 8. Hybrid Analog/Digital Attenuation

4.3.3 Soft Mute/Mute on Zero Input Data

Muting is achieved by hardware or software control. Soft mute can be achieved by lowering the $\overline{\text{SMUTE}}$ pin at which point the output level will ramp down in 0.5 dB steps to a muted state. Upon returning the $\overline{\text{SMUTE}}$ pin high, the output will ramp up to the volume control setting in the Output Attenuator Data Bytes (#3 & #4). “Soft” mute may be disabled through the SOFT bit in the DAC Control Byte (#2). When “soft” mute is defeated, muting occurs on zero crossings or after a time-out period, similar to the volume control changes.

Under software control, each output can be independently muted via mute control bits, MUTR and MUTL, in the DAC Control Byte (#2). Soft mute or zero crossing mute will be implemented depending on the state of the SOFT bit in the DAC Control Byte (#2).

Muting on consecutive zero input data is also provided where all DAC outputs will mute if they receive between 512 and 1024 consecutive zeros (or -1 code). Detection and muting is done independently for left and right channels. A single non-zero value will immediately unmute the DAC output. This feature is disabled on power-up, and it may be enabled with the MUTC bit in the DAC Control Byte (#2).

4.4 Master Clock Generation

The Master Clock, MCLK, is used to operate the digital filters and the delta-sigma modulator. MCLK must be either 256x, 384x, or 512x the desired Input Sample Rate, Fs. Fs is the frequency at which digital audio samples for each channel are input to the DAC or output from the ADC and is equal to the LRCK frequency. The MCLK to LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period. Internal dividers are then set to generate the proper clocks for the digital filters, delta-sigma modulators and switched-capacitor filter. Table 3 illustrates the standard audio sample rates and the required MCLK frequencies. If MCLK stops for 10 µs, the CS4222 will enter a power down state until the clock returns. The control port registers will maintain their current settings. It is required to have SCLK and LRCK derived from the master clock.

Table 3. Common Clock Frequencies

Fs (kHz)	MCLK (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

4.4.1 MCLK Timing Constraint

The rising edge of LRCK must be less than 5 ns or greater than 15 ns after the rising edge of MCLK. This timing constraint can be met by synchronizing the LRCK with either the rising or falling edge of MCLK.

4.5 Serial Audio Data Interface

4.5.1 Serial Audio Interface Signals

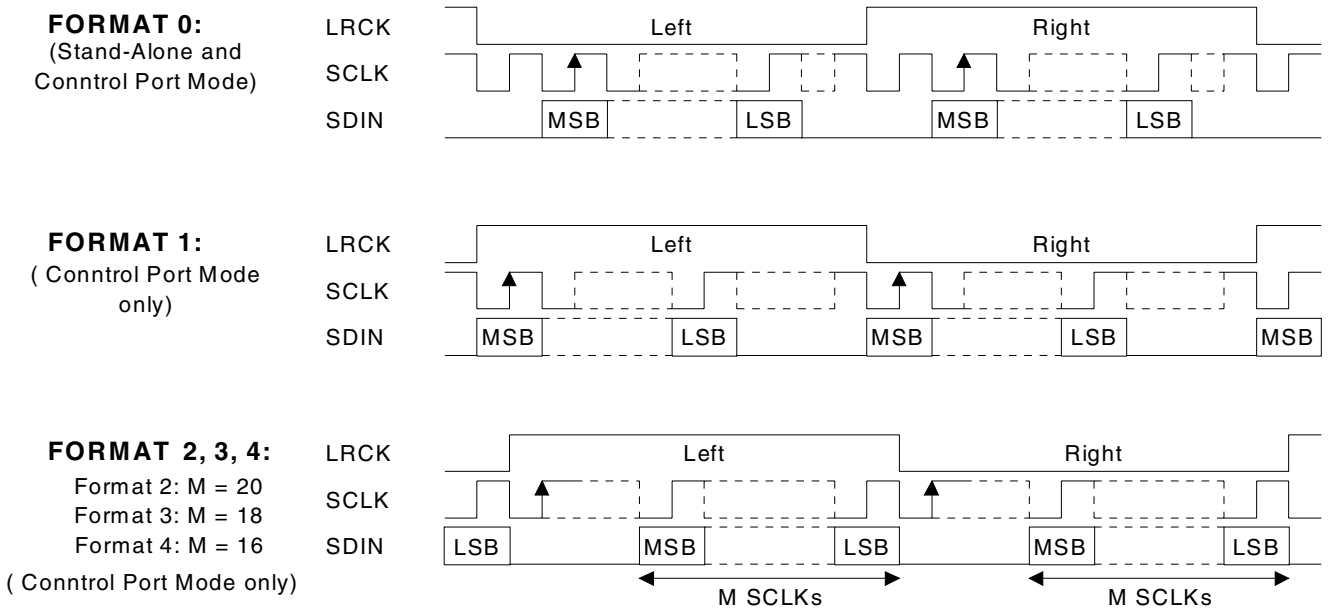
The serial interface clock, SCLK, is used for transmitting and receiving audio data. The active edge of SCLK is chosen by setting the DSCK bit in the DSP Port Mode Byte (#6). The default on power up is that data is valid on the rising edge for both input and output. SCLK is an input from an external source and at least 20 SCLK's per half period of LRCK are required for proper operation.

The Left/Right clock (LRCK) is used to indicate left and right data and the start of a new sample period. The frequency of LRCK must be equal to the system sample rate, Fs.

SDIN is the data input pin which drives a pair of DACs. SDOUT is the output data pin from the ADCs.

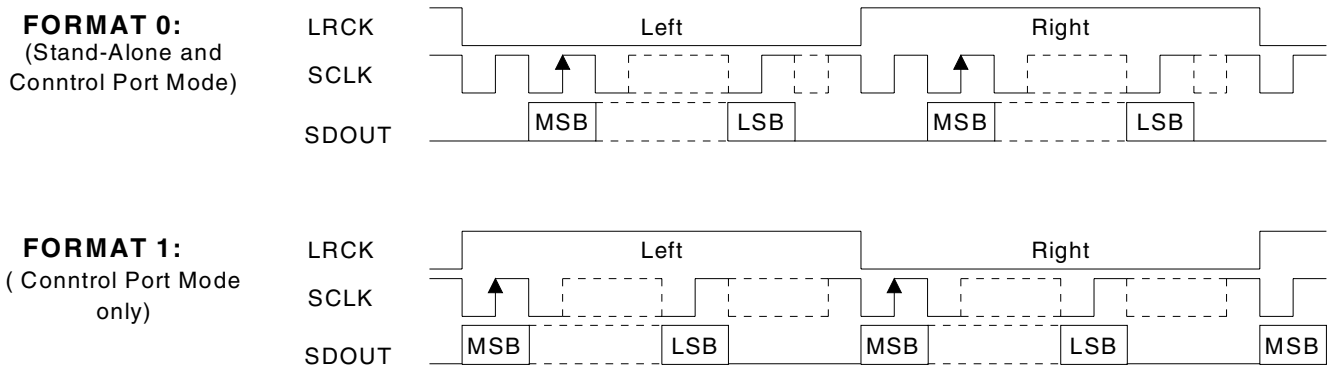
4.5.2 Serial Audio Interface Formats

The serial audio port supports 5 input and 2 output formats, shown in Figures 9 and 10. These interface formats are chosen via the DIF0/DIF1 pins. With the CS4222, these formats are chosen through the DSP Port Mode Byte (#5) with the DDO and DDI2/1/0 bits. The data output format is 20 bits and may be left justified or I^2S compatible depending on the state of the DDO bit. The input data format is set with the DDI bits to be left or right justified or I^2S compatible. In addition, the polarity of the SCLK edge used to clock in/out data from the CS4222 may be set via the DSCK bit in the DSP Port Mode Byte (#5). The default input and output format for the CS4222 is I^2S compatible.



Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

Figure 9. Audio DSP Data Input Formats.



Note: SCLK shown for DSCK = 0. SCLK inverted for DSCK = 1.

Figure 10. Audio DSP Data Output Formats.

4.6 Control Port Interface

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI® and I²C®, with the CS4222 operating as a slave device. If I²C operation is desired, AD0/$\overline{CS}$ should be tied to VD or DGND. If the CS4222 ever detects a negative transition on AD0/$\overline{CS}$ after power-up, SPI mode will be selected.

4.6.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4222 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 11 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. Register reading from the CS4222 is not supported in the SPI mode. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into a register designated by the MAP.

The CS4222 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive writes. If INCR is set to a 1, then MAP will auto increment after each byte is written, allowing block writes of successive registers. Register reading from the CS4222 is not supported in the SPI mode.

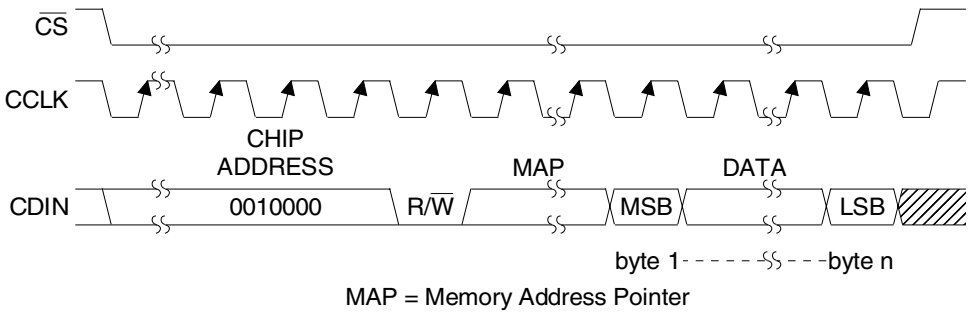


Figure 11. Control Port Timing, SPI mode

4.6.2 I²C Mode

In I²C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock-to-data relationship as shown in Figure 12. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VD or DGND as desired. The upper 6 bits of the 7 bit address field must be 001000. In order to communicate with the CS4222, the LSB of the chip address field (first byte sent to the CS4222) should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

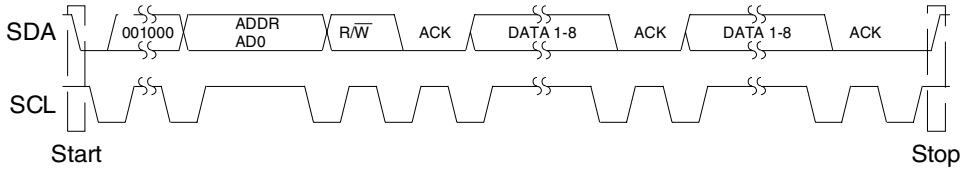


Figure 12. Control Port Timing, I²C mode

4.6.3 Control Port Bit Definitions

All registers can be written and read in I²C mode, except the Converter Status Report Byte (#6) and the CLKE and CALP bits in the ADC control byte (#1) which are read only. SPI mode only allows for register writing (see the following bit definition tables for bit assignment information).

4.7 De-Emphasis

The CS4222 is capable of digital de-emphasis for 32, 44.1, or 48 kHz sample rates. Implementation of digital de-emphasis requires reconfiguration of the digital filter to maintain the filter response at multiple sample rates (see Figure 13).

De-emphasis control is achieved with the DEM1/0 pins or through the DEM2-0 bits in the DSP Port Mode Byte (#2). The default state on power-up is de-emphasis controlled via the DEM1/0 pins (DEM2-0 bits=0). DEM1/0 pin control is defined in Table 4.

Table 4. De-Emphasis filter control

DEM 1	DEM 0	De-emphasis
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	OFF

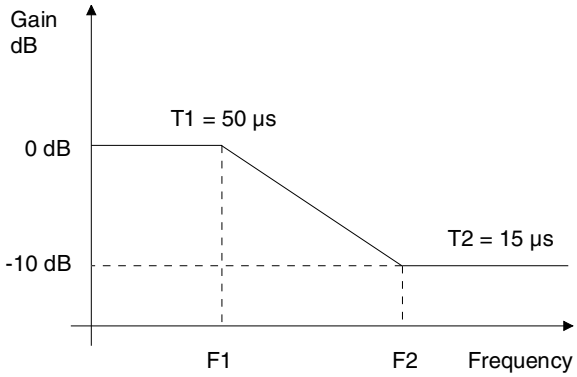


Figure 13. De-emphasis Curve.

4.8 Power-up / Reset / Power Down / Calibration

Upon power up, the user should hold $\overline{RST}$ = 0 for approximately 10 ms. In this state, the control port is reset to its default settings and the part remains in the power down mode. At the end of $\overline{RST}$, the device performs an offset calibration which lasts approximately 50 ms after which the device enters normal operation. A calibration may also be initiated via the CAL bit in the ADC Control Byte (#1). The CALP bit in the ADC Control Byte is a read only bit indicating the status of the calibration.

Reset/Power Down is achieved by lowering the $\overline{RST}$ pin causing the part to enter power down. Once $\overline{RST}$ goes high, the control port is functional and the desired settings should be loaded.

The CS4222 will also enter power down mode if the master clock source stops for approximately 10 µs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings.

Additionally, the PDAD (ADC Control Byte #1) and PDDA (DAC Control Byte #2) bits can be used to power down the ADC's and DAC's independently. If both are set to 1, the CS4222 will power down the entire chip. The control port will retain its current settings.

The CS4222 will mute the analog outputs and enter the power down mode if the supply drops below approximately 4 volts.

4.9 Power Supply, Layout and Grounding

As with any high resolution converter, the CS4222 requires careful attention to power supply and grounding arrangements to optimize performance. The Typical Connection Diagram shows the recommended power arrangement with VA, and VD connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but the recommended decoupling capacitors should still be placed on each supply pin. The AGND and DGND pins should be tied together with solid ground plane fill underneath the converter extending out to the GND side of the decoupling caps for VA, and VD. This recommended layout can be seen in the CDB4222 evaluation board and data sheet.

4.10 ADC and DAC Filter Response Plots

Figures 14 through 19 show the overall frequency response, passband ripple and transition band for the CS4222 ADCs and DACs.

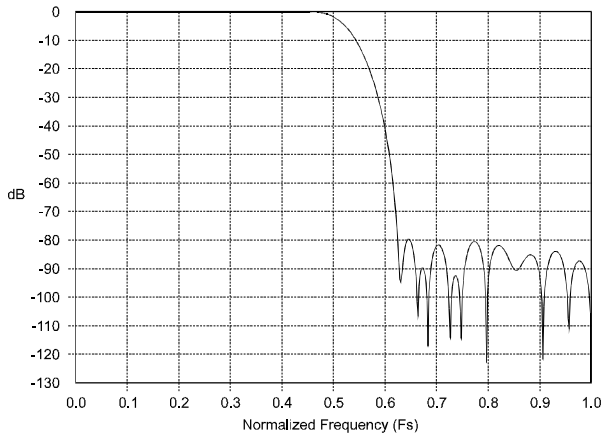


Figure 14. ADC Filter Response

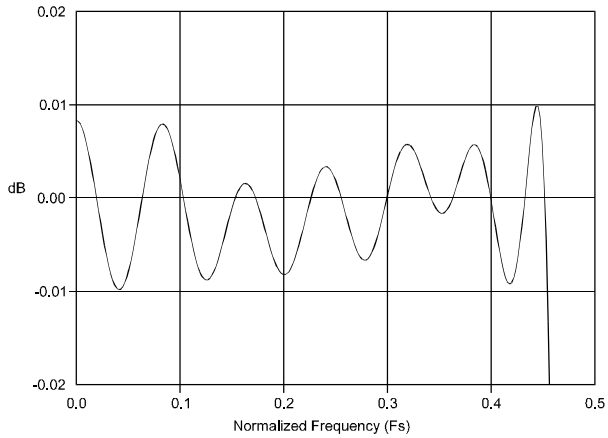


Figure 15. ADC Passband Ripplee

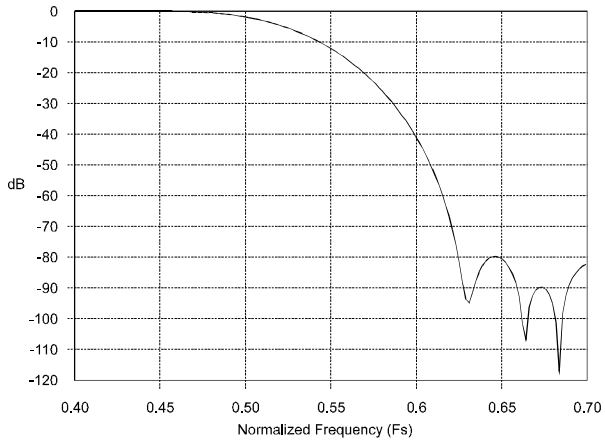


Figure 16. ADC Transition Band

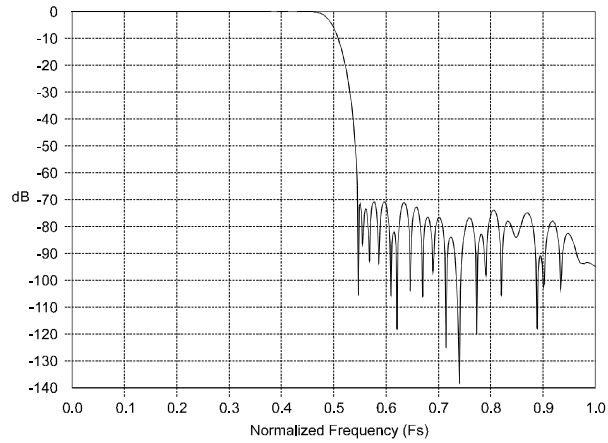


Figure 17. DAC Filter Response

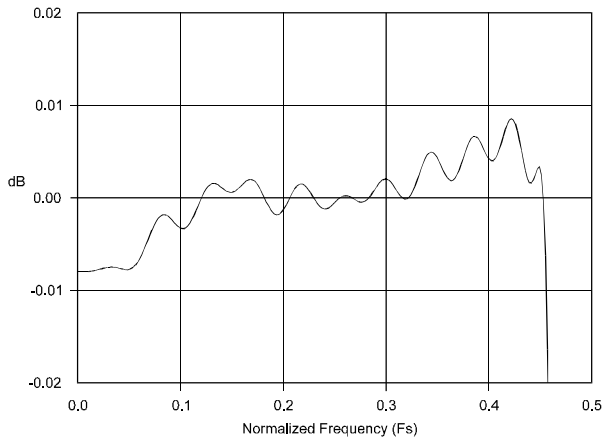


Figure 18. DAC Passband Ripple

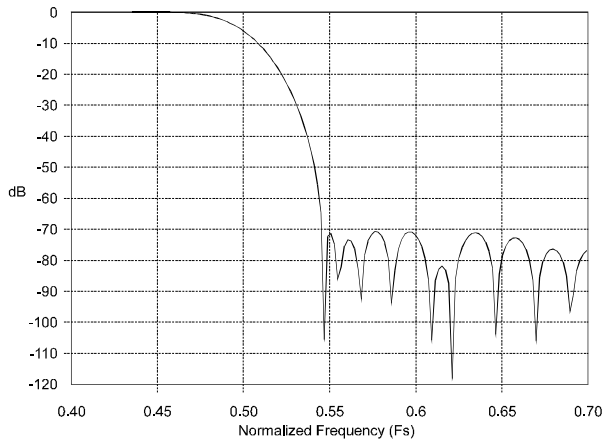


Figure 19. DAC Transition Band

5. REGISTER DESCRIPTIONS

Memory Address Pointer (MAP)

B7	B6	B5	B4	B3	B2	B1	B0
INCR	0	0	0	0	MAP2	MAP1	MAP0

MAP2-MAP0 Register Pointer

INCR Auto Increment Control Bit
0 - No auto increment
1 - Auto increment on

This register defaults to 00h.

Reserved Byte (0)

This byte is reserved for internal use and must be set to 00h for normal operation.

This register defaults to 00h.

ADC Control Byte (1)

B7	B6	B5	B4	B3	B2	B1	B0
PDAD	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE

PDAD Power Down
0 - Normal
1 - Power Down

HPDR-HPDL High pass filter defeat, right and left
0 - High pass filters active
1 - High pass filters defeated

ADMR-ADML ADC Muting, right and left
0 - Normal
1 - Output muted

CAL Calibration control bit
0 - Normal operation
1 - Rising edge initiates calibration

The following bits are read only:

CALP Calibration status
0 - Calibration done
1 - Calibration in progress

CLKE Clocking Error
0 - No error
1 - error

This register defaults to 00h.

DAC Control Byte (2)

B7	B6	B5	B4	B3	B2	B1	B0
PDDA	MUTC	MUTR	MUTL	SOFT	0	RMP1	RMP0

PDDA — Powers down DAC
0 - Normal.
1 - Power down

MUTC — Controls mute on consecutive zeros function
0 - 512 consecutive zeros will mute DAC
1 - DAC output will not mute on zeros.

MUTR-MUTL — Mute control bits
0 - Normal output level
1 - Selected DAC output muted

SOFT — Soft Mute Control
0 - Volume control changes, muting and mute-on-zeros occur with "ramp"
1 - Volume control changes, muting and mute-on-zeros occur on zero crossings

RMP1-0 — Soft Volume 0.5 dB step rate
0 - 1 step per 8 LRCK's
1 - 1 step per 4 LRCK's
2 - 1 step per 16 LRCK's
3 - 1 step per 32 LRCK's

This register defaults to 00h.

Output Attenuator Data Byte (3, 4)

B7	B6	B5	B4	B3	B2	B1	B0
ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

ATT7-ATT0 — Sets attenuator level
0 - No attenuation
227 - 113.5 dB attenuation
>227 - DAC muted
ATT0 represents 0.5 dB of attenuation

This register defaults to 00h.

DSP Port Mode Byte (5)

B7	B6	B5	B4	B3	B2	B1	B0
DEM2	DEM1	DEM0	DSCK	DDO	DDF2	DDF1	DDF0

DEM2-0 Selects de-emphasis control source

0 - De-emphasis controlled by pins

1 - 44.1 kHz de-emphasis setting
2 - 48 kHz de-emphasis setting
3 - 32 kHz de-emphasis setting
4 - De-emphasis disabled

5, 6, 7 - Not used

DSCK Sets the polarity of clocking data for both input and output
0 - Data valid on rising edge of SCLK
1 - Data valid on falling edge of SCLK

DDO Data output format
0 - I^2S compatible
1 - Left justified

DDI2-DDI0 Data input format
0 - I^2S compatible
1 - Left justified
2 - Right justified, 20-bit

3 - Right justified, 18-bit

4 - Right justified, 16-bit

5, 6, 7 - Not used

This register defaults to 00h.

Converter Status Report Byte (Read Only) (6)

B7	B6	B5	B4	B3	B2	B1	B0
ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL2	LVL0

ACCR-ACCL Acceptance bit
0 - ATT7-0 has been accepted
1 - New setting waiting for zero crossing

LVL2-0,LVR2-0 Left and Right ADC output level
0 - Normal output levels
1 - -6 dB level
2 - -5 dB level
3 - -4 dB level
4 - -3 dB level
5 - -2 dB level
6 - -1 dB level
7 - Clipping

LVL2-0 and LVR2-0 bits are 'sticky'. They constantly monitor the ADC output for the peak levels and hold the maximum output. They are reset to 0 when the *DSP Port Mode Byte (5)* is read.

This register is read only.

6. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFS as suggested in AES17-1991 Annex A and DACs are measured at 0 dBFS.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1 kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

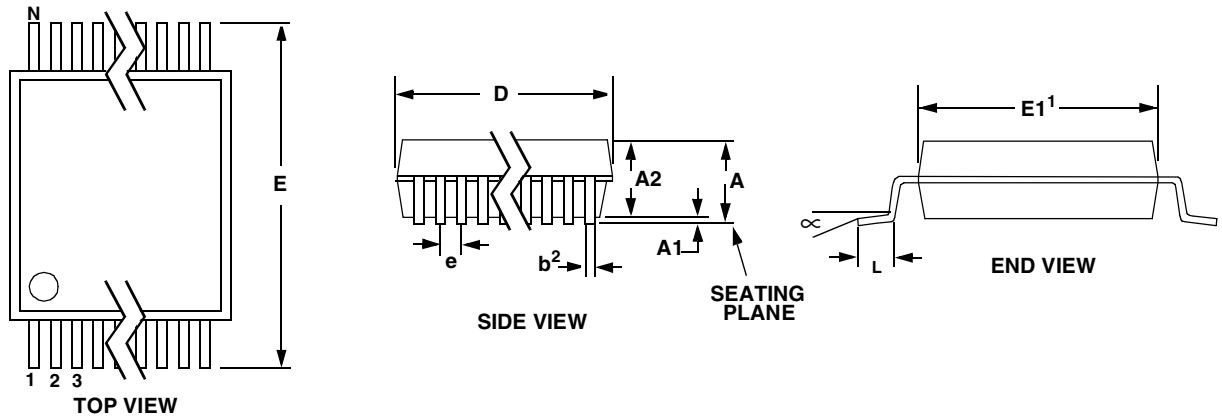
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected inputs tied to a common potential. For the DAC's, the differential output voltage with mid-scale input code. Units are in volts.

7. PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES		MILLIMETERS		NOTE
DIM	MIN	MAX	MIN	MAX	
A	--	0.084	--	2.13	
A1	0.002	0.010	0.05	0.25	
A2	0.064	0.074	1.62	1.88	
b	0.009	0.015	0.22	0.38	15,16
D	0.390	0.413	9.90	10.50	14
E	0.291	0.323	7.40	8.20	
E1	0.197	0.220	5.00	5.60	14
e	0.024	0.027	0.61	0.69	
L	0.025	0.040	0.63	1.03	
∝	0°	8°	0°	8°	

Notes: 14. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line. Mold flash or protrusions shall not exceed 0.20 mm per side.

15. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

16. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.