SCAS546B - NOVEMBER 1995 - REVISED MAY 1996

- Provides System Clock Solution for Pentium™/82430X/82430VX and Pentium Pro 82440FX Chipsets
- Four Host-Clock Outputs With Programmable Frequency (50 MHz, 60 MHz and 66 MHz)
- Six PCI Clock Outputs at Half-CPU Frequency
- One 48-MHz Universal Serial Bus (USB) Clock Output
- Three 14.318-MHz Reference Clock Outputs
- All Output Clock Frequencies Derived From a Single 14.31818-MHz Crystal Input
- LVTTL-Compatible Inputs and Outputs
- Internal Loop Filters for Phase-Locked Loops Eliminate the Need for External Components
- Operates at 3.3 V_{CC}
- Packaged in Plastic Small-Outline Package

(TOP VIEW) 28 REF0 V_{CC} X1 🛮 2 27 REF1 26 V_{CC} X2 **∏** 3 25 REF2 GND 4 OE [5 24 N SBCLK HCLK0 6 23 **∏** GND HCLK1 **∏** 7 22 PCLK0 V_{CC} [] 8 21 | PCLK1 HCLK2 9 20 VCC HCLK3 10 19 PCLK2 18 PCLK3 GND **1** 11 SEL1 12 17 ¶ GND SEL0 [] 13 16 PCLK4 15 PCLK5 V_{CC}

DW PACKAGE

description

The CDC9842 is a high-performance clock synthesizer/driver that generates the system clocks necessary to support Pentium™/82430X/82430VX and Pentium Pro 82440FX chipsets. Four host-clock outputs (HCLKn) are programmable to one of three frequencies (50 MHz, 60 MHz, or 66 MHz) via the SEL0 and SEL1 control inputs. Six PCI-clock outputs (PCLKn) are half the frequency of CPU clock outputs and are delayed 1 ns to 4 ns from the rising edge of the CPU clock. In addition, a universal serial bus (USB) clock output at 48 MHz (SBCLK) and three 14.318-MHz reference clock outputs (REF0, REF1, REF2) are provided.

All output frequencies are generated from a 14.318-MHZ crystal input. A reference clock can be provided at the X1 input instead of a crystal input.

Two phase-locked loops (PLLs) are used to generate the host clock frequency and the 48-MHz clock frequency. On-chip loop filters and internal feedback eliminate the need for external components. The PCI-clock frequency is derived directly from the host-clock frequency. The PLL circuit can be bypassed in the TEST mode (i.e., SEL0 = SEL1 = H) to distribute a test clock provided at the X1 input.

The host- and PCI-clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs are 3 state and are enabled via OE.

Because the CDC9842 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at the X1 input, as well as following any changes to the OE or SELn inputs.



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CDC9842 PC MOTHERBOARD CLOCK SYNTHESIZER/DRIVER WITH 3-STATE OUTPUTS SCAS546B - NOVEMBER 1995 - REVISED MAY 1996

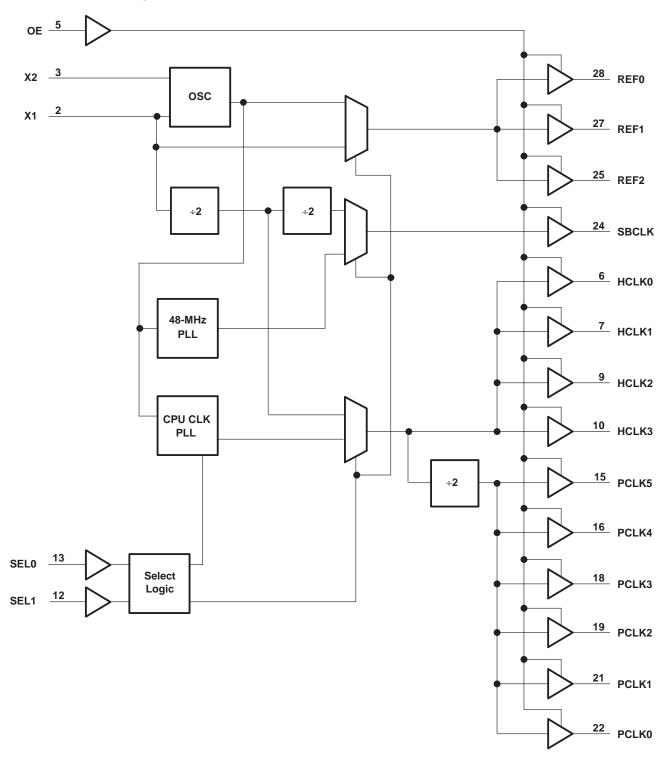
FUNCTION TABLE

OE	SEL0	SEL1	X1	HCLKn	PCLKn	REFn	SBCLK
L	Х	Х	14.318 MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Н	L	L	14.318 MHz	50 MHz	25 MHz	14.318 MHz	48 MHz
Н	L	Н	14.318 MHz	60 MHz	30 MHz	14.318 MHz	48 MHz
Н	Н	L	14.318 MHz	66 MHz	33 MHz	14.318 MHz	48 MHz
Н	Н	Н	TCLK [†]	TCLK/2	TCLK/4	TCLK	TCLK/4

[†] TCLK is a test-clock input at the X1 input during test mode.



functional block diagram





CDC9842 PC MOTHERBOARD CLOCK SYNTHESIZER/DRIVER WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
V _O (see Note 1)	V to V_{CC} + 0.5 V
Current into any output in the low state, I _O	16 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	−50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2)	1.2 W
Storage temperature range, T _{stg}	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	3.135	3.6	V
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
VI	Input voltage	0	VCC	V
ІОН	High-level output current		-8	mA
loL	Low-level output current		8	mA
TA	Operating free-air temperature	0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		T _A = 25°C			UNIT		
PARAMETER		MIN	TYP [‡]	MAX	ONIT		
VIK	$V_{CC} = 3.135 \text{ V},$	I _I = -18 mA				-1.2	V
Voн	$V_{CC} = 3.135 \text{ V},$	$I_{OH} = -8 \text{ mA}$		2.5			V
V _{OL}	$V_{CC} = 3.135 \text{ V},$	$I_{OL} = 8 \text{ mA}$				0.4	V
lį	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND				±1	μΑ
loz	$V_{CC} = 3.6 \text{ V},$	$V_O = V_{CC}$ or GND					μΑ
loo	V _{CC} = 3.6 V,	I _O = 0,	Outputs enabled§			50	mA
Icc	$V_I = V_{CC}$ or GND		Outputs disabled			1	mA
Ci	$V_I = V_{CC}$ or GND				6		pF
Co	$V_O = V_{CC}$ or GND				6		pF

[‡] All typical values are at $V_{CC} = 3.3 \text{ V}$.



[§] Device in normal operating mode with no load on outputs

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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
	After SEL1, SEL0		5	
Stabilization time†	After OE↑		5	ms
	After power up		5	ļ

Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at X1. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

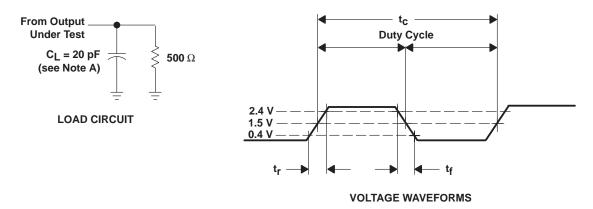
switching characteristics (see Figures 1 and 2)

PARAMETER	FROM (INPUT)		TO (OUTPUT)	V _{CC} = 3.135 V to 3.6 V, T _A = 0°C to 70°C		UNIT
				MIN	MAX	
. +		HCLKn			200	ps
t _{skew} ‡			PCLKn		400	ps
Offset [‡]	HCLKn		1	4	ns	
ru t			HCKLn		±250	ps
Jitter‡		PCLKn			±350	ps
Duty cycle		Any output		45%	55%	
			SEL0 = L, SEL1 = L	20		ns
		HCKLn	SEL0 = L, SEL1 = H	16.7		ns
. +			SEL0 = H, SEL1 = L	15		ns
t _C ‡			SEL0 = L, SEL1 = L	40		ns
		PCLKn	SEL0 = L, SEL1 = H	33.3		ns
			SEL0 = H, SEL1 = L	30		ns
t _r ‡§		HCLKn PCKLn			2	no
ι _γ +3						ns
. +8		HCKLn			2	200
t _f ‡§			PCLKn]		ns

[‡] Specifications are applicable only after the PLL stabilization time has elapsed.

 $[\]S$ Rise and fall times are characterized using the load circuits shown in Figure 1.

PARAMETER MEASUREMENT INFORMATION CLOCK DRIVER CIRCUITS



NOTES: A. CL includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50~\Omega$, $t_\Gamma \leq 2.5~ns$, $t_f \leq 2.5~ns$.
- C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

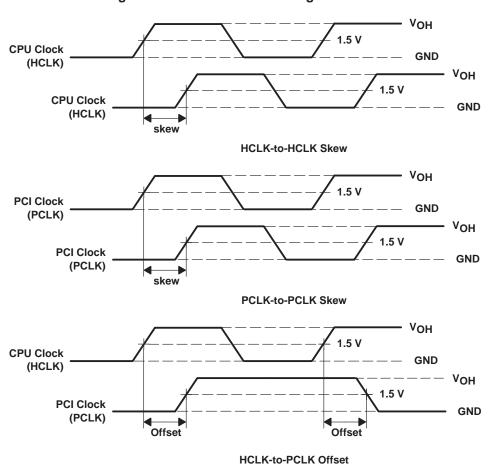


Figure 2. Waveforms for Calculation of t_{skew} and Offset





PACKAGE OPTION ADDENDUM

30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CDC9842DW	OBSOLETE	SOIC	DW	28	TBD	Call TI	Call TI
CDC9842DWR	OBSOLETE	SOIC	DW	28	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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