

# TWR-K65F180M User's Guide

## 1 Introduction

The K65F180M Tower MCU Module (TWR-K65F180M) is a low-cost evaluation, demonstration, and development board, which features the Kinetis 180 MHz K65 low-power MCU. The TWR-K65F180M microcontroller module can operate in stand-alone mode or as part of the Freescale Tower System, a modular development platform that enables rapid prototyping and tool re-use through reconfigurable hardware. Take your design to the next level and begin constructing your Tower System today by visiting [freescale.com/tower](http://freescale.com/tower) for additional Tower System microcontroller modules and compatible peripherals.

## Contents

1	Introduction	1
1.1	Features	2
1.2	Getting started	3
2	Contents	3
3	Hardware description	4
3.1	K65F180M microcontroller	4
3.2	Clocking	5
3.3	System power	5
3.4	Tamper module (Dryice) and Real-Time Clock supply	6
3.5	Serial and Debug Adapter version 2 (OpenSDAv2)	6
3.6	Cortex Debug connector	7
3.7	External Bus Interface – FlexBus	7
3.8	SDRAM	8
3.9	Accelerometer	8
3.10	Potentiometer, Pushbuttons, LEDs	8
3.11	General Purpose Tower Plug-in (TWRPI) socket	9
3.12	Touch interface	9
3.13	USB interface	10
3.14	Secure digital card slot	10
3.15	Ethernet and 1588	11
4	Jumper table	11
5	Input/output connectors and pin usage table	13
6	Elevator connections	14
7	References	16
8	Revision history	17

## 1.1 Features

The following list summarizes the features of the K65F180M Tower MCU boards:

- Tower compatible processor board
- K20 based OPENSDA circuit
- Four user-controlled status LEDs
- Two Capacitive Touch Pads and two mechanical push buttons
- Socket for Tower Plug-in (TWRPI, for instance a sensor board)
- Standalone high speed USB host and device function
- Potentiometer
- SDRAM connection
- MMA8451Q three-axis accelerometer
- Battery holder for 20 mm lithium battery (battery diameter 20 mm, thickness 25 mm)
- Board power select with 3.3 V or 1.8 V MCU operation
- MicroSD card slot
- OpenSDA USB

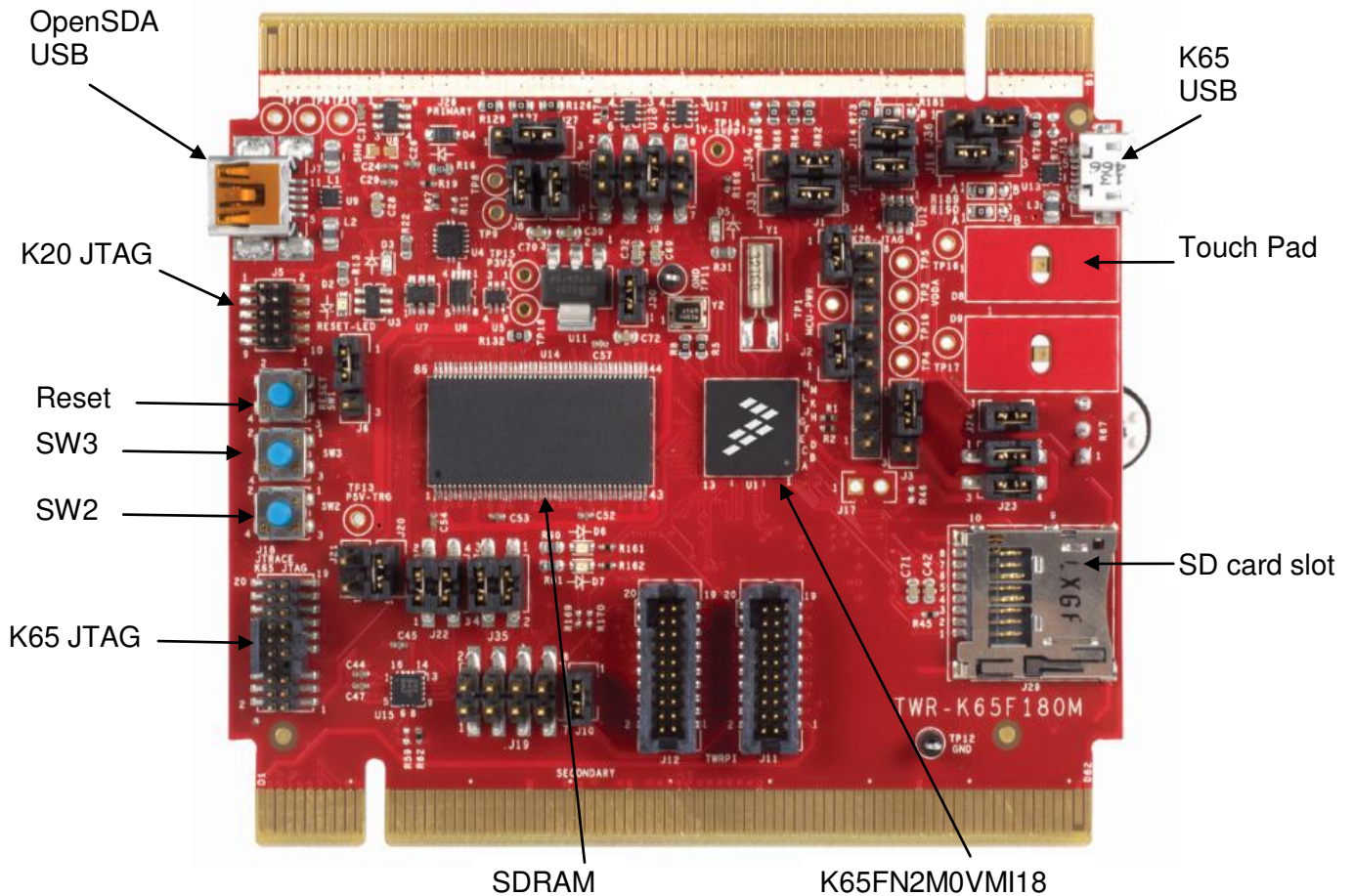


Figure 1. Front side of the TWR-K65F180M module

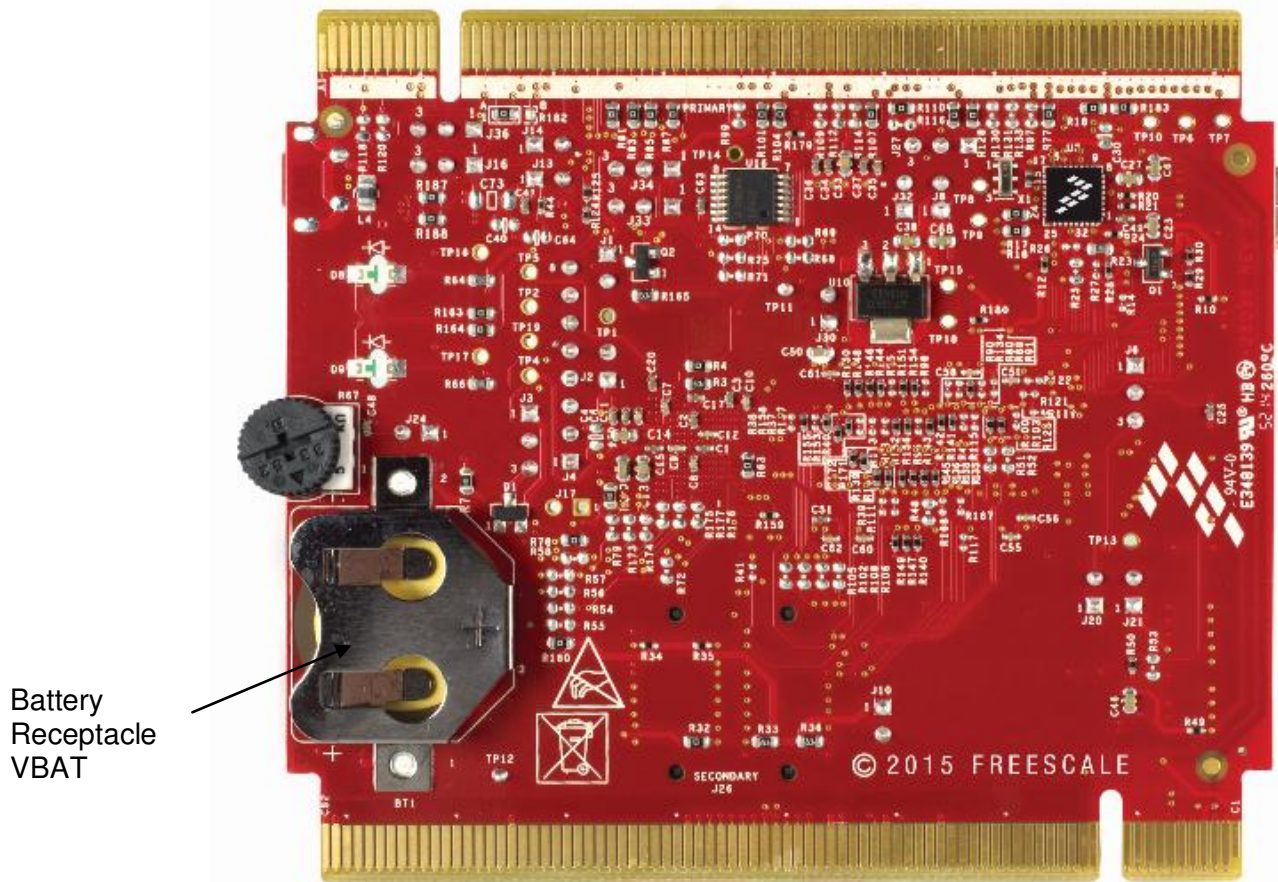


Figure 2. Back side of the TWR-K65F180M module

## 1.2 Getting started

You can find a printed version of the Quick Start Guide in the TWR-K65F180M box that contains the list of recommended steps for getting started.

## 2 Contents

The TWR-K65F180M includes:

- TWR-K65F180M for board assembly
- Quick Start Guide
- USB A to mini-B cable for debug interface and power supply
- CR2032 coin cell battery for VBAT power supply
- USB A to micro-B cable for K65FN2M0VMI18 USB interface

### 3 Hardware description

The TWR-K65F180M is a Tower MCU Module featuring the K65FN2M0VMI18 – an ARM<sup>®</sup> Cortex<sup>®</sup>-M4F based MCU with 2 MB on-chip flash, 256 KB on-chip SRAM, SDRAM controller and dual USB controllers in a 169 pin MAPBGA package. It has a maximum core operating frequency of 180 MHz. It is intended for use in the Freescale Tower System but can operate as a stand-alone module. An on-board debug circuit, OPENSDA, provides the SWD debug interface and power supply input through a single USB mini-AB connector. The following sections describe the hardware in more detail. This figure shows a block diagram for the TWR-K65F180M.

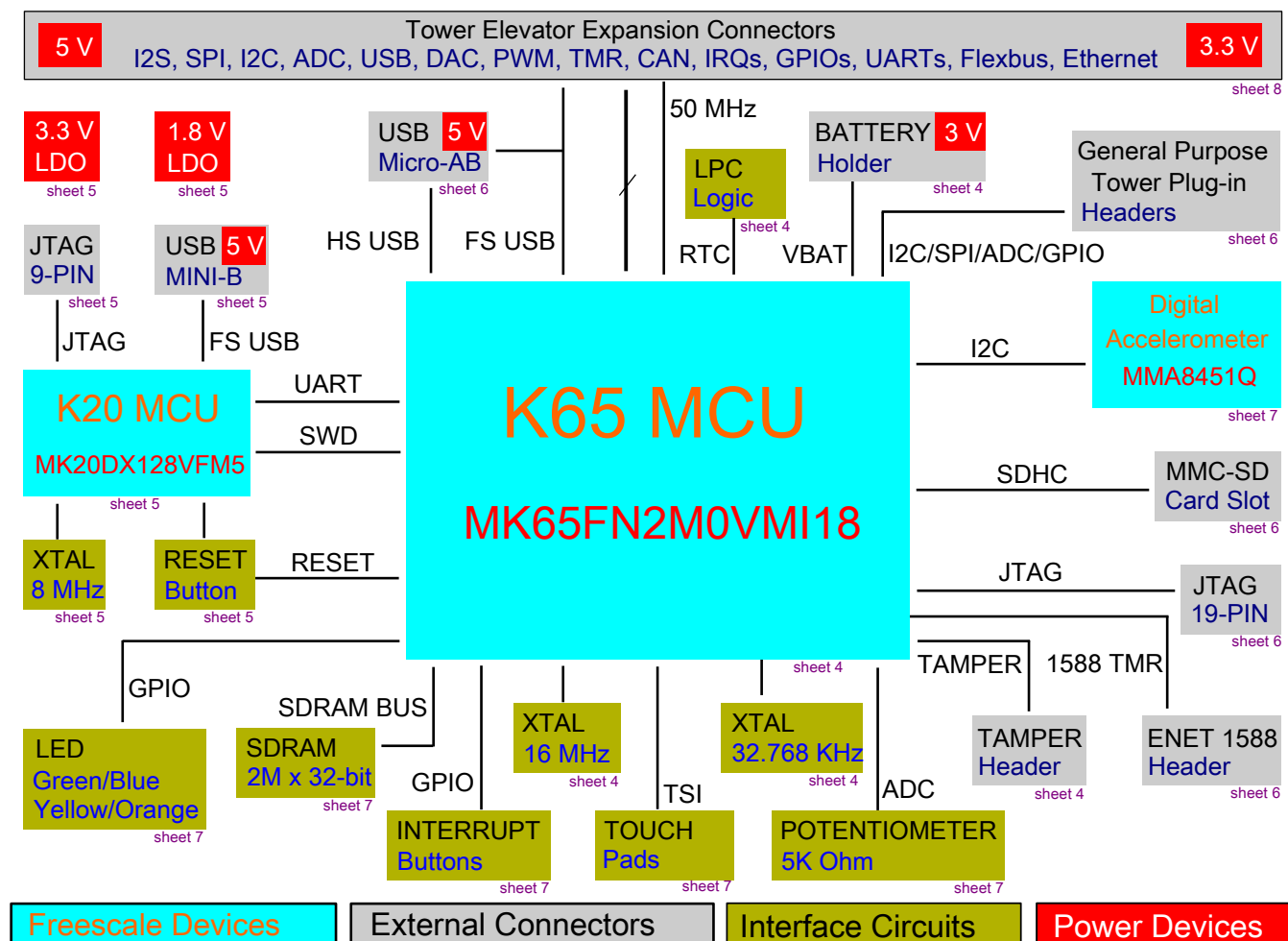


Figure 3. TWR-K65F180M Block Diagram

#### 3.1 K65F180M microcontroller

The TWR-K65F180M module features the K65FN2M0VMI18. The K65 microcontroller family is part of the Kinetis portfolio of devices built around an ARM Cortex-M4F core. Refer to the *K65 Family Reference Manual* (document [K65P169M180SF5RMV2](#)) for comprehensive information on the K65FN2M0VMI18 device. The key features of K65FN2M0VMI18 are as follows.



**Table 1. K65FN2M0VM18 key features**

Feature	Description
Performance	<ul style="list-style-type: none"> <li>Up to 180 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit</li> </ul>
Memory and memory expansion	<ul style="list-style-type: none"> <li>2 MB program flash memory and 256 KB RAM</li> <li>FlexBus external bus interface and SDRAM controller</li> </ul>
Analog modules	<ul style="list-style-type: none"> <li>Two 16-bit SAR ADCs and two 12-bit DACs</li> <li>Four analog comparators (CMP) containing a 6-bit DAC and programmable reference input</li> <li>Voltage reference 1.2 V</li> </ul>
Communication interfaces	<ul style="list-style-type: none"> <li>Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability</li> <li>USB high-, full-, and low-speed On-the-Go with on-chip high speed transceiver</li> <li>USB full-, low-speed OTG with on-chip transceiver</li> <li>Two CAN, three SPI and four I<sup>2</sup>C modules</li> <li>One low power UART and five standard UARTs</li> <li>Secure Digital Host Controller (SDHC)</li> <li>I2S module</li> </ul>
Security	<ul style="list-style-type: none"> <li>Tamper detect and secure storage</li> <li>Hardware random-number generator</li> <li>Supports DES, AES, SHA accelerator (CAU)</li> <li>Multiple levels of embedded flash security</li> </ul>
Timers	<ul style="list-style-type: none"> <li>Four periodic interrupt timers</li> <li>16-bit low-power timer</li> <li>Two 16-bit low-power timer PWM modules</li> <li>Two 8-channel motor control / general purpose / PWM timers</li> <li>Two 2-channel quad decoder / general purpose timers</li> <li>Real-time clock</li> </ul>
Human machine interface	<ul style="list-style-type: none"> <li>Low-power hardware touch sensor interface (TSI)</li> <li>General-purpose input / output</li> </ul>

## 3.2 Clocking

The Kinetis microcontrollers start up from an internal digitally controlled oscillator (DCO). The software can enable one or two external oscillators if required. The external oscillator for the Multipurpose Clock Generator (MCG) module can range from 32.768 kHz up to a 32 MHz crystal or ceramic resonator. The external oscillator for the Real-Time Clock (RTC) module accepts a 32.768 kHz crystal.

Two crystals are provided on-board for clocking the K65F180M device: a 16 MHz crystal as the main oscillator to clock the MCG module and a 32.768 kHz crystal for clocking the RTC module.

### NOTE

The on-chip HS USB PHY requires a 12, 16, or 24 MHz crystal with the main oscillator on EXTAL0 and XTAL0 pins.

## 3.3 System power

In standalone operation, the main power source for the TWR-K65F180M is derived from the 5.0 V input from either the USB mini-B connector, J7, or the debugger header, J18, when a shunt is placed on jumper J21. An on-board low-dropout regulator provides either 3.3 V or 1.8 V supply from the 5.0 V

input voltage based on the configuration of jumper J9. See sheet 5 of the *TWR-K65F180M Schematics* (document [TWR-K65F180M-SCH](#)) for further details.

When installed into a Tower System, the TWR-K65F180M can be powered from either an on-board power source or from another power source in the assembled Tower System. If both the on-board and off-board power sources are available, the TWR-K65F180M will default to the off-board power source.

The 3.3 V or 1.8 V power supplied to the MCU is routed through a jumper, J1. The jumper shunt can be removed to allow the following:

- 1) Alternate MCU supply voltages to be injected.
- 2) Measurement of power consumed by the MCU.

### 3.4 Tamper module (Dryice) and Real-Time Clock supply

The Dryice tamper detection module and the Real-Time Clock (RTC) module on the K65FN2M0VMI18 have two modes of operation: system power up and system power down. During system power down, the tamper detection module and the RTC are powered from the backup power supply (VBAT) and electrically isolated from the rest of the MCU. The TWR-K65F180M provides a battery receptacle for a coin cell battery that can be used as the VBAT supply. The receptacle uses standard 20 mm diameter 3 V lithium coin cell batteries.

### 3.5 Serial and Debug Adapter version 2 (OpenSDAv2)

OpenSDAv2 is a serial and debug adapter circuit which includes an open-source hardware design, an open-source bootloader, and debug interface software. It bridges serial and debug communications between a USB host and an embedded target processor as shown in figure 4. The hardware circuit is based on a Freescale Kinetis K20 family MCU with 128 KB of embedded flash and an integrated USB controller. OpenSDAv2 comes preloaded with the CMSIS-DAP bootloader—an open-source mass storage device (MSD) bootloader—and the CMSIS-DAP interface firmware (also known as the mbed interface), which provides an MSD flash programming interface, a virtual serial port interface, and a CMSIS-DAP debug protocol interface. For more information on the OpenSDAv2 software, see [mbed.org](http://mbed.org) and <https://github.com/mbedmicro/CMSIS-DAP>.

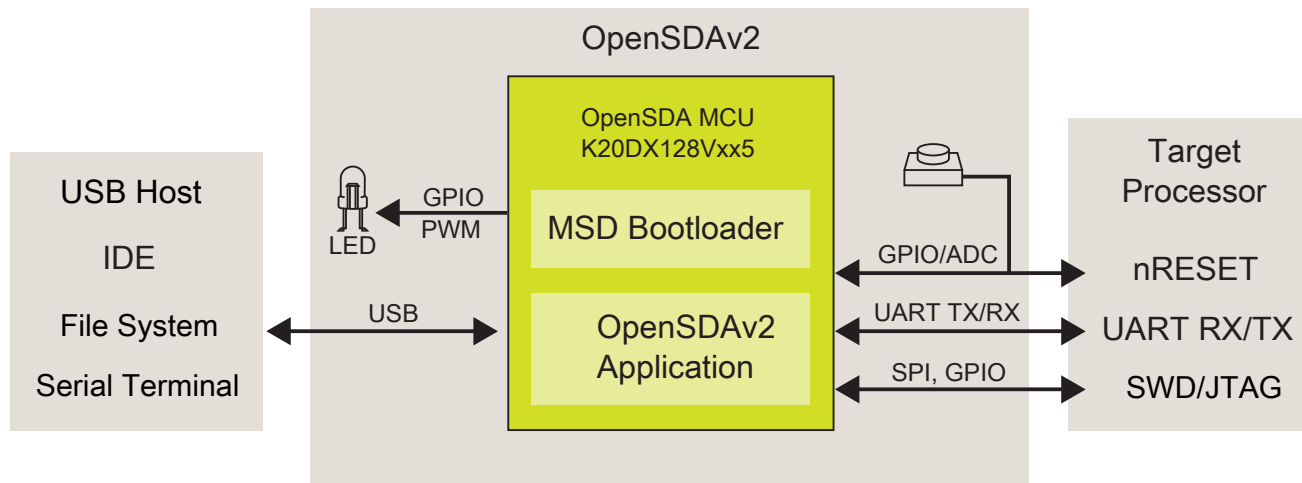


Figure 4. OpenSDAv2 high-level block diagram

OpenSDAv2 is managed by a Kinetis K20 MCU built on the ARM Cortex-M4 core. The OpenSDAv2 circuit includes a status LED (D3) and a pushbutton (SW1). The pushbutton asserts the Reset signal to the K65 target MCU. It can also be used to place the OpenSDAv2 circuit into bootloader mode. SPI and GPIO signals provide an interface to either the SWD debug port or the K20. Additionally, signal connections are available to implement a UART serial channel. The OpenSDAv2 circuit receives power when the USB connector J7 is plugged into a USB host.

### 3.6 Cortex Debug connector

The Cortex Debug connector is a 20-pin (0.05 inch) connector providing access to the SWD, JTAG, and EzPort signals available on the K65 device. The K65 pin connections to the debug connector (J18) are shown in this table.

**Table 2. Cortex Debug connector pinout**

Pin	Function	TWR-K65F180M connection
1	VTref	3.3 V MCU supply (MCU_PWR)
2	TMS/SWDIO	PTA3/UART0_RTS_b/FTM0_CH0/JTAG_MS/SWD_DIO
3	GND	GND
4	TCK/SWCLK	PTA0/UART0_CTS_b/FTM0_CH5/JTAG_CLK/SWD_CLK/EZP_CLK
5	GND	GND
6	TDO/SWO	PTA2/UART0_TX/FTM0_CH7/JTAG_DO/TRACE_SWO/EZP_DO
7	Key	–
8	TDI	PTA1/UART0_TX/FTM0_CH6/JTAG_DI/EZP_DI
9	GNDDETECT	PTA4/FTM0_CH1/MS/NMI_b/EZP_CS_b
10	nReset	RESET_b
11	Target Power	5 V supply (via J21)
12	TRACECLK	PTE0/SPI1_PCS1/UART1_TX/SDHC0_D1/TRACE_CLKOUT
13	Target Power	5 V supply (via J21)
14	TRACEDATA[0]	PTE4/SPI1_PCS0/UART3_TX/SDHC0_D3/TRACE_D0
15	GND	GND
16	TRACEDATA[1]	PTE3/SPI1_SIN/UART1_RTS_b/SDHC0_CMD/TRACE_D1
17	GND	GND
18	TRACEDATA[2]	PTE2/SPI1_SCK/UART1_CTS_b/SDHC0_DCLK/TRACE_D2
19	GND	GND
20	TRACEDATA[3]	PTE1/SPI1_SOUT/UART1_RX/SDHC0_D0/TRACE_D3

#### NOTE

To avoid conflict with RMI signals, trace signals are routed to the PTE port with unpopulated 0 Ohm resistors to avoid signal conflicts with SDHC.

### 3.7 External Bus Interface – FlexBus

The K65 device features a multi-function external bus interface called the FlexBus interface controller. This is capable of interfacing with slave-only devices. The FlexBus interface is not used directly on the TWR-K65F180M. Instead, a subset of the FlexBus is connected to the Primary Connector so that the external bus can access devices on Tower peripheral modules. See [Table 6](#) “**Error! Reference source not found.**” and sheet 8 of the *TWR-K65F180M Schematics* (document [TWR-K65F180M-SCH](#)) for more details.

### 3.8 SDRAM

The TWR-K65F180M board contains 64 Mb SDRAM (32-bit width) which is connected to the K65 SDRAM controller. The SDRAM signals are multiplexed with Flexbus signals. See the *K65 Family Reference Manual* (document [K65P169M180SF5RMV2](#)) “Flexbus signal multiplexing” section and “SDRAM SDR signal multiplexing” section on how to use the Flexbus and SDRAM in multiplexed mode.

### 3.9 Accelerometer

An MMA8451Q digital accelerometer is connected to the K65 MCU through an I<sup>2</sup>C interface (I<sup>2</sup>C0) and two GPIO/IRQ signals (PTE27 and PTE28). See [Table 5](#) “**Error! Reference source not found.**” for connection details.

When using Kinetis Bootloader to update K65 MCU flash firmware with an I<sup>2</sup>C interface, remove the jumpers on J35 so I<sup>2</sup>C communication is not affected by the accelerometer connection. For information on Kinetis Bootloader, see [freescale.com/kboot](http://freescale.com/kboot).

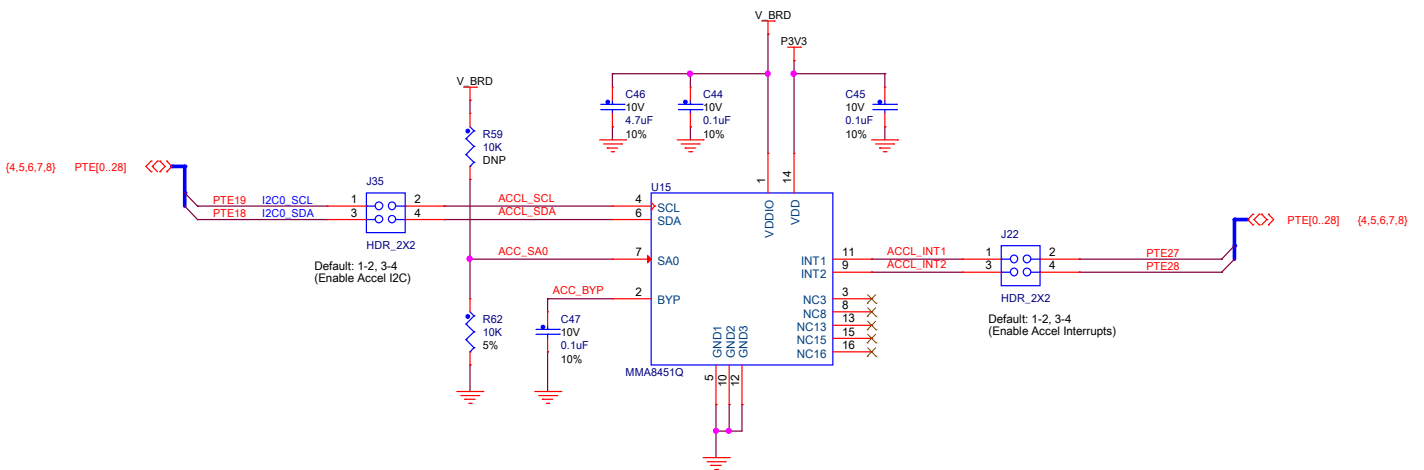


Figure 5. Accelerometer connection

### 3.10 Potentiometer, Pushbuttons, LEDs

The TWR-K65F180M features:

- A potentiometer connected to an ADC input signal (ADC1\_SE16/ADC0\_SE22)
- Two pushbutton switches (SW2 and SW3 connected to PTA4 and PTA10)
- User controllable LEDs connected to GPIO signals
  - Yellow LED D6 connected to PTB4
  - Orange LED D7 connected to PTB5
  - LED D8 connected to PTA28
  - LED D9 connected to PTA29



### 3.11 General Purpose Tower Plug-in (TWRPI) socket

The TWR-K65F180M features two sockets (J11 and J12) that can accept a variety of different Tower Plug-in modules featuring sensors, RF transceivers, and more. The General Purpose TWRPI socket provides access to I<sup>2</sup>C, SPI, IRQs, GPIOs, timers, analog conversion signals, TWRPI ID signals, reset, and voltage supplies. The pinout for the TWRPI Socket is defined in the following table.

**Table 3. TWRPI socket pin description**

Left-side 2x10 Connector		Right-side 2x10 Connector	
Pin	Description	Pin	Description
1	5V VCC	1	GND
2	3.3 V VCC	2	GND
3	GND	3	I <sup>2</sup> C: SCL
4	3.3 V VDDA	4	I <sup>2</sup> C: SDA
5	VSS (Analog GND)	5	GND
6	VSS (Analog GND)	6	GND
7	VSS (Analog GND)	7	GND
8	ADC: Analog 0	8	GND
9	ADC: Analog 1	9	SPI: MISO
10	VSS (Analog GND)	10	SPI: MOSI
11	VSS (Analog GND)	11	SPI: SS
12	ADC: Analog 2	12	SPI: CLK
13	VSS (Analog GND)	13	GND
14	VSS (Analog GND)	14	GND
15	GND	15	GPIO: GPIO0/IRQ
16	GND	16	GPIO: GPIO1/IRQ
17	ADC: TWRPI ID 0	17	GPIO: GPIO2/UART0_RX
18	ADC: TWRPI ID 1	18	GPIO: GPIO3/ UART0_TX
19	GND	19	GPIO: GPIO4/ UART0_CTS
20	Reset	20	GPIO: GPIO5/ UART0_RTS

### 3.12 Touch interface

The touch-sensing input (TSI) module of the Kinetis microcontrollers provides capacitive touch-sensing detection with high sensitivity and enhanced robustness. Each TSI pin implements the capacitive measurement of an electrode. There are two individual electrodes on-board the TWR-K65F180M that simulates pushbuttons.

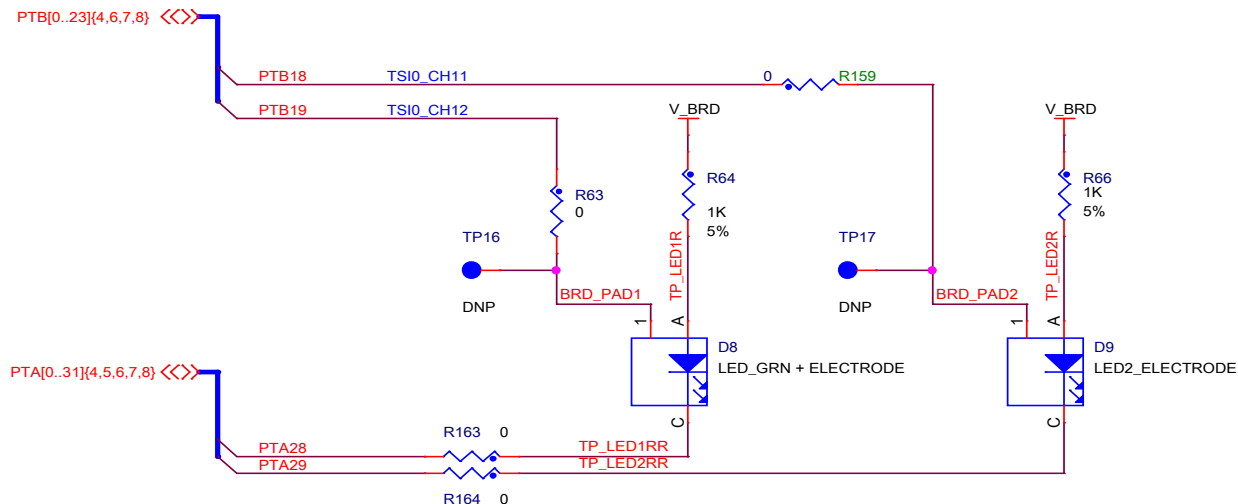


Figure 6. Touch pad circuitry

### 3.13 USB interface

The K65FN2M0VM118 features a high-, full-, and low-speed USB controller with on-chip HS USB PHY, and a full-, low-speed USB controller with on-chip USB PHY. The TWR-K65F180M board enables the USB to be host or device in standalone mode or with connection to a TWR-SER1 board in a complete tower kit. FS USB controller DP/DM signals can be selectively routed to the MicroUSB connector J15 or the MiniUSB connector J14 on a TWR-SER1 board by changing the 0 ohm resistor to connect either to A or B as shown in the following schematic. This is to help reduce on-board signal stub. The HS USB controller signal DP/DM signals can only be connected to on-board MicroUSB connector J15.

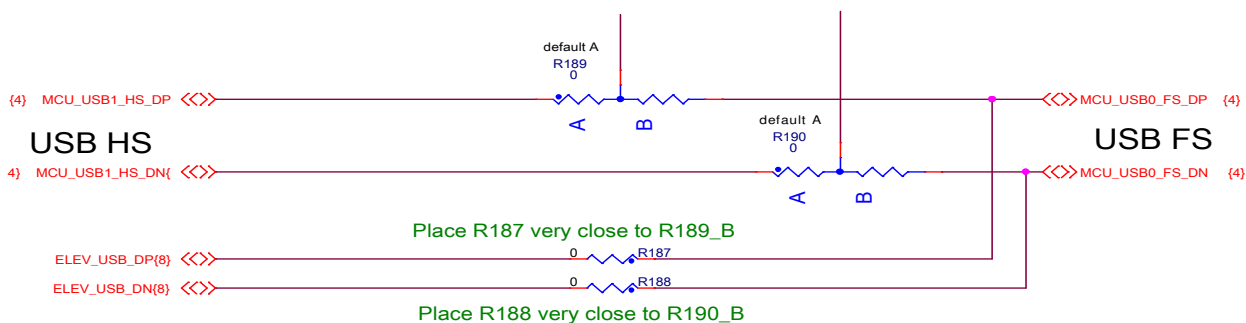


Figure 7. USB signal routing

### 3.14 Secure digital card slot

A Micro SD card slot is available on the TWR-K65F180M connected to the SD host controller (SDHC) signals of the MCU. This slot will accept standard format SD memory cards. See [Table 5](#) “**Error! Reference source not found.**” for connection details.

### 3.15 Ethernet and 1588

The K65FN2M0VMI18 features a 10/100 Mbps Ethernet MAC with MII and RMII interfaces. The TWR-K65F180M routes RMII interface signals from the K65 MCU to the primary elevator connector which enables a connection to an external Ethernet PHY that can be found on some Tower peripheral modules.

The reason that only RMII instead of MII interface signals are routed out is because there is multiplexing of the Flexbus function on some of the MII signals. Routing only the RMII signals enables Ethernet and Flexbus functions to work at the same time.

When the K65 Ethernet MAC is operating in RMII mode, synchronization of the MCU clock and the 50 MHz RMII transfer clock is important. The MCU input clock must remain in phase with the 50 MHz clock supplied to the external PHY. According to the K65 reference manual, the RMII clock can be selected between EXTAL and ENET\_1588\_CLKIN (PTE26) and because the system oscillator is already connected with 16 MHz to allow HS USB PHY to function, the RMII clock is coming from PTE26 and this signal is connected to CLKIN0 (B24) of the primary elevator.

## 4 Jumper table

There are several jumpers provided for isolation, configuration, and feature selection. See the following table for details.

**Table 4. TWR-K65F180M jumper table**

Jumper	Option	Setting	Description	Default setting
J1	MCU power connection	On	Connect V_SUPPLY and V_BRD with MCU_PWR	On
		Off	Disconnect V_SUPPLY and V_BRD with MCU_PWR	
J2	VDD and VDDA connection	On	Connect VDD and VDDA	On
		Off	Disconnect VDD and VDDA	
J3	VBAT power selection	1-2	Connect VBAT to on-board 3.3 V supply from V_SUPPLY	1-2
		2-3	Connect VBAT to the higher voltage between on-board 3.3 V supply or coin cell supply	
J4	Tamper signal header	2-3	Tamper signal header	2-3
J6	RESET button connection	1-2	When powering the OPENSDA MCU, bootloader mode can be selected	1-2
		2-3	When OPENSDA MCU is not powered, RESET button can be used	
J8	5V power connection	On	Connect P5V_TRG_USB to input of on-board 3.3 V regulator	On
		Off	Disconnect P5V_TRG_USB to on-board 3.3 V regulator	
J9	Board power selection	1-2	V_SUPPLY comes from OPENSDA MCU (K20) USB regulator	5-6
		3-4	V_SUPPLY comes from on-board 1.8 V regulator	
		5-6	V_SUPPLY comes from on-board 3.3 V regulator	
		7-8	V_SUPPLY comes from K65 USB regulator	
J10	TWRPI power selection	On	Connect V_BRD to TWRPI connector power	On
		OFF	Disconnect V_BRD to TWRPI connector power	

**Table 4. TWR-K65F180M jumper table (continued)**

Jumper	Option	Setting	Description	Default setting
J13	USB power enable connection	On	Connect PTD8 to USB power enable for MIC2005	On
		OFF	Disconnect PTD8 to USB power enable for MIC2005	
J14	USB over-current flag connection	On	Connect PTD9 to USB over-current flag for MIC2005	On
		OFF	Disconnect PTD9 to USB over-current flag for MIC2005	
J16	USB ID connection	1-2	Connect PTD15 to USB ID pin on MicroUSB connector J15	1-2
		2-3	Connect PTE10 to USB ID pin on MicroUSB connector J15	
J17	Pulldown connection on CD/DAT3 for MicroSD slot	On	Disconnect pull down resistor on CD/DAT3 pin on MicroSD slot	Off
		Off	Connect pull down resistor on CD/DAT3 pin on MicroSD slot	
J20	MCU reset connection on JTAG connector	On	Connect MCU reset on pin10 of JTAG connector J18	On
		Off	Disconnect MCU reset on pin10 of JTAG connector J18	
J21	JTAG Power Connection	On	Connect on-board 5V supply to JTAG port (supports powering board from external JTAG probe)	Off
		Off	Disconnect on-board 5V supply from JTAG port	
J22	Accelerometer INT connection	1-2	Connects INT1 from MMA8451 to PTE27	1-2 3-4
		3-4	Connects INT2 from MMA8451 to PTE28	
J23	K65 VREGIN selection	1-2	VREG_IN0 connected with ONBOARD_USB_VBUS	1-2 3-4
		1-3	VREG_IN1 connected with ONBOARD_USB_VBUS	
		2-4	VREG_IN0 connected with ELEV_USB_VBUS	
		3-4	VREG_IN1 connected with ELEV_USB_VBUS	
J24	Potentiometer connection	On	Connect potentiometer to ADC1_SE16	On
		Off	Disconnect potentiometer to ADC1_SE16	
J27	/RSTOUT connection	1-2	MCU reset signal connected to /RSTOUT (A63) on primary elevator	2-3
		2-3	PTD10 connected to /RSTOUT (A63) on primary elevator	
J30	SDRAM power connection	On	Connect V_BRD to SDRAM chip	On
		Off	Disconnect V_BRD to SDRAM chip	
J32	SWD clock disconnection	On	Connect SWD_CLK from OPENSDA circuit to K65 MCU to allow debugging using OPENSDA	On
		OFF	Disconnect SWD_CLK from OPENSDA circuit to K65 MCU to allow J-Link or U-Link debug	
J33	UART2 RX connection	1-2	Connect UART2_RX to elevator	2-3
		2-3	Connect UART2_RX to OPENSDA UART RX	
J34	UART2 TX connection	1-2	Connect UART2_TX to elevator	2-3
		2-3	Connect UART2_TX to OPENSDA UART TX	
J35	I <sup>2</sup> C connection with accelerometer	1-2	Connect I <sup>2</sup> C0_SCL with accelerometer SCL	1-2 3-4
		3-4	Connect I <sup>2</sup> C0_SDA with accelerometer SDA	
J36	USB 5 V power connection	1-2	Connect MiniUSB connector (J7) VBUS with U12 pin 1	2-3
		2-3	Connect P5V_ELEV with U12 pin 1	

## 5 Input/output connectors and pin usage table

The table below provides details on which K65F180M pins are used to communicate with the TWR-K65F180M sensors, LEDs, switches, and other I/O interfaces.

### NOTE

Some port pins are used in multiple interfaces on-board and many are potentially connected to off-board resources via the primary and secondary Connectors. You must take care to avoid attempted simultaneous usage of mutually exclusive features.

**Table 5. I/O Connectors and Pin Usage Table**

Feature	Connection	Port Pin	Pin Function
OPENSDA USB-to-serial bridge	OPENSDA RX data	PTE17	UART2_RX
	OPENSDA TX data	PTE16	UART2_TX
SD Card Slot	SD clock	PTE2	SDHC0_DCLK
	SD Command	PTE3	SDHC0_CMD
	SD Data0	PTE1	SDHC0_D0
	SD Data1	PTE0	SDHC0_D1
	SD Data2	PTE5	SDHC0_D2
	SD Data3	PTE4	SDHC0_D3
	SD Card Detect	PTA9	PTA9
Pushbuttons	SW2 (NMI)	PTA4	PTA4
	SW3 (LLWU)	PTA10	PTA10
	SW1 (RESET)	RESET_b	RESET_b
Touch Pads	Touch	PTB18	TSI0_CH11
	Touch	PTB19	TSI0_CH12
LEDs	D2 / Orange LED	—	RESET_b
	D5 / YEL/GRN LED	—	Power on
	D6 / Yellow LED	PTB4	Yellow LED
	D7 / Orange LED	PTB5	Orange LED
	D8	PTA28	D8 Electrode LED
	D9	PTA29	D9 Electrode LED
Potentiometer	Potentiometer (R67)	—	ADC1_SE16/ADC0_SE22
Accelerometer	I <sup>2</sup> C SDA	PTE19	I <sup>2</sup> C0_SDA
	I <sup>2</sup> C SCL	PTE18	I <sup>2</sup> C0_SCL
	IRQ1	PTE27	PTE27
	IRQ2	PTE28	PTE28



**Table 5. I/O Connectors and Pin Usage Table (continued)**

High Speed USB	USB VBUS Enable	PTD8	PTD8
	USB Over-current flag	PTD9	PTD9
	USB ID	PTD15 or PTE10	USB1_ID
ENET 1588	ENET 1588 TMR0	PTB2	ENET0_1588_TMR0
	ENET 1588 TMR1	PTB3	ENET0_1588_TMR1
	ENET 1588 TMR2	PTB4	ENET0_1588_TMR2
	ENET 1588 TMR3	PTB5	ENET0_1588_TMR3
RTC	RTC bypass	PTA11	PTA11
General Purpose TWRPI Socket	TWRPI AN0 (J11 Pin 8)	—	ADC0_SE16 / ADC0_SE21
	TWRPI AN1 (J11 Pin 9)	—	ADC1_DP0 / ADC0_DP3
	TWRPI AN2 (J11 Pin 12)	—	ADC1_DM0 / ADC0_DM3
	TWRPI ID0 (J7 Pin 17)	—	ADC0_DP0 / ADC1_DP3
	TWRPI ID1 (J7 Pin 18)	—	ADC0_DM0 / ADC1_DM3
	TWRPI I <sup>2</sup> C SCL (J12 Pin 3)	PTE19	I <sup>2</sup> C0_SCL
	TWRPI I <sup>2</sup> C SDA (J12 Pin 4)	PTE18	I <sup>2</sup> C0_SDA
	TWRPI SPI MISO (J12 Pin 9)	PTD14	SPI2_SIN
	TWRPI SPI MOSI (J12 Pin 10)	PTD13	SPI2_SOUT
	TWRPI SPI SS (J12 Pin 11)	PTD15	SPI2_PCS1
	TWRPI SPI CLK (J12 Pin 12)	PTD12	SPI2_SCK
	TWRPI GPIO0 (J12 Pin 15)	PTC14	PTC14
	TWRPI GPIO1 (J12 Pin 16)	PTC15	PTC15
	TWRPI GPIO2 (J12 Pin 17)	PTC16	PTC16
	TWRPI GPIO3 (J12 Pin 18)	PTC17	PTC17
	TWRPI GPIO4 (J12 Pin 19)	PTC18	PTC18
TWRPI GPIO5 (J12 Pin 20)	PTC19	PTC19	

## 6 Elevator connections

The TWR-K65F180M features two expansion card-edge connectors that interface to Elevator boards in a Tower System: the primary and secondary Elevator connectors. The pinout for the primary Elevator Connector is provided in this table. The values in **bold** are either power or ground.

**Table 6. TWR-K65F180M Primary Connector Pinout**

Pin #	Side B		Pin #	Side A	
	Name	Usage		Name	Usage
B1	<b>5 V</b>	<b>5.0 V Power</b>	A1	<b>5V</b>	<b>5.0 V Power</b>
B2	<b>GND</b>	<b>Ground</b>	A2	<b>GND</b>	<b>Ground</b>
B3	<b>3.3 V</b>	<b>3.3 V Power</b>	A3	<b>3.3 V</b>	<b>3.3 V Power</b>
B4	ELE_PS_SENSE	Elevator Power Sense	A4	<b>3.3 V</b>	<b>3.3 V Power</b>
B5	<b>GND</b>	<b>Ground</b>	A5	<b>GND</b>	<b>Ground</b>

**Table 6. TWR-K65F180M Primary Connector Pinout (continued)**

B6	<b>GND</b>	<b>Ground</b>	A6	<b>GND</b>	<b>Ground</b>
B7	SDHC_CLK / SPI1_CLK	PTE2	A7	SCL0	PTE19
B8	SDHC_D3 / SPI1_CS1_b	—	A8	SDA0	PTE18
B9	SDHC_D3 / SPI1_CS0_b	PTE4	A9	GPIO9 / CTS1	PTD1
B10	SDHC_CMD / SPI1_MOSI	PTE3	A10	GPIO8 / SDHC_D2	PTE5
B11	SDHC_D0 / SPI1_MISO	PTE1	A11	GPIO7 / SD_WP_DET	PTA9
B12	ETH_COL	—	A12	ETH_CRS	—
B13	ETH_RXER	PTA5	A13	ETH_MDC	PTA8
B14	ETH_TXCLK	—	A14	ETH_MDIO	PTA7
B15	ETH_TXEN	PTA15	A15	ETH_RXCLK	—
B16	ETH_TXER	—	A16	ETH_RXDV	PTA14
B17	ETH_TXD3	—	A17	ETH_RXD3	—
B18	ETH_TXD2	—	A18	ETH_RXD2	—
B19	ETH_TXD1	PTA17	A19	ETH_RXD1	PTA12
B20	ETH_TXD0	PTA16	A20	ETH_RXD0	PTA13
B21	GPIO1 / RTS1	PTD0	A21	I2S0_MCLK	PTE6
B22	GPIO2 / SDHC_D1	PTE0	A22	I2S0_DOUT_BCLK	PTE12
B23	GPIO3	PTD10	A23	I2S0_DOUT_FS	PTE11
B24	CLKIN0	PTE26	A24	I2S0_RXD0	PTE7
B25	CLKOUT1	PTC3	A25	I2S0_TXD0	PTE10
B26	<b>GND</b>	<b>Ground</b>	A26	<b>GND</b>	<b>Ground</b>
B27	AN7	PTA6	A27	AN3	ADC0_SE16
B28	AN6	PTC3	A28	AN2	ADC1_DP0
B29	AN5	PTE24	A29	AN1	ADC1_DM0
B30	AN4	PTE25	A30	AN0	ADC0_SE16
B31	<b>GND</b>	<b>Ground</b>	A31	<b>GND</b>	<b>Ground</b>
B32	DAC1	DAC1_OUT	A32	DAC0	DAC0_OUT
B33	TMR3	PTD6	A33	TMR1	PTB13
B34	TMR2	PTD7	A34	TMR0	PTB12
B35	GPIO4	PTA28	A35	GPIO6	PTA29
B36	<b>3.3 V</b>	<b>3.3 V Power</b>	A36	<b>3.3 V</b>	<b>3.3 V Power</b>
B37	PWM7	—	A37	PWM3	PTD3
B38	PWM6	—	A38	PWM2	PTD2
B39	PWM5	PTD5	A39	PWM1	PTD1
B40	PWM4	PTD4	A40	PWM0	PTD0
B41	CANRX0	PTA31	A41	RXD0	PTA1
B42	CANTX0	PTA30	A42	TXD0	PTA2
B43	1WIRE	—	A43	RXD1	ELEV_UART_RX
B44	SPI0_MISO	PTD14	A44	TXD1	ELEV_UART_TX
B45	SPI0_MOSI	PTD13	A45	VSS	VSSA
B46	SPI0_CS0_b	PTD11	A46	VDDA	VDDA
B47	SPI0_CS1_b	PTD15	A47	CAN1_RX	PTE25
B48	SPI0_CLK	PTD12	A48	CAN1_TX	PTE24
B49	<b>GND</b>	<b>Ground</b>	A49	<b>GND</b>	<b>Ground</b>
B50	SCL1	PTE19	A50	GPIO14	PTA24
B51	SDA1	PTE18	A51	GPIO15	PTA25
B52	GPIO5 / SPI0_HOLD/IO3	PTA10	A52	GPIO16	PTA26

**Table 6. TWR-K65F180M Primary Connector Pinout (continued)**

B53	USB0_DP_PDOWN	—	A53	GPIO17	PTA27
B54	USB0_DM_PDOWN	—	A54	USB0_DM	ELEV_USB_DN
B55	IRQ_H	PTC27	A55	USB0_DP	ELEV_USB_DP
B56	IRQ_G	PTC27	A56	USB0_ID	—
B57	IRQ_F	PTC11	A57	USB0_VBUS	ELEV_USB_VBUS
B58	IRQ_E	PTC11	A58	I2S0_DIN_BCLK	PTC9
B59	IRQ_D	PTC3	A59	I2S0_DIN_FS	PTC8
B60	IRQ_C	PTC3	A60	I2S0_RXD1	PTC8
B61	IRQ_B	PTC28	A61	I2S0_TXD1	PTC9
B62	IRQ_A	PTC28	A62	RSTIN_b	RESET_b
B63	EBI_ALE / EBI_CS1_b	PTD0	A63	RSTOUT_b	Either RESET_b or PTD10
B64	EBI_CS0_b	PTD1	A64	CLKOUT0	PTA6
B65	<b>GND</b>	<b>Ground</b>	A65	<b>GND</b>	<b>Ground</b>
B66	EBI_AD15	PTB18	A66	EBI_AD14	PTC0
B67	EBI_AD16	PTB17	A67	EBI_AD13	PTC1
B68	EBI_AD17	PTB16	A68	EBI_AD12	PTC2
B69	EBI_AD18	PTB11	A69	EBI_AD11	PTC4
B70	EBI_AD19	PTB10	A70	EBI_AD10	PTC5
B71	EBI_RW_b	PTC11	A71	EBI_AD9	PTC6
B72	EBI_OE_b	PTB19	A72	EBI_AD8	PTC7
B73	EBI_D7	PTB20	A73	EBI_AD7	PTC8
B74	EBI_D6	PTB21	A74	EBI_AD6	PTC9
B75	EBI_D5	PTB22	A75	EBI_AD5	PTC10
B76	EBI_D4	PTB23	A76	EBI_AD4	PTD2
B77	EBI_D3	PTC12	A77	EBI_AD3	PTD3
B78	EBI_D2	PTC13	A78	EBI_AD2	PTD4
B79	EBI_D1	PTC14	A79	EBI_AD1	PTD5
B80	EBI_D0	PTC15	A80	EBI_AD0	PTD6
B81	<b>GND</b>	<b>Ground</b>	A81	<b>GND</b>	<b>Ground</b>
B82	<b>3.3 V</b>	<b>3.3 V Power</b>	A82	<b>3.3 V</b>	<b>3.3 V Power</b>

## 7 References

The list below provides references for more information on the Kinetis family, Tower System and the MCU modules. These can be found in the documentation section of [freescale.com/TWR-K65F180M](http://freescale.com/TWR-K65F180M) or [freescale.com/kinetis](http://freescale.com/kinetis).

- *TWR-K65F180M Quick Start Guide* (document [TWR-K65F180M-QSG](#))
- *TWR-K65F180M Schematics* (document [TWR-K65F180M-SCH](#))
- *K65 Family Data Sheet* (document [K65P169M180SF5V2](#))
- *K65 Family Reference Manual* (document [K65P169M180SF5RMV2](#))
- *Kinetis Quick Reference User Guide* (document [KQRUG](#))

## 8 Revision history

Table 7. Revision history

Revision number	Date	Substantive changes
0	05/2015	Initial release

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