FAIRCHILD SEMICONDUCTOR™

March 1994
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74ABT2240
Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The ABT2240 is an inverting octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

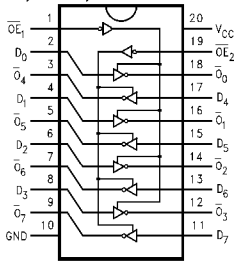
Ordering Code:

Order Number	Package Number	Package Description
74ABT2240CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT2240CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT2240CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT2240CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending letter suffix "X" to the ordering code.

Connection Diagram

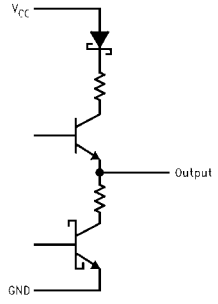
Pin Assignment for SOIC, SSOP, TSSOP and EIAJ



Pin Descriptions

Pin Names	Descriptions
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
D_0–D_7	Data Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Schematic of Each Output



Truth Table

$\overline{OE}_1$	I_{0-3}	$\overline{O}_{0-3}$	$\overline{OE}_2$	I_{4-7}	$\overline{O}_{4-7}$
H	X	Z	H	X	Z
L	H	L	L	H	L
L	L	H	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current (Across Comm Operating Range)	−300 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		2.5			V	Min	I_{OH} = −3 mA
			2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage				0.8	V	Min	I_{OL} = 15 mA
I_{IH}	Input HIGH Current				1	µA	Max	V_{IN} = 2.7V (Note 3)
					1			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−1	µA	Max	V_{IN} = 0.5V (Note 3)
					−1			V_{IN} = 0.0V
V_{ID}	Input Leakage Test					V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OZH}	Output Leakage Current				10	µA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}n$ = 2.0V
I_{OZL}	Output Leakage Current				−10	µA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}n$ = 2.0V
I_{OS}	Output Short-Circuit Current				−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	µA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	µA	Max	$\overline{OE}n$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			1.5	mA		V_I = V_{CC} − 2.1V
		Outputs 3-STATE			1.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs 3-STATE			50	µA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 3)	No Load			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}n$ = GND (Note 4) One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

Note 4: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

AC Electrical Characteristics

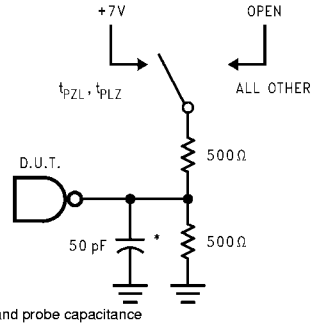
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation	1.0		4.9	1.0	4.9	
t_{PHL}	Delay Data to Outputs	1.5		5.3	1.5	5.3	ns
t_{PZH}	Output Enable	1.5		6.6	1.5	6.6	ns
t_{PZL}	Time	2.7		6.9	2.7	6.9	
t_{PHZ}	Output Disable	1.9		6.4	1.9	6.4	ns
t_{PLZ}	Time	1.9		6.4	1.9	6.4	

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

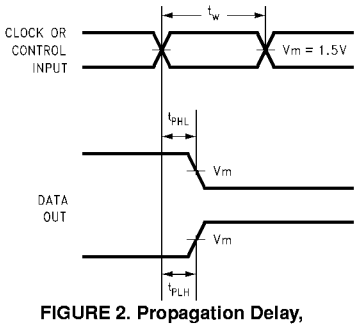


FIGURE 2. Propagation Delay, Pulse Width Waveforms

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

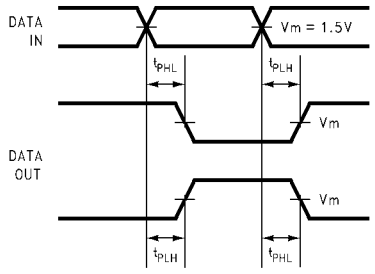


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

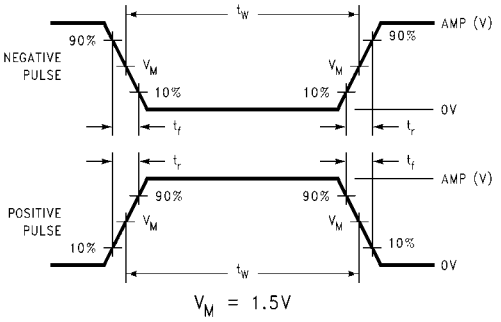


FIGURE 6. Test Input Signal Levels

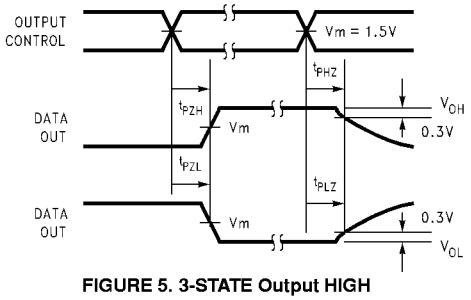


FIGURE 5. 3-STATE Output HIGH and LOW Enable and Disable Times

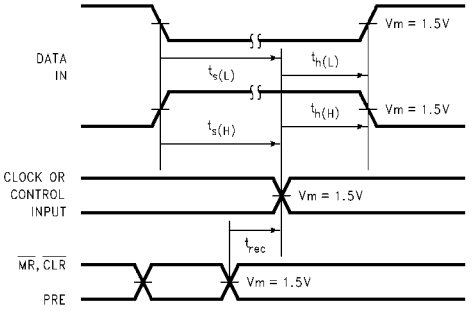
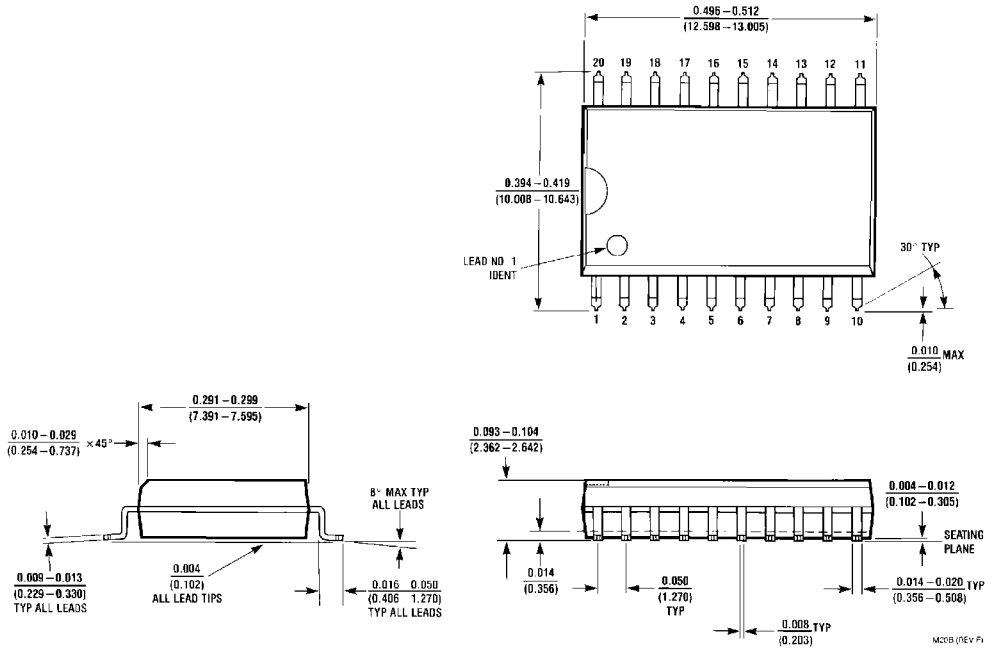
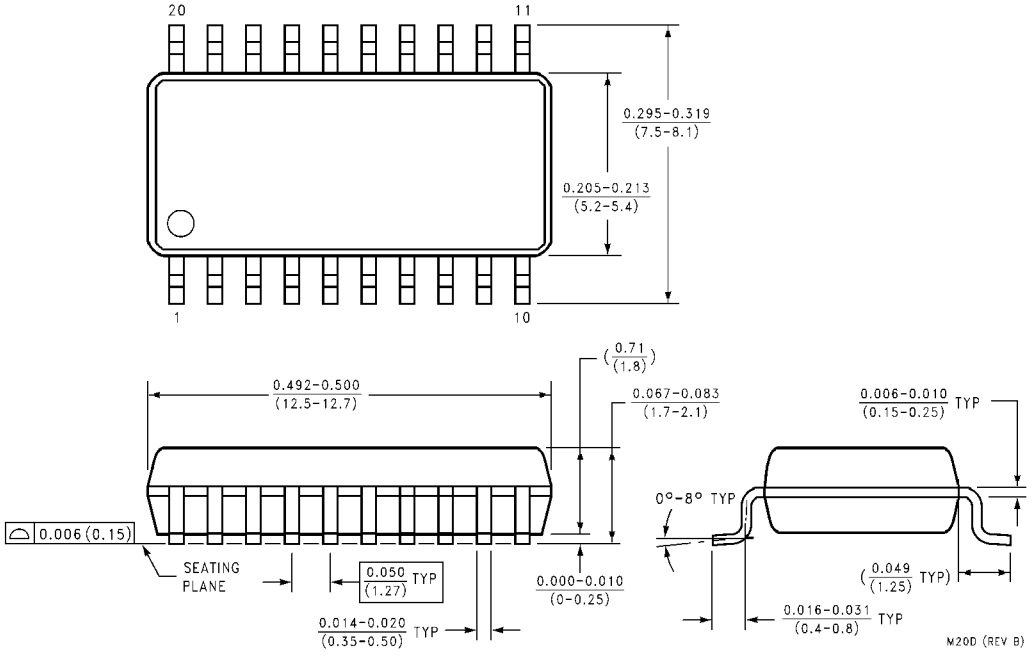


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

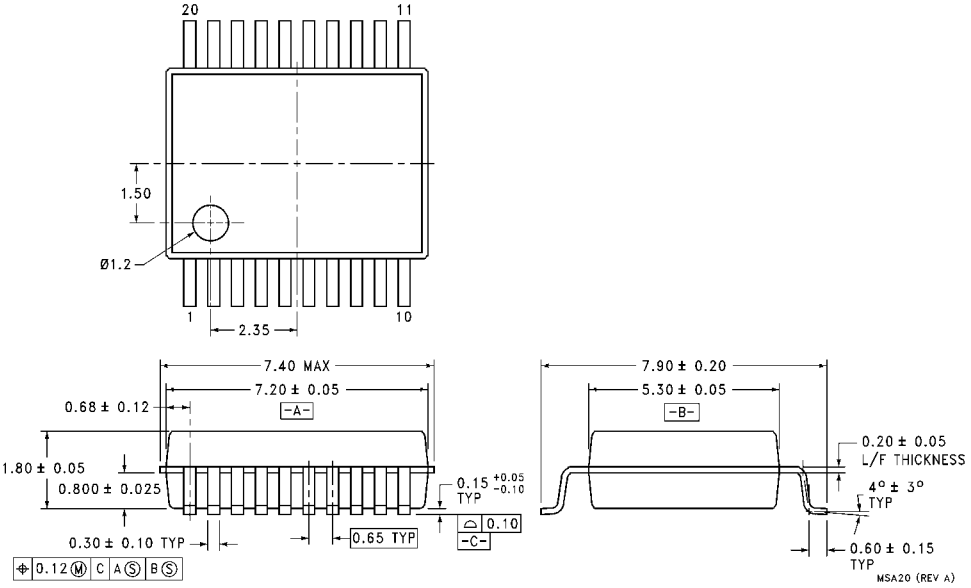


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B



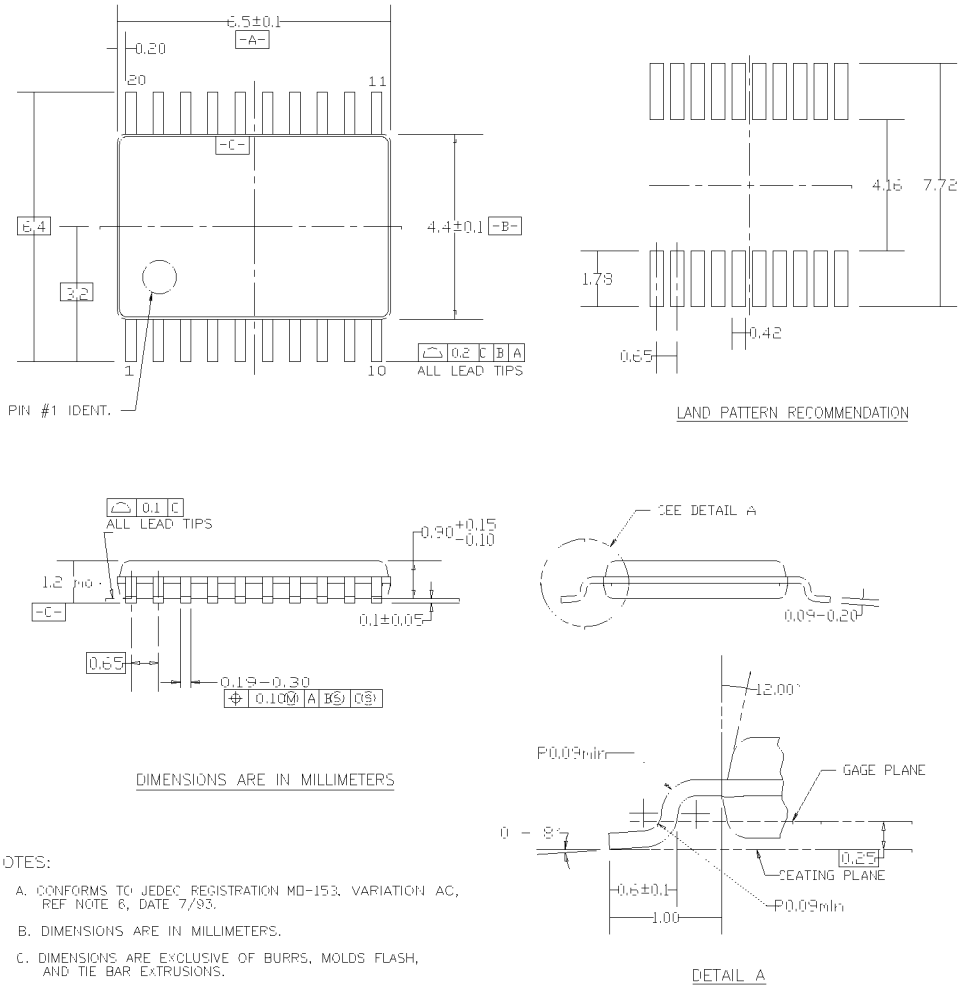
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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