

## General Description

The 87972I-147 is a low skew, LVCMOS/LVTTL Clock Generator and a member of the family of High Performance Clock Solutions from IDT. The 87972I-147 has three selectable inputs and provides 14 LVCMOS/LVTTL outputs.

The 87972I-147 is a highly flexible device. Using the crystal oscillator input, it can be used to generate clocks for a system. All of these clocks can be the same frequency or the device can be configured to generate up to three different frequencies among the three output banks. Using one of the single ended inputs, the 87972I-147 can be used as a zero delay buffer/multiplier/divider in clock distribution applications.

The three output banks and feedback output each have their own output dividers which allows the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. In addition, 2 outputs in Bank C (QC2, QC3) can be selected to be inverting or non-inverting. The output frequency range is 10MHz to 150MHz. Input frequency range is 6MHz to 150MHz.

The 87972I-147 also has a QSYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period of the faster clock prior to coincident rising edges of Bank A and Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

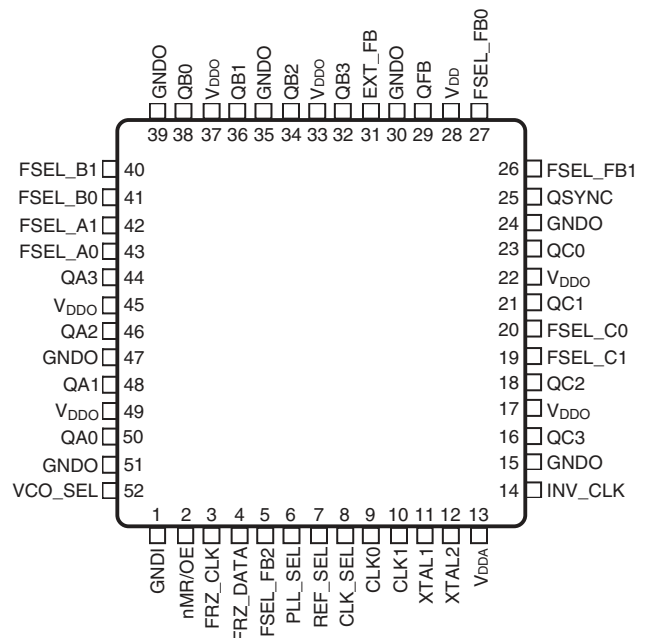
### Example Applications:

- System Clock generator:** Use a 16.66 MHz Crystal to generate eight 33.33MHz copies for PCI and four 100MHz copies for the CPU or PCI-X.
- Line Card Multiplier:** Multiply 19.44MHz from a back plane to 77.76MHz for the line Card ASICs and Serdes.
- Zero Delay buffer for Synchronous memory:** Fan out up to twelve 100MHz copies from a memory controller reference clock to the memory chips on a memory module with zero delay.

## Features

- Fully integrated PLL
- Fourteen LVCMOS/LVTTL outputs; (12)clocks, (1)feedback, (1)sync
- Selectable crystal oscillator interface or LVCMOS/LVTTL reference clock inputs
- CLK0, CLK1 can accept the following input levels: LVCMOS or LVTTL
- Output frequency range: 10MHz to 150MHz
- VCO range: 240MHz to 500MHz
- Output skew: 200ps (maximum)
- Cycle-to-cycle jitter, (all banks  $\pm$ 4): 55ps (maximum)
- Full 3.3V supply voltage
- 40°C to 85°C ambient operating temperature
- Compatible with PowerPC™ and Pentium™ Microprocessors
- Available in lead-free (RoHS 6) packages.

## Pin Assignment



87972I-147

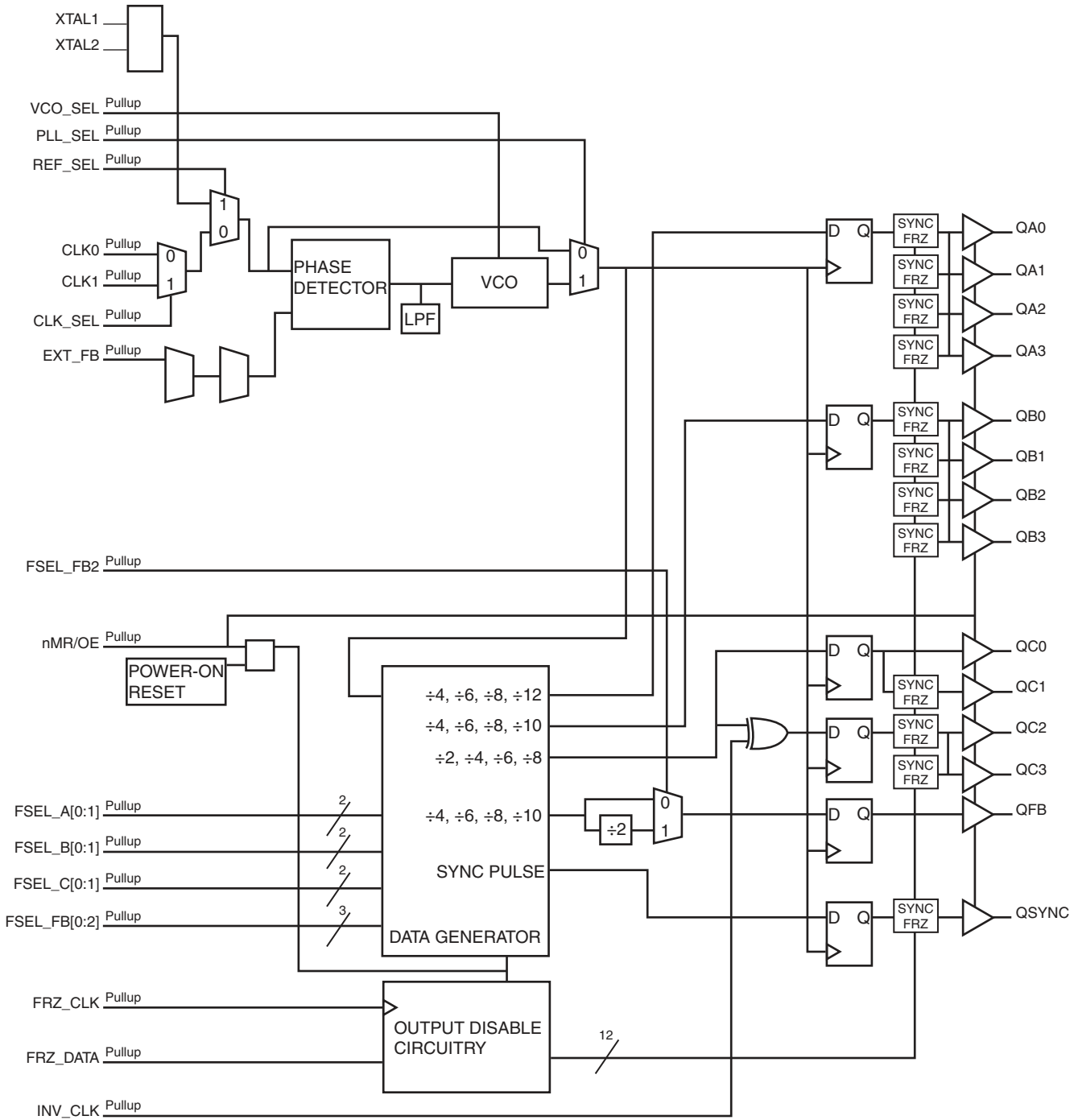
52-Lead LQFP

10mm x 10mm x 1.4mm package body

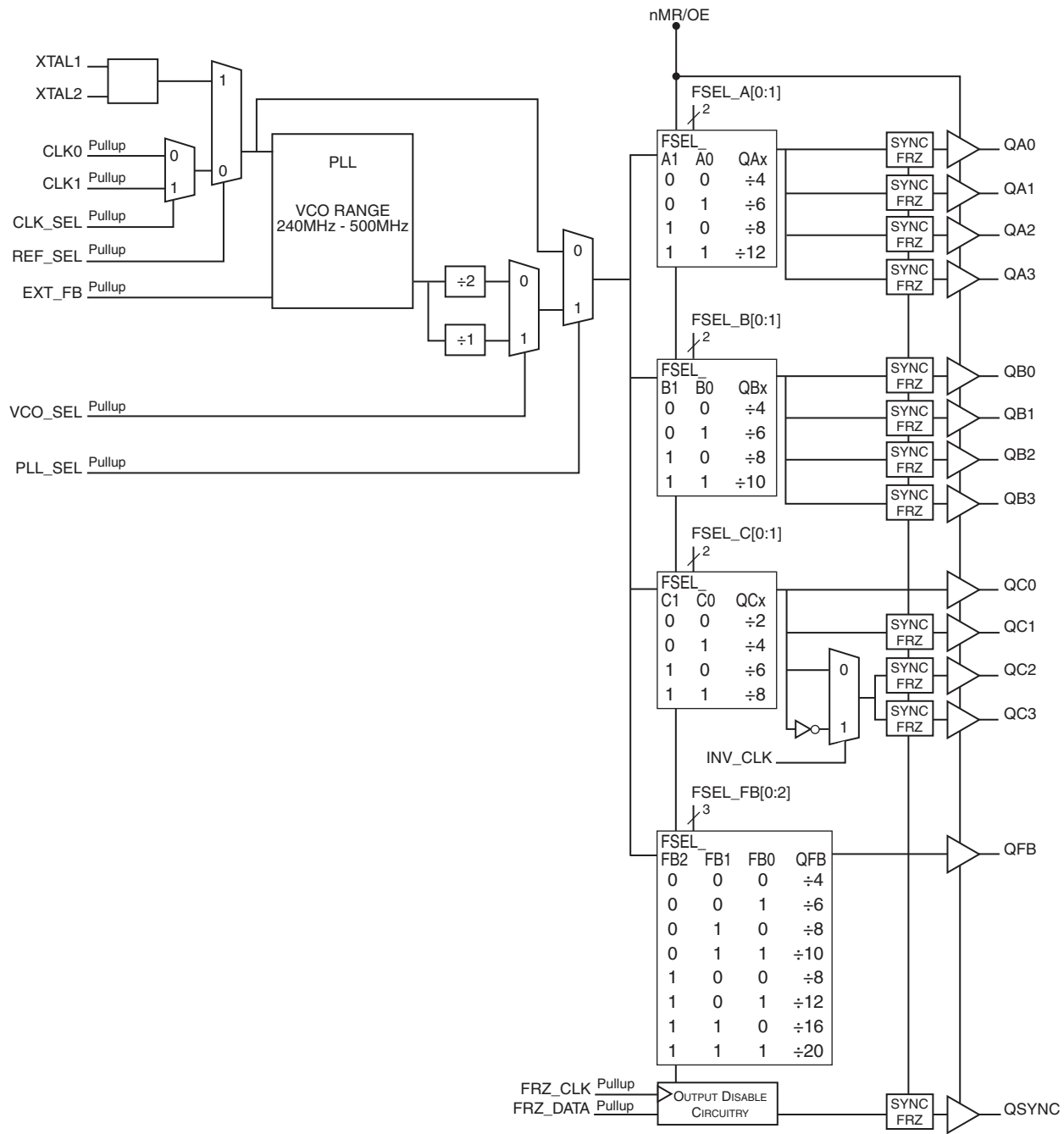
Y Package

Top View

# Block Diagram



## Simplified Block Diagram



**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	GNDI	Power		Power supply ground.
2	nMR/OE	Input	Pullup	Master reset and output enable. When HIGH, enables the outputs. When LOW, resets the outputs to Hi-Z and resets output divide circuitry. Enables and disables all outputs. LVCMOS / LVTTTL interface levels.
3	FRZ_CLK	Input	Pullup	Clock input for freeze circuitry. LVCMOS / LVTTTL interface levels.
4	FRZ_DATA	Input	Pullup	Configuration data input for freeze circuitry. LVCMOS / LVTTTL interface levels.
5, 26, 27	FSEL_FB2, FSEL_FB1, FSEL_FB0	Input	Pullup	Select pins control Feedback Divide value. LVCMOS / LVTTTL interface levels. See Table 3B.
6	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL and reference clocks. LVCMOS / LVTTTL interface levels.
7	REF_SEL	Input	Pullup	Selects between crystal and reference clock. When LOW, selects CLK0 or CLK1. When HIGH, selects crystal inputs. LVCMOS / LVTTTL interface levels.
8	CLK_SEL	Input	Pullup	Clock select input. When LOW, selects CLK0. When HIGH, selects CLK1. LVCMOS / LVTTTL interface levels.
9, 10	CLK0, CLK1	Input	Pullup	Single-ended reference clock inputs. LVCMOS/LVTTTL interface levels.
11, 12	XTAL_1, XTAL_2	Input		Crystal oscillator interface. XTAL_1 is the input. XTAL_2 is the output.
13	V <sub>DDA</sub>	Power		Analog supply pin.
14	INV_CLK	Input	Pullup	Inverted clock select for QC2 and QC3 outputs. LVCMOS / LVTTTL interface levels.
15, 24, 30, 35, 39, 47, 51	GND0	Power		Power supply ground.
16, 18, 21, 23	QC3, QC2, QC1, QC0	Output		Single-ended Bank C clock outputs. LVCMOS/ LVTTTL interface levels.
17, 22, 33, 37, 45, 49	V <sub>DDO</sub>	Power		Output power supply pins.
19, 20	FSEL_C1, FSEL_C0	Input	Pullup	Select pins for Bank C outputs. LVCMOS / LVTTTL interface levels. See Table 3A.
25	QYSNC	Output		Synchronization output for Bank A and Bank C. Refer to Figure 1, Timing Diagrams. LVCMOS / LVTTTL interface levels.
28	V <sub>DD</sub>	Power		Power supply pin.
29	QFB	Output		Single-ended feedback clock output. LVCMOS / LVTTTL interface levels.
31	EXT_FB	Input	Pullup	External feedback. LVCMOS / LVTTTL interface levels.
32, 34, 36, 38	QB3, QB2, QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/ LVTTTL interface levels.
40, 41	FSEL_B1, FSEL_B0	Input	Pullup	Select pins for Bank B outputs. LVCMOS / LVTTTL interface levels. See Table 3A.
42, 43	FSEL_A1, FSEL_A0	Input	Pullup	Select pins for Bank A outputs. LVCMOS / LVTTTL interface levels. See Table 3A.
44, 46, 48, 50	QA3, QA2, QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS/ LVTTTL interface levels.
52	VCO_SEL	Input	Pullup	Selects VCO. When HIGH, selects VCO ÷ 1. When LOW, selects VCO ÷ 2. LVCMOS / LVTTTL interface levels.

NOTE: Pullup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

## Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DD</sub> , V <sub>DDA</sub> , V <sub>DDO</sub> = 3.465V			18	pF
R <sub>OUT</sub>	Output Impedance		5	7	12	Ω

## Function Tables

### Table 3A. Output Bank Configuration Select Function Table

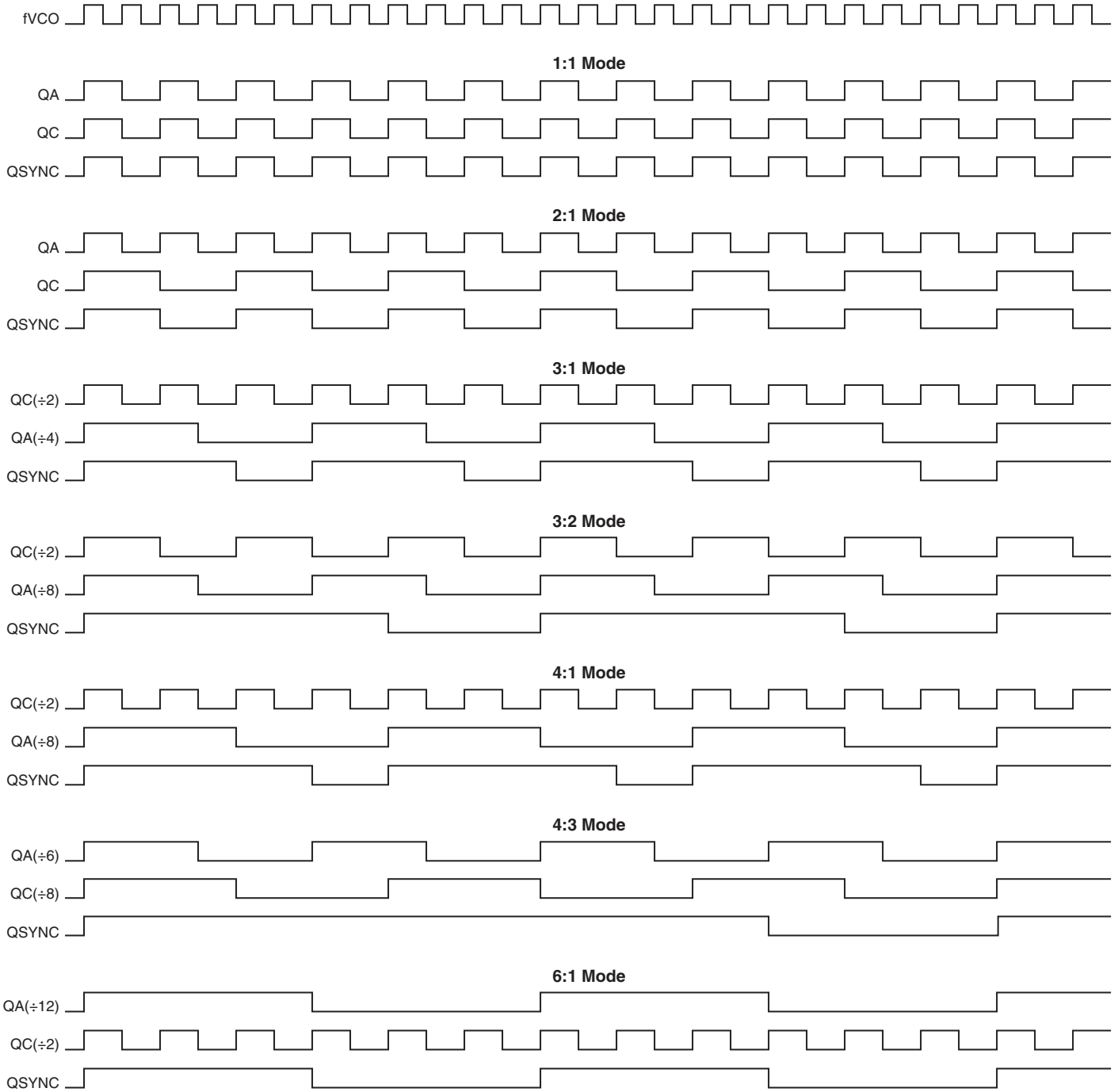
Inputs		Outputs	Inputs		Outputs	Inputs		Outputs
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

### Table 3B. Feedback Configuration Select Function Table

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

### Table 3C. Control Input Select Function Table

Control Pin	Logic 0	Logic 1
VCO_SEL	VCO/2	VCO
REF_SEL	CLK0 or CLK1	XTAL
CLK_SEL	CLK0	CLK1
PLL_SEL	BYPASS PLL	Enable PLL
nMR/OE	Master Reset/Output Hi-Z	Enable Outputs
INV_CLK	Non-Inverted QC2, QC3	Inverted QC2, QC3



**Figure 1. Timing Diagrams**

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	42.3°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				250	mA
$I_{DDA}$	Analog Supply Current				20	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	VCO_SEL, PLL_SEL, REF_SEL, CLK_SEL, EXT_FB, FSEL_FB[0:2], FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FRZ_DATA	-0.3		0.8	V
		CLK0, CLK1, INV_CLK, FRZ_CLK	-0.3		1.3	V
$I_{IN}$	Input Current				$\pm 120$	$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	$I_{OH} = -20\text{mA}$	2.4			V
$V_{OL}$	Output Low Voltage; NOTE 1	$I_{OL} = 20\text{mA}$			0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section. *Load Test Circuit diagram*.

**Table 5. Input Frequency Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$F_{IN}$	Input Frequency	CLK0, CLK1; NOTE 1			150	MHz
		XTAL1, XTAL		12	40	MHz
		FRZ_CLK			20	MHz

NOTE 1: Input frequency depends on the feedback divide ratio to ensure "clock \* feedback divide" is in the VCO range of 240MHz to 500MHz.

**Table 6. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

## AC Electrical Characteristics

**Table 7. AC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{MAX}$	Output Frequency	$\div 2$			150	MHz	
		$\div 4$			125	MHz	
		$\div 6$			83.33	MHz	
		$\div 8$			62.5	MHz	
$t(\phi)$	Static Phase Offset; NOTE 1	CLK0	QFB $\div 8$ , In Frequency = 50MHz	-10	145	300	ps
		CLK1		-65	90	245	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				200	ps	
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 3		All Banks $\div 4$		55	ps	
$f_{VCO}$	PLL VCO Lock Range		240		500	MHz	
$t_{LOCK}$	PLL Lock Time; NOTE 4				10	ms	
$t_R / t_F$	Output Rise/Fall Time		0.8V to 2V		0.15	0.7	ns
odc	Output Duty Cycle		45		55	%	
$t_{PZL}, t_{PZH}$	Output Enable Time; NOTE 4				10	ns	
$t_{PLZL}, t_{PHZ}$	Output Disable Time; NOTE 4				8	ns	

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

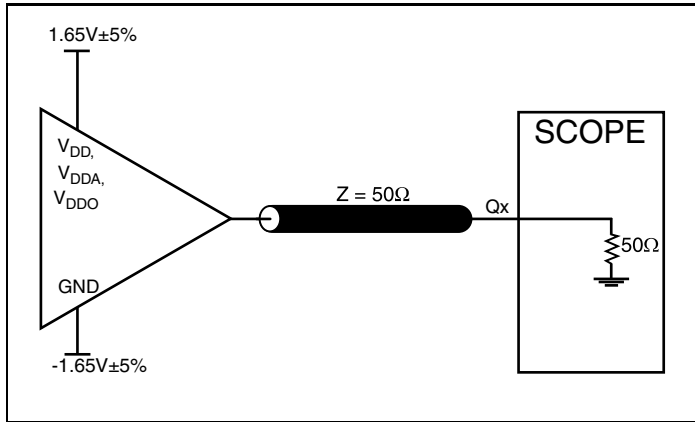
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

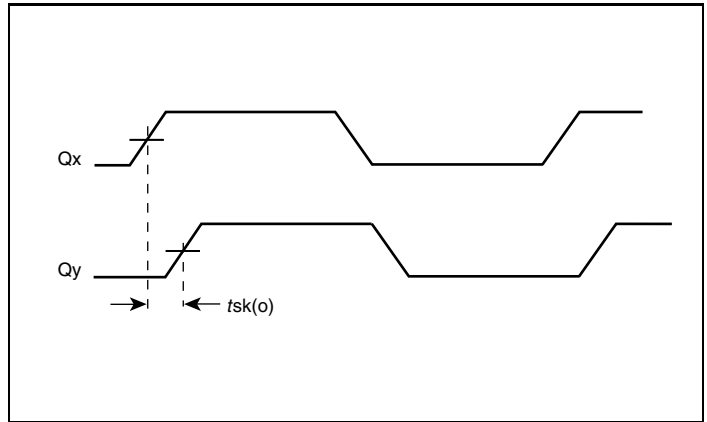
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.



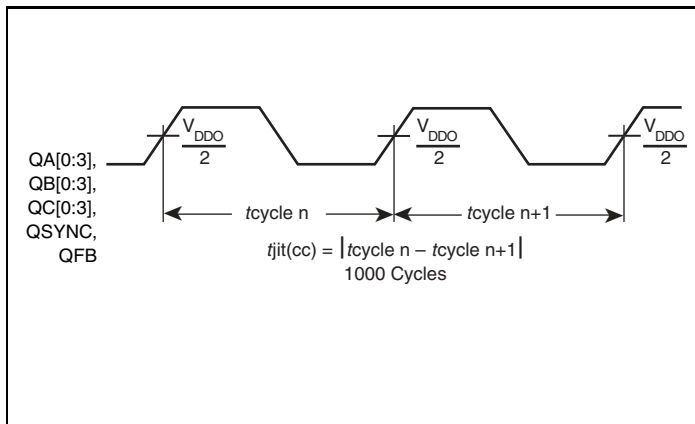
## Parameter Measurement Information



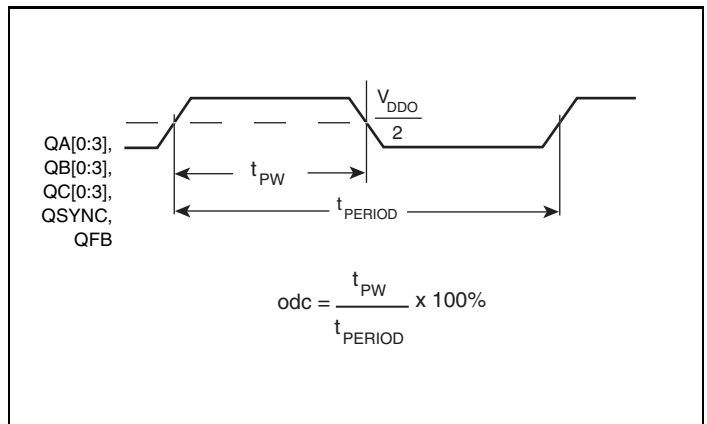
3.3V Core/3.3V LVC MOS Output Load AC Test Circuit



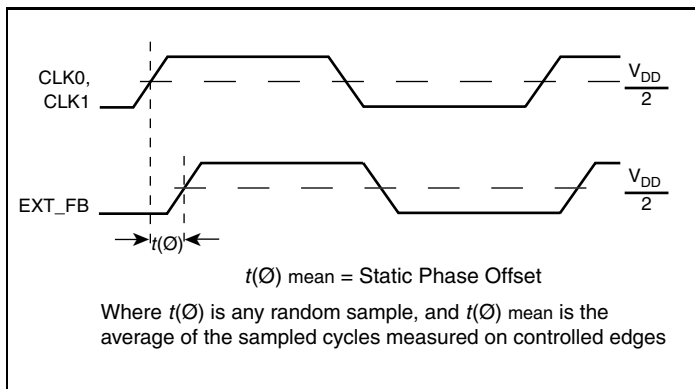
Output Skew



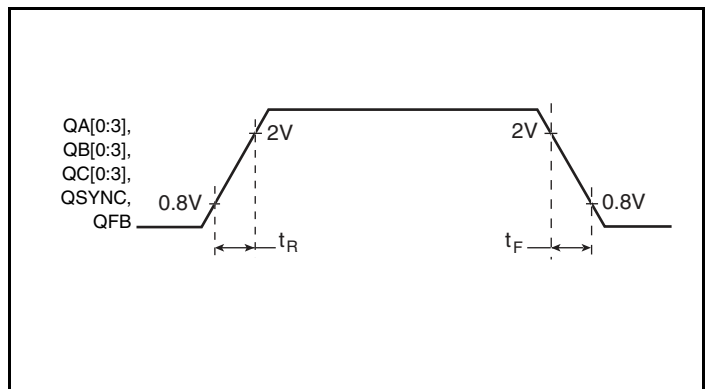
Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width Period



Static Phase Offset



Output Rise/Fall Time

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 87972I-147 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.

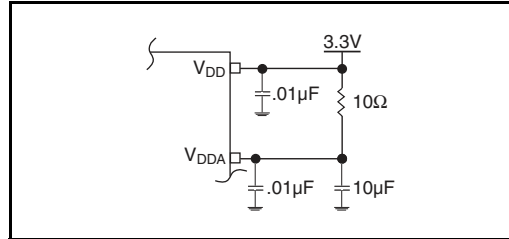


Figure 2. Power Supply Filtering

## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

#### CLK Inputs

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the CLK to ground.

#### LVC MOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

### Outputs:

#### LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

## Crystal Input Interface

The 87972I-147 has been characterized with 18 pF parallel resonant crystals. External capacitors are not required for this crystal interface. While layout the PC board, it is recommended to have spare footprints capacitor C1 and C2. If required, the spare C1 and C2 footprints can be used for fine tuned further for more accurate frequency. The possible C1 and C2 value are ranged from 2pF – 25pF. The suggest footprint size is 0402 or 0603.

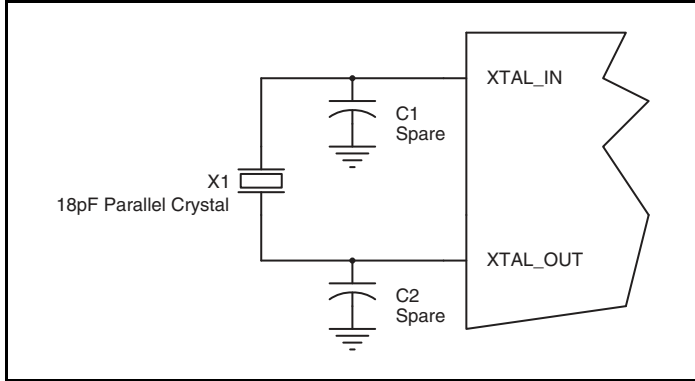


Figure 3. Crystal Input Interface

## LVC MOS to XTAL Interface

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

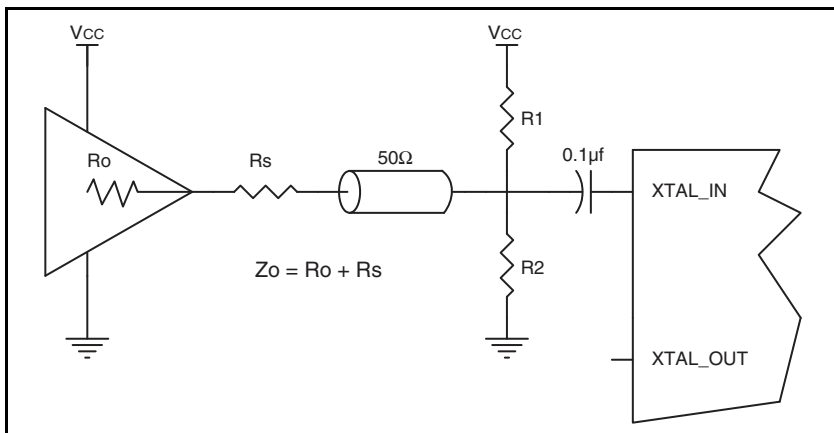


Figure 4. General Diagram for LVC MOS Driver to XTAL Input Interface

## Using the Output Freeze Circuitry

### OVERVIEW

To enable low power states within a system, each output of 87972I-147 (Except QC0 and QFB) can be individually frozen (stopped in the logic “0” state) using a simple serial interface to a 12 bit shift register. A serial interface was chosen to eliminate the need for each output to have its own Output Enable pin, which would dramatically increase pin count and package cost. Common sources in a system that can be used to drive the 87972I-147 serial interface are FPGA’s and ASICs.

### PROTOCOL

The Serial interface consists of two pins, FRZ\_Data (Freeze Data) and FRZ\_CLK (Freeze Clock). Each of the outputs which can be frozen has its own freeze enable bit in the 12 bit shift register. The sequence is started by supplying a logic “0” start bit followed by 12NRZ freeze enable bits. The period of each FRZ\_DATA bit equals the period of the FRZ\_CLK signal. The FRZ\_DATA serial transmission should be timed so the 87972I-147 can sample each

FRZ\_DATA bit with the rising edge of the FRZ\_CLK signal. To place an output in the freeze state, a logic “0” must be written to the respective freeze enable bit in the shift register. To unfreeze an output, a logic “1” must be written to the respective freeze enable bit. Outputs will not become enabled/disabled until all 12 data bits are shifted into the shift register. When all 12 data bits are shifted in the register, the next rising edge of FRZ\_CLK will enable or disable the outputs. If the bit that is following the 12th bit in the register is a logic “0”, it is used for the start bit of the next cycle; otherwise, the device will wait and won’t start the next cycle until it sees a logic “0” bit. Freezing and unfreezing of the output clock is synchronous (see the timing diagram below). When going into a frozen state, the output clock will go LOW at the time it would normally go LOW, and the freeze logic will keep the output low until unfrozen. Likewise, when coming out of the frozen state, the output will go HIGH only when it would normally go HIGH. This logic, therefore, prevents runt pulses when going into and out of the frozen state.

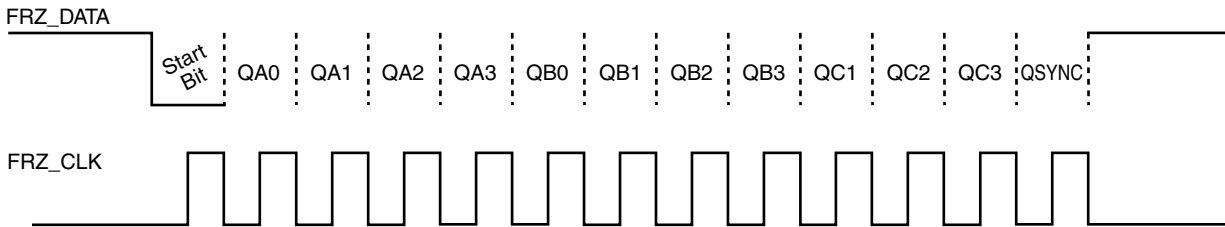


Figure 5A. Freeze Data Input Protocol

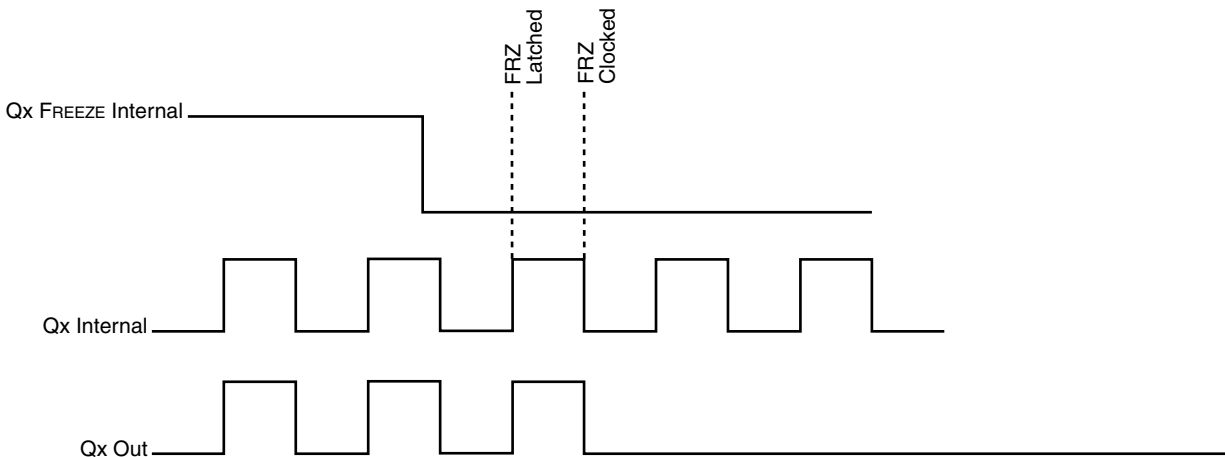


Figure 5B. Output Disable Timing Diagram

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 52 Lead LQFP**

$\theta_{JA}$ by Velocity			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### Transistor Count

The transistor count for 87972I-147: 8364

Pin Compatible with MPC972

## Package Outline and Package Dimensions

### Package Outline - Y Suffix for 52 Lead LQFP

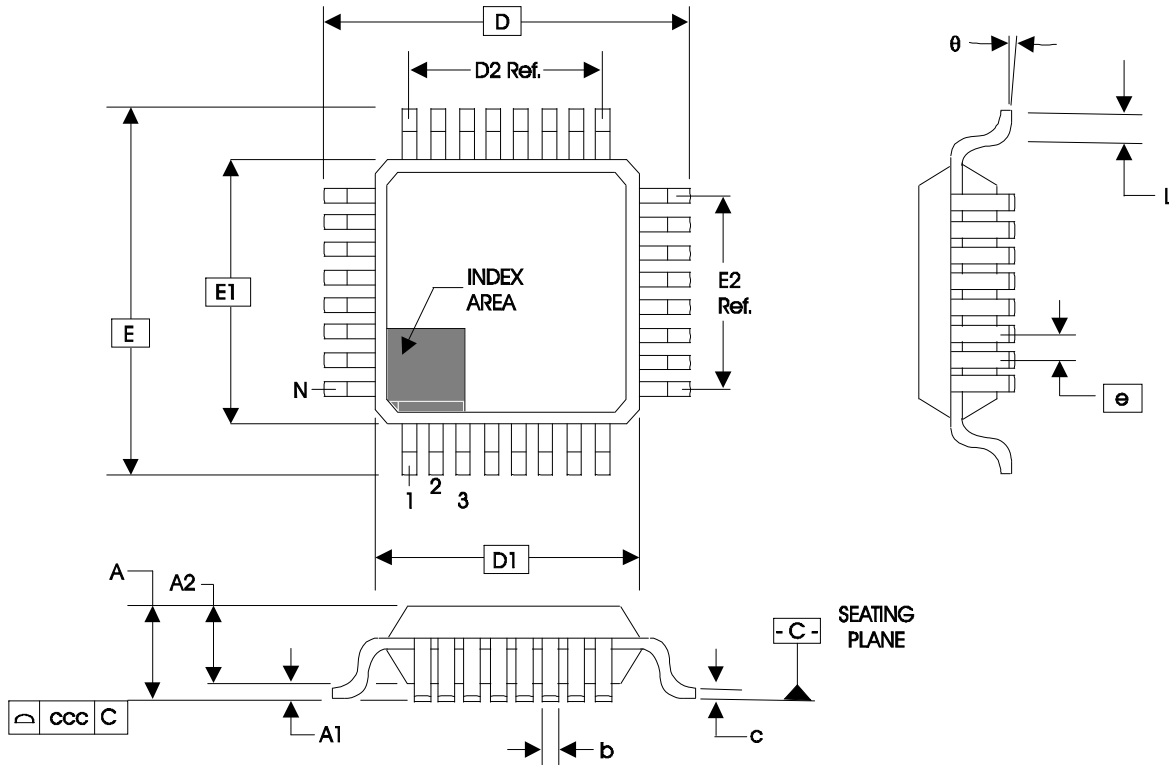


Table 9. Package Dimensions for 52 Lead LQFP

JEDEC Variation: BCC			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
<b>N</b>	52		
<b>A</b>			1.60
<b>A1</b>	0.05	0.10	0.15
<b>A2</b>	1.35	1.40	1.45
<b>b</b>	0.22		0.38
<b>c</b>	0.09		0.20
<b>D &amp; E</b>	12.00 Basic		
<b>D1 &amp; E1</b>	10.00 Basic		
<b>D2 &amp; E2</b>	7.80 Ref.		
<b>e</b>	0.65 Basic		
<b>L</b>	0.45	0.60	0.75
$\theta$	0°		7°
<b>ccc</b>			0.10

Reference Document: JEDEC Publication 95, MS-026

## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87972DYI-147LF	ICS87972DI147L	"Lead-Free" 52 Lead LQFP	Tray	-40°C to 85°C
87972DYI-147LFT	ICS87972DI147L	"Lead-Free" 52 Lead LQFP	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9 T10	1	Features Section - added leaf-free bullet.	6/5/08
		10	Added <i>Recommendations for Unused Input/Output Pins</i> section.	
		11	Added <i>LVC MOS to XTAL Interface</i> section.	
		14	Package Dimensions Table - added L and $\theta$ dimensions.	
		15	Ordering Information Table - added 52 Lead LQFP ordering information; corrected non-LF marking from ICS87972DYI147 to ICS87972DYI-147.	
A	T10	15	Ordering Information - Removed leaded devices, shipping tape and reel quantity and the LF note below the table. Updated datasheet format.	12/7/15







## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.