ISOLATED EVALUATION BOARD FOR THE Si3402

1. Description

The Si3402 isolated evaluation boards (Si3402 ISO-EVB Rev 1.0) is a reference design for power supplies in Power over Ethernet (PoE) Powered Device (PD) applications. The Si3402 is described more completely in the data sheet and application notes. This document describes only the Si3402 ISO-EVB evaluation board. An evaluation board demonstrating the non-isolated application is described in the Si3402-EVB User's Guide.

2. Planning for Successful Designs

Silicon Labs strongly recommends the use of the schematic and layout databases provided with the evaluation boards as the starting point for your design. Use of external components other than those described and recommended in this document is generally discouraged. Refer to Table 2 on page 10 for more information on critical component specifications. Careful attention to the recommended layout guidelines is required to enable robust designs and full specification compliance. To help ensure design success, please submit your schematic and layout databases to PoEInfo@silabs.com for review and feedback.

3. Si3402 Board Interface

Ethernet data and power are applied to the board through the RJ-45 connector (J1). The board may be powered by the following:

- Connecting a dc source to 1, 2 and 3, 6 (either polarity)
- Connecting a dc source to 4, 5 and 7, 8 (either polarity)
- Using an 802.3af-compliant PSE, such as Phihong PSA16U-480 (PoE)

The board itself has no Ethernet data transmission functionality. The dc output is at connectors J11(+) and J12(–). Boards are generally shipped configured to produce +5 V but can be configured for +3.3 V or other output voltages as shown in Table 2 on page 10. The Si3402 board schematics and layout are shown in Figures 1 through 6. The Si3402 ISO-EVB is normally populated for 5 V output class 3 signature and without the diode bridge bypass recommended for higher power levels. Use the ordering option Si3402 ISO-C4-EVB for 5 V output, class 4 signature and diode bridge bypass for higher power levels.

The feedback loop compensation has been optimized for 3.3, 5, 9, and 12 V output as well as with standard and low ESR capacitors in the output filter section (Table 2 on page 10). The use of low ESR capacitors is recommended for lower output ripple, improved load transient response and low temperature (below 0 °C) operation.

Copyright © 2010 by Silicon Laboratories

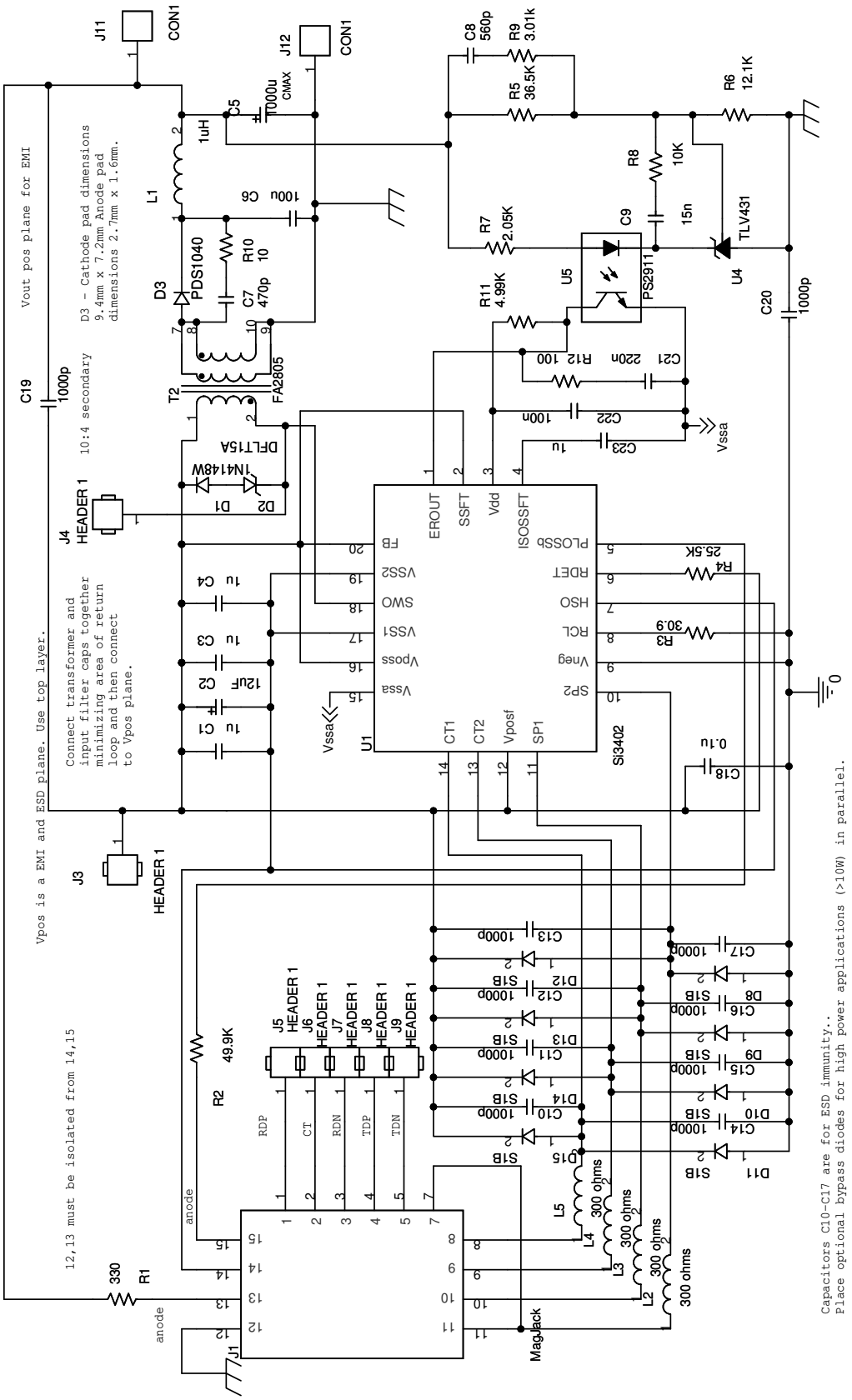

Figure 1. Si3402 Schematic—5 V, Class 3 PD

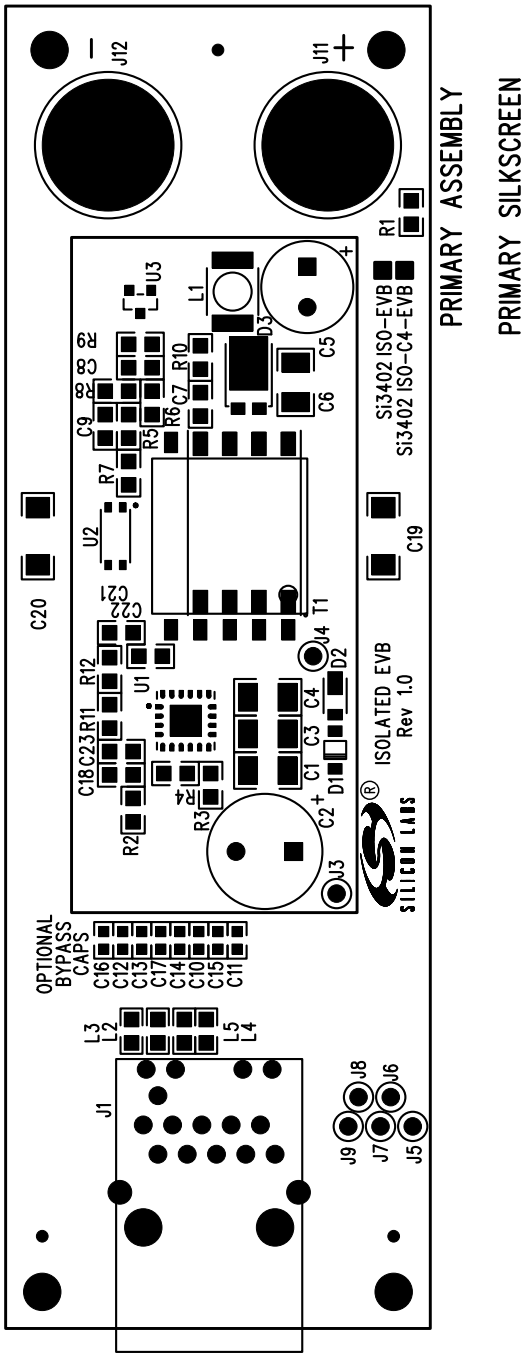

Figure 2. Si3402 Layout

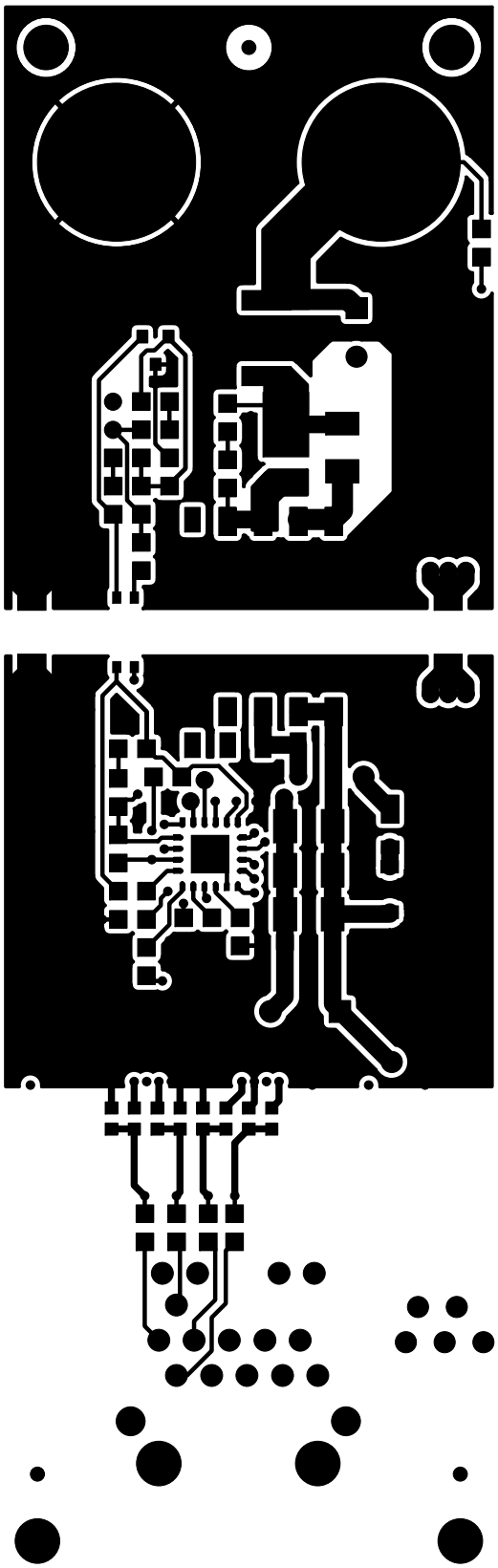

Figure 3. Primary Side

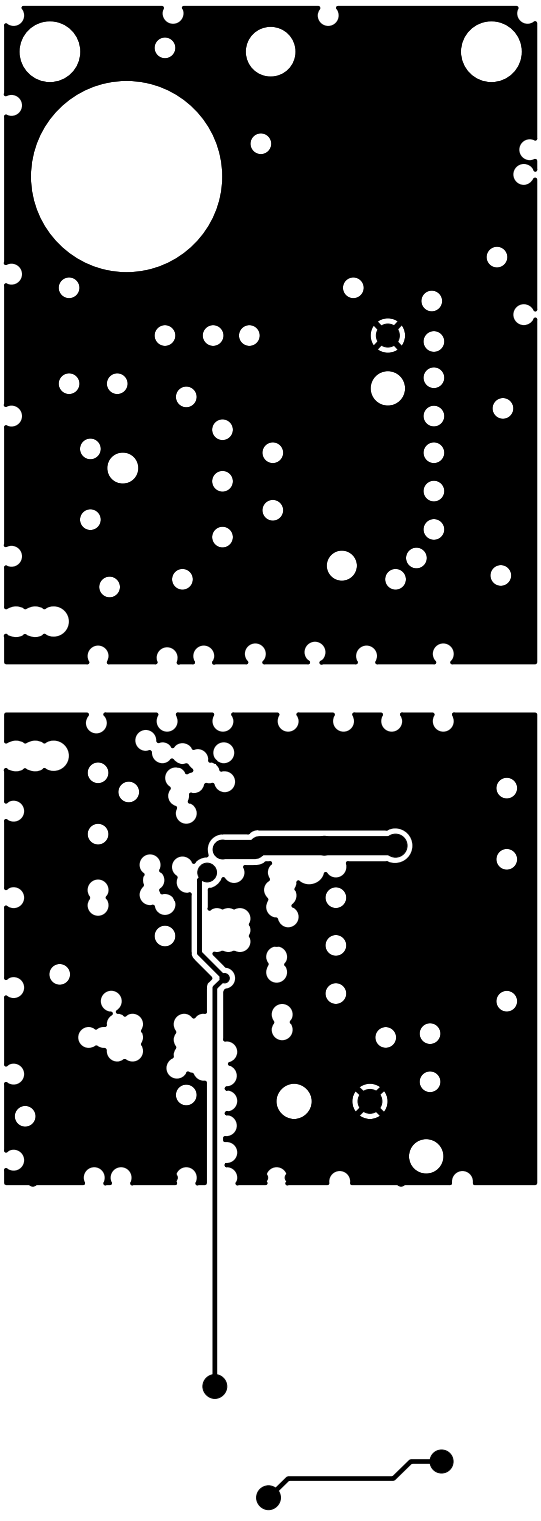

Figure 4. Internal 1

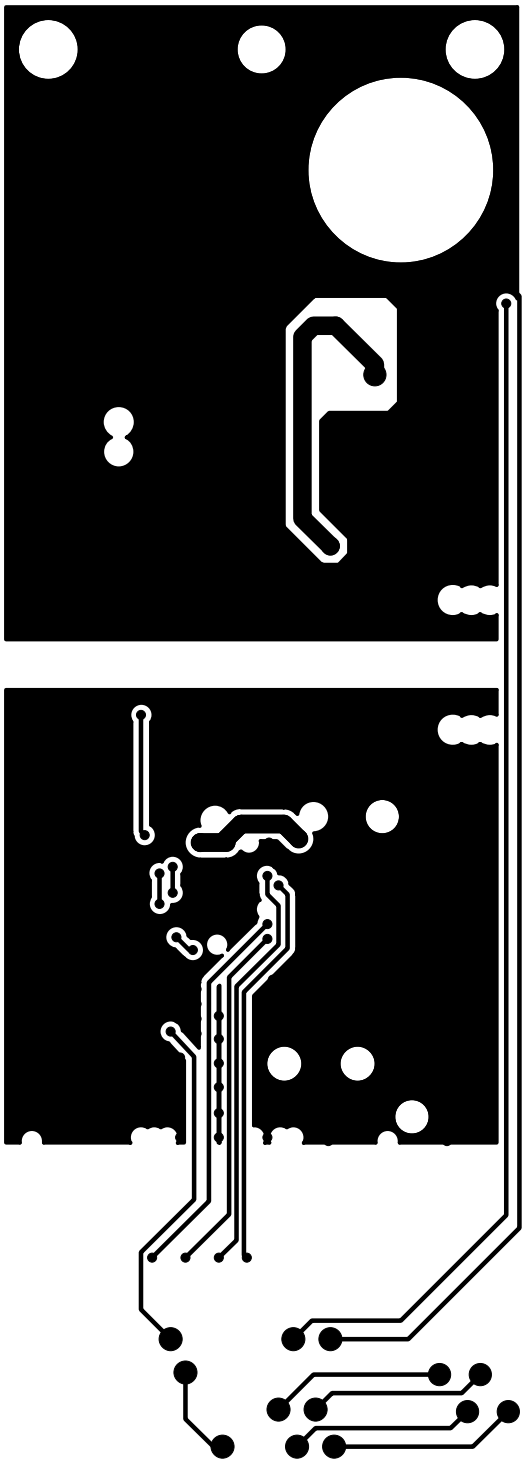

Figure 5. Internal 2

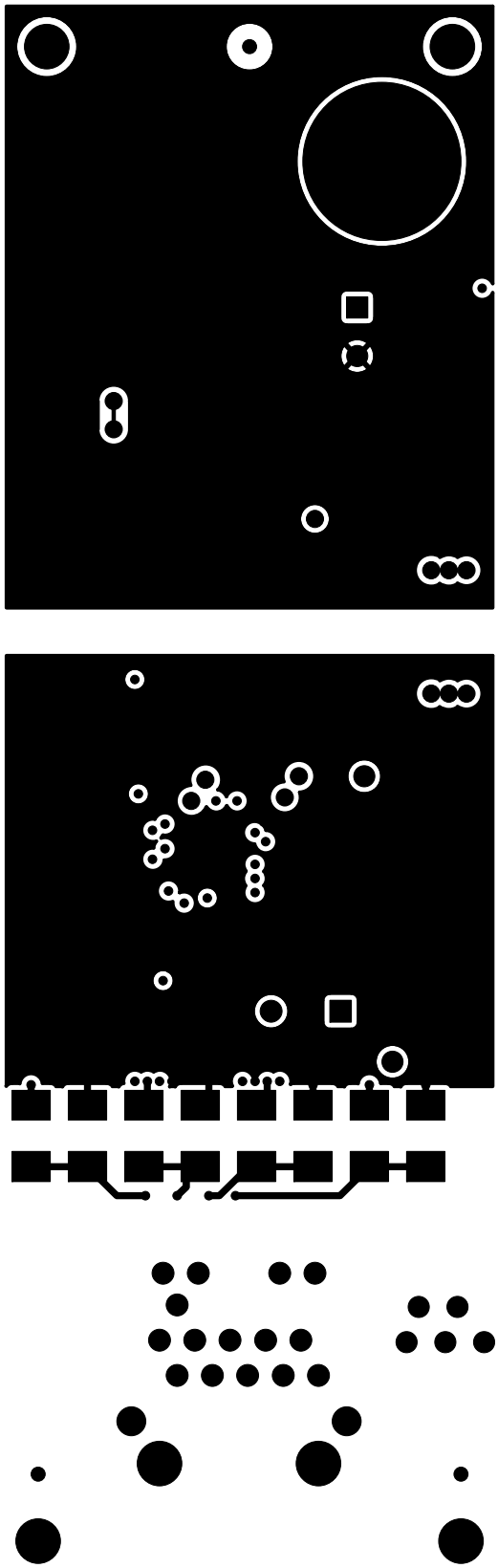

Figure 6. Secondary Side

4. Bill of Materials

The following bill of materials is for a 5 V, Class 3 design or a Class 4 design. Tables 2 and 3 list changes to the bill of materials for other output voltages and classification levels. Refer to “AN296: Using the Si3400, Si3401, and Si3402 PoE PD Controllers in Isolated and Non-Isolated Designs” and its accompanying Excel® spreadsheet utility for more information.

Table 1. Si3402 ISO-EVB Bill of Materials

Item	NI	Qty	Reference	Value	Rating	Tol	Dielectric	PCB Footprint	Manufacturer Part Number	Manufacturer
1		3	C1,C3,C4	1 µF	100 V	10%	X7R	1210	GRM32ER72A105KA01 C1210X7R101105K	Murata Venkel
2		1	C2	12 µF	100 V		Al Elec	thru hole	EEUFC2A120 100ME12AX	Panasonic Sanyo
3		1	C5	1000 µF	6.3 V			thru hole	ECA0JM102	Panasonic
4		1	C6	100 µF	6.3 V		X5R	CC1210	GRM32ER60J107ME20 C1210X5R6R3107K	Murata Venkel
5		1	C7	470 pF	50 V		X7R	CC0805	C0805X7R101471K	Venkel
6		1	C8	560 pF	16 V		X7R	CC0805	C0805X7R160561K	Venkel
7		1	C9	15 nF	16 V		X7R	CC0805	C0805X7R160153K	Venkel
8[1]		8	C10,C11,C12, C13,C14,C15, C16,C17	1000 pF	100 V	10%		CC0603	C0603X7R101102K	Venkel
		1	C18	0.1 µF	100 V	10%		805	C0805X7R101104K	Venkel
9		2	C19,C20	1000 pF	3 kV			1808	C1808X7R302102K	Venkel
10		1	C21	220 nF	16 V		X7R	CC0805	C0805X7R160224K	Venkel
		1	C22	100 nF	16 V		X7R	CC0805	C0805X7R160104K	Venkel
11		1	C23	1 µF	16 V		X7R	CC0805	C0805X7R160105K	Venkel
12		1	D1	1N4148W	100 V			SOD123	1N4148W	Diodes Inc.
13		1	D2	DFLT15A	15 V			DI123	DFLT15A	Diodes Inc.
14		1	D3	PDS1040				PDI5	PDS1040	Diodes Inc.
15		1	J1	MagJack				RJ45	SI-52003-F RJSE1R8090B-R	BelFuse Delta
16		2	J11,12	CON1					101	Abbatron HH Smith
17		1	L1	1 µH					DO1608C-102MLC	Coilcraft
18		4	L2,L3,L4, L5	300 Ω			Ferrite	805	BLM21P331SG	Murata
19		1	R1	330 Ω				805	CR0805-10W3300F	Venkel
20		1	R2	49.9 Ω	100 V			805	CR0805-8W4992F	Venkel
21	1		R3	30.9 Ω				805	CR0805-10W30R9F	Venkel (Class 4)
				45.3 Ω				805	CR0805-10W45R3F	Venkel (Class 3)
22		1	R4	25.5 kΩ				805	CR0805-10W2552F	Venkel
23		1	R5	36.5 kΩ				805	CR0805-10W36.5F	Venkel
24		1	R6	12.1 kΩ				805	CR0805-10W1212F	Venkel
25		1	R7	2.05 kΩ				805	CR0805-10W2051F	Venkel
26		1	R8	10 kΩ				805	CR0805-10W1002F	Venkel
27		1	R9	3.01 kΩ				805	CR0805-10W3011F	Venkel
28		1	R10	10 Ω				805	CR0805-10W10R0F	Venkel
29		1	R11	4.99 kΩ				805	CR0805-10W4991F	Venkel

Notes:
1. C10–C17 are populated by default. See the “Surge” section in AN296 for more information.
2. Bypass diodes D8–D15 are populated for the Class 4 option.

Table 1. Si3402 ISO-EVB Bill of Materials (Continued)

Item	NI	Qty	Reference	Value	Rating	Tol	Dielectric	PCB Footprint	Manufacturer Part Number	Manufacturer
31		1	R12	100 Ω				805	CR0805-10W1000F	Venkel
32		1	T1	COIL-CRAFT	transformer				FA2805CL	Coilcraft
33		1	U1	Si3402				5x5 QFN		Silabs
34		1	U2	PS2911 Opto				4 pin SO 4.6x2.5	PS2911-1-L	NEC
35		1	U3	TLV431				SOT23	TLV431	TI
37	NI	7	J3,J4,J5,J6, J7,J8,J9	HEADER 1				TESTPOINT		
37[2]	NI	8	D8,D9,D10,D11, D12,D13,D14, D15	S1B	1 A, 100 V			SMB	S1B	Diodes Inc.

Notes:
1. C10–C17 are populated by default. See the “Surge” section in AN296 for more information.
2. Bypass diodes D8–D15 are populated for the Class 4 option.

Table 2. Component Selection for other Output Voltages and Filter Types

3.3 V output	**Transformer* EP10 FA2671 EP13 FA2924AL**		**Output Rectifier: PDS1040 Snubber: R10, C7 470p,10**		**Reference Any TLV431**	
	R5 R6	C6	C5	Panasonic	R7, R9, R12	C8,C9,C21
Standard ESR Output Filter	24.3 kΩ 14.7 kΩ	100 µF X5R	1000 µF 6.3 V	ECA0JM102	1 kΩ, 3.01 kΩ, 100 Ω	560 pF, 15 nF, 0.22 µF
Low ESR Output Filter	24.3 kΩ 14.7 kΩ	100 µF X5R	560 µF 6.3 V	EEUFM0J561	1 kΩ, 1 kΩ, 47 Ω	8200 pF, 100 nF, 0.47 µF
5.0 V Output	**Transformer* EP10 FA2672 EP13 FA2805CL**		**Output Rectifier: PDS1040 Snubber: R10, C7 470p,10**		**Reference Any TLV431**	
	R5 R6	C6	C5	Panasonic	R7, R9, R12	C8,C9,C21
Standard ESR Output Filter	36.5 kΩ 12.1 kΩ	100 µF X5R	1000 µF 6.3 V	ECA0JM102	2.05 kΩ, 3.01 kΩ, 47 Ω	560 pF, 15 nF, 0.22 µF
Low ESR Output Filter	36.5 kΩ 12.1 kΩ	100 µF X5R	560 µF 6.3 V	EEUFM0J561	2.05 kΩ, 1 kΩ, 47 Ω	8200 pF, 100 nF, 0.47 µF
9.0 V Output	**Transformer* EP10 FA2732 EP13 FA2925AL**		**Output rectifier: PDS5100 Snubber: R10, C7 68p,20**		**Reference Higher voltage e.g., TLV431ASNT1G**	
	R5 R6	C6	C5	Panasonic	R7, R9, R12	C8,C9,C21
Standard ESR Output Filter	66.5 kΩ 10.5 kΩ	22 µF X5R	470 µF 16 V	ECA1M471	4.99 kΩ, 2.05 kΩ, 301 Ω	3300 pF, 47 nF, 0.22 µF
Low ESR Output Filter	66.5 kΩ 10.5 kΩ	22 µF X5R	330 µF 16 V	EEUFM1C331	4.99 kΩ, 2.05 kΩ, 1 kΩ	8200 pF, 22 nF, 0.1 µF
12.0 V Output	**Transformer* EP10 FA2732 EP13 FA2925AL**		**Output rectifier: PDS5100 Snubber: R10, C7 68p,20**		**Reference Higher voltage e.g., TLV431ASNT1G**	
	R5 R6	C6	C5	Panasonic	R7, R9, R12	C8,C9,C21
Standard ESR Output Filter	88.7 kΩ 10.2 kΩ	22 µF X5R	470 µF 16 V	ECA1M471	4.99 kΩ, 2.05 kΩ, 301 Ω	3300 pF, 47 nF, 0.22 µF
Low ESR Output Filter	88.7 kΩ 10.2 kΩ	22 µF X5R	330 µF 16 V	EEUFM1C331	4.99 kΩ, 2.05 kΩ, 1 kΩ	3300 pF, 22 nF, 0.1 µF

***Note:** Coilcraft part number. EP13 core is recommended for >10 W output power and short circuit protection.

Table 3. Component Selection for Different Classification Levels

Class	R3
0	Open
1	127
2	69.8
3	45.3
4	30.9

APPENDIX—Si3402 ISO DESIGN AND LAYOUT CHECKLIST

Introduction

Although all four EVB designs are pre-configured as a Class 3 PD with a 5 V output, the schematics and layouts can easily be adapted to meet a wide variety of common output voltages and power levels.

The complete EVB design databases for the standard 5 V/Class 3 configuration are located at www.silabs.com/PoE under the "Documentation" link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and to help avoid common mistakes in the schematic capture and PCB layout processes.

Following are recommended design checklists that can assist in trouble-free development of robust PD designs:

Refer also to the Si3402 data sheet and AN296 when using the checklists below.

1. **Design Planning Checklist:**
    a. Determine if your design requires an isolated or non-isolated topology. For more information, see Section 4 of AN296.
    b. To begin integrating the Si3402 into your schematics, download the schematic and layout database for your particular isolation requirements from www.silabs.com/PoE.
    c. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si3402 into your system design process.
    d. Determine your load's power requirements (i.e., V_{OUT} and I_{OUT} consumed by the PD, including the typical expected transient surge conditions). In general, to achieve the highest overall efficiency performance of the Si3402, choose the highest voltage used in your PD and then post regulate to the lower supply rails, if necessary.
    e. If your PD design consumes >10 W, make sure you bypass the Si3402's on-chip diode bridges with external diode bridges or discrete diodes. Bypassing the Si3402's on-chip diode bridges with external bridges or discrete diodes is required to help spread the heat generated in designs dissipating ≥10 W.
    f. Based on your required PD power level, select the appropriate class resistor value by referring to Table 2 of AN296. This sets the Rclass resistor (R3 in Figure 1 on page 2).
    g. The feedback loop stability has been checked over the entire load range for the specific component choices in Table 1. Low ESR filter capacitors will give better load transient response and lower output ripple so they are generally preferred. Silicon Laboratories recommends against component substitution in the filtering and feedback path as this may result in unstable operation. Also, use care in situations that have additional capacitive loading as this will also affect loop stability.
2. **Calculate Design-Specific External Components (for all designs which are not for a 5 V, Class 3 output configuration):**
    a. To help guide the selection of the other application-specific external component values needed for your design's isolation requirements, access the Excel spreadsheet utility at the following address: https://www.silabs.com/products/power/poe/Pages/default.aspx
        i. Use the "Non-isolated" worksheet if your design is intended for a non-isolated output supply.
        ii. Use either the "Isolated Continuous" or the "Isolated Discontinuous" worksheets if your design is for an isolated output supply ("continuous" versus "discontinuous" mode is determined by the current value calculated in cell H11 of the spreadsheet).
    b. If your design is a 5 V output Class 3 design, you do **not** need to change any external components.
    c. To avoid potential performance issues for non-5 V output configurations, Silicon Labs strongly recommends using the exact components and component values shown and calculated in the Excel worksheets.
    d. Begin entering your design targets in cells B9 through B13 of the Excel worksheet:

i. If using appropriate, select on-chip “diode bypass” option in cell B9 in the Excel spreadsheet utility. By entering a “1” in this cell, the Si3402’s on chip diodes are assumed to be bypassed with external diode bridges in your schematic. A “0” in this cell means the Si3402’s on-chip diode bridges will be used.

ii. Enter V_{IN} into cell B10. This voltage is the input voltage at the diode bridge output, which is 2 to 3 V less than the PSE input voltage, or typically 46 V.

iii. Enter your design’s desired output current, I_O in Amperes, into cell B11.

iv. Enter your design’s desired output voltage, V_O in Volts, in cell B12.

v. Enter your design’s maximum ambient operating temperature in °C into cell B13.

e. If you are using the “Non-isolated” worksheet:

i. The feedback resistor network values (R5 and R6) for your design are calculated and displayed in cells G13 and G12, respectively. Use these resistor values to update your schematic.

ii. To use the default diode and inductor components used in the Si3402-EVB non-isolated schematic, Silicon Labs strongly recommends leaving each default values “as-is” in cells B15 through B18.

iii. To ensure your design is operating within the acceptable operating ranges for all the external components you use in your schematic, carefully review the calculated values found in cells B20 through B27.

iv. Carefully review the calculated values in the Summary section (cells B29 through B33).

1. Cell B29: PSE input voltage. Make sure the PSE input voltage is compatible with the PSE intended to power your PD.
2. Cell B30: PSE input power. If the power is >12.95 W (more than the IEEE 802.3af limits), then this cell is shaded in light RED and your PSE must be capable of sourcing the power level shown in cell B30.
3. Cell B33: If the calculated junction temperature is $\geq$140 °C, then this cell is shaded in light red. Consider bypassing the on-chip diodes to lower the effective junction temperature, or reducing the output current (if possible). Other inputs in cells B9 through B13 may also need to be adjusted to lower the calculated junction temperature.

f. If you are using either of the “Isolated” worksheets, enter in the input values to determine if your design will be operating in the “continuous” mode or the “discontinuous mode”:

i. Check the value of the current calculated in cell H11.

1. If your desired output current (B11) is **less than** the value shown in cell H11, then use the “Isolated Discontinuous” worksheet.
2. If your desired output current (B11) is **greater than** the value shown in cell H11, then use the “Isolated Continuous” worksheet.

ii. The feedback resistor network values (R5 and R6) for your design are calculated and displayed in cells E12 and E13, respectively. Use these resistor values to update your schematic.

iii. Select transformer turns ratio: use 3.3, 2.5 or 1 as standard choices for 3.3, 5, and 12 V output, respectively. Leave the rest of the options as defaults. If you have different output voltage, then contact Silicon Labs for recommendations.

iv. To use the default transformer, snubber and diode components used in the Si3402 ISO-EVB isolated schematic, Silicon Labs strongly recommends leaving each default values “as-is” in cells B15 through B23. Always select the EP13 core if you require short circuit protection.

v. To ensure your design is operating within the acceptable operating ranges for all the external components you use in your schematic, carefully review the calculated values found in cells B25 through B35.

vi. Carefully review the calculated values in the Summary section (cells B37 through B41):

1. Cell B37: PSE input voltage. Make sure the PSE input voltage is compatible with the PSE intended to power your PD.
2. Cell B38: PSE input power. If the power is >12.95 W (more than the IEEE 802.3af limits), then this cell is shaded in light RED and your PSE must be capable of sourcing the power level shown in cell B30.
3. Cell B41: If the calculated junction temperature is ≥140 °C, then this cell is shaded in light red. Consider bypassing the on-chip diodes to lower the effective junction temperature, or reducing the output current (if possible). Other inputs in cells B9 through B13 may also need to be adjusted to lower the calculated junction temperature.

3. **General Design Checklist Items:**

a. ESD caps (C10–C17 in Figure 1) are strongly recommended for designs where system-level ESD (IEC6100-4-2) must provide >15 kV tolerance.

b. Never disable the soft start features. Make sure the soft start capacitor is in your schematics and connected correctly.

c. If your design uses an AUX supply, make sure to include a 3 Ω surge limiting resistor in series with the AUX supply for hot insertion. Refer to AN296 when AUX supply is 48 V.

d. Silicon Labs strongly recommends the inclusion of a minimum load (250 mW) to avoid switcher pulsing when no load is present, and to avoid false disconnection when less than 10 mA is drawn from the PSE. If your load is not at least 250 mW, add a resistor load to dissipate at least 250 mW.

e. If using PLOSS function, make sure it's properly terminated for connection in your PD subsystem. If PLOSS is not needed, float this pin.

4. Layout Guidelines:

a. Make sure the VNEG pin of the Si3402 is connected to the backside of the QFN package with an adequate thermal plane, as noted in the data sheet and AN296.

b. Keep the trace length from connecting to SWO and retuning to Vss1 and Vss2 as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere.

c. Usually one standard via handles 200 mA of current. If the trace will need to conduct a significant amount of current from one plane to the other use multiple vias.

d. Keep the circular area of the loop from the Switcher FET output to the inductor or transformer and returning from the input filter capacitors (C1–C4) to Vss1 and Vss2 as small a diameter as possible. Also, minimize the circular area of the loop from the output of the inductor or transformer to the Schottky diode and retuning through the fist stage output filter capacitor back to the inductor or transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.

e. Connect the sense points to the output terminals directly to avoid load regulation issues related to IR drops in the PSB traces. For the non-isolated case the sense points are Vposs and the sense resistor R6. For the non-isolated case the sense points are R5 and the TLV431 pin 3.

f. Keep the feedback and loop stability components as far from the transformer/inductor and noisy power traces as possible.

g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together and then connect to the plane at a single point.

h. As a convenience in layout, please note that the IC is symmetrical with respect to CT1, CT2, SP1 and SP2. These leads can be interchanged.

To help ensure first pass success, please submit your schematics and layout files to PoEInfo@silabs.com for review. Other technical questions may be sent to this e-mail address as well.

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Updated schematics and BOM to latest recommendations.
- Updated artwork to correct errors and for improved EMI.
- Added component selection tables.

Revision 0.3 to Revision 0.4

- Updated layout to Rev 1.2.
- Updated "4. Bill of Materials," on page 8 for Rev D, Si3400/01.
- Added Si3401.

Revision 0.4 to Revision 0.5

- Updated Figure 1, “Si3402 Schematic—5 V, Class 3 PD,” on page 2 to include ISOSSFT (pin 4) for the isolated mode soft start feature (for revisions beginning with Rev. E), Vssa support and ESD improvements.
- Updated "4. Bill of Materials," on page 8 per schematic.

Revision 0.5 to Revision 0.6

- Updated all Figures and Tables.
- Updated BOM.
- Added Appendix.

Revision 0.6 to Revision 0.7

- Updated low ESR compensation for the 3.3 V and 5 V cases.

Revision 0.7 to Revision 0.8

- Changed document title from Si3400/Si3401ISO-EVB to Si3400/1/2 ISO-EVB.
- Updated "4. Bill of Materials," on page 8.

Revision 0.8 to Revision 1.0

- Added Si3402 ISO-C4-EVB
- Removed Si3400/01 as the Si3402 replaces these.

Revision 1.0 to Revision 1.1

- Updated schematic.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.

Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.