To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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78K0/LE2

8-BIT SINGLE-CHIP MICROCONTROLLE

The 78K0/LE2 products are 8-bit single-chip microcontrollers of the 78K0 series.

These microcontrollers feature Single-voltage Self-programming Flash memory, LCD C/D and many peripherals.

FEATURES

- 78K0 CPU core, 8-bit CISC architecture
- Flash EEPROM and RAM sizes

Item / Product name	Program memory	Data memory
uPD78F0363	32K bytes (Flash)	1K bytes
uPD78F0361	16K bytes (Flash)	768 bytes

Minimum instruction cycle

0.1 µs (20MHz@4.0V to 5.5V)
0.2 µs (10MHz@2.7V to 5.5V)
0.4 µs (5MHz@1.8V to 5.5V)

Clock

- Main clock
  - Internal Ring-oscillator 8MHz (Typ.)
  - External Ceramic or Crystal Oscillator(2MHz to 20MHz)
  (Instruction execution time = 100ns(min.) @20MHz)
- SUB CLOCK
  - 32.768KHz Crystal oscillator
- WDT CLOCK
  - Internal Ring-oscillator 240KHz (Typ.)

Peripherals

- On-Chip Power-On-Clear(POC) Circuit
- Low-Voltage Detector(LVI) Circuit
- Timer
  - 16bit Timer 1ch
  - 8bit Timer 4ch
  - Watch Timer
  - Watchdog Timer (Operable with 240KHz Ring-OSC)
- Serial I/F
  - UART0/CSI1 1ch
  - UART6 (with LIN-bus) 1ch
  - IIC 1ch
- LCD C/D
  - Segment signal output 20 (max)
  - Common signal output 4 (max)
  - booster type or ladder type selectable
- A/D Converter
  -10-bit resolution A/D converter 5ch
- I/O port
  - CMOS I/O : 24 + IIC : 2
- Operation Voltage : 1.8V to 5.5V
- Package
  - 64-pin QFP(12mm x 12mm, 0.65mm pitch)
  - 64-pin QFP(10mm x 10mm, 0.5mm pitch)
- Other
  - On-chip debug function*

* uPD78F0363D

)

This information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion

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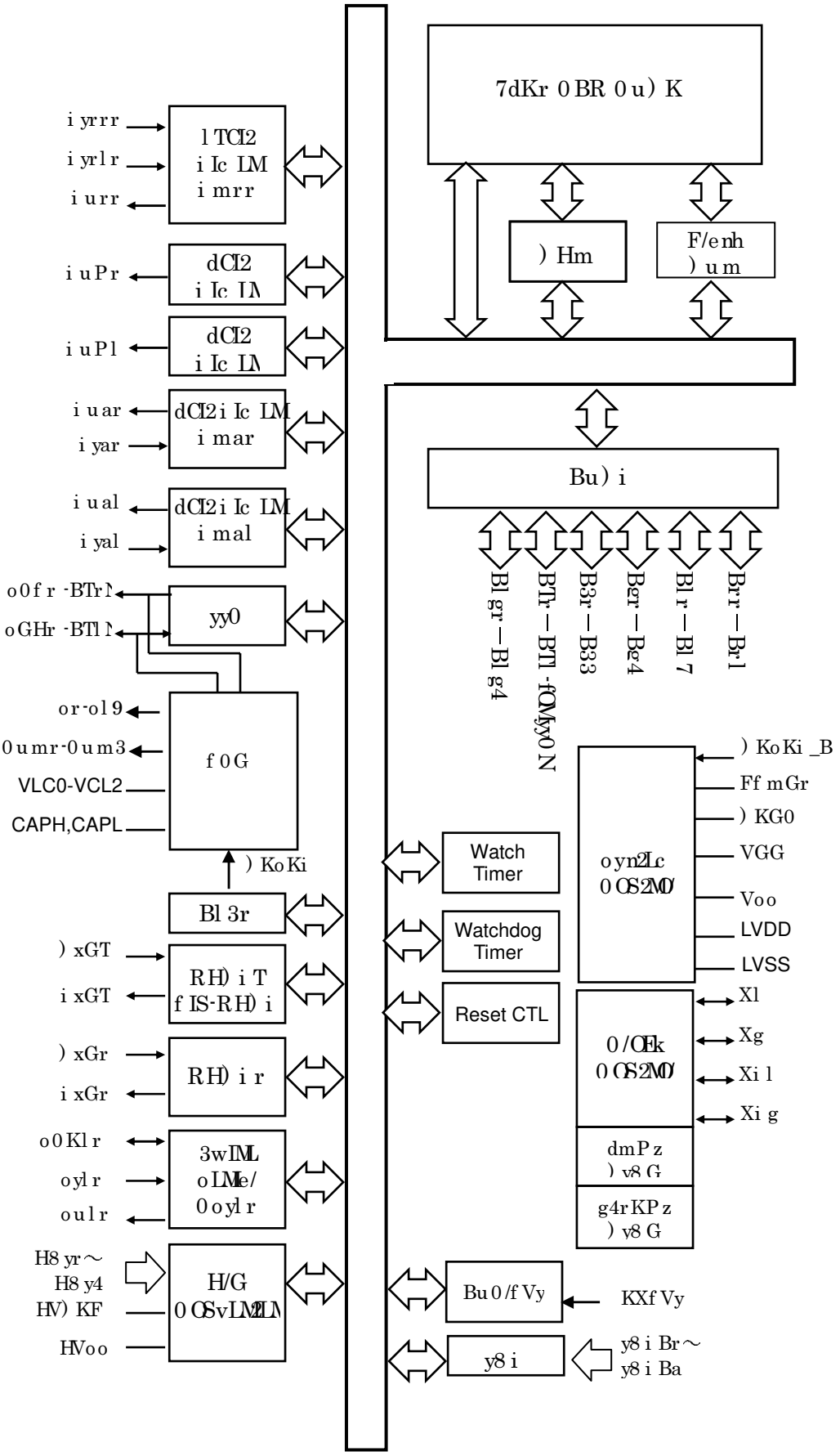
1. Block Diagram

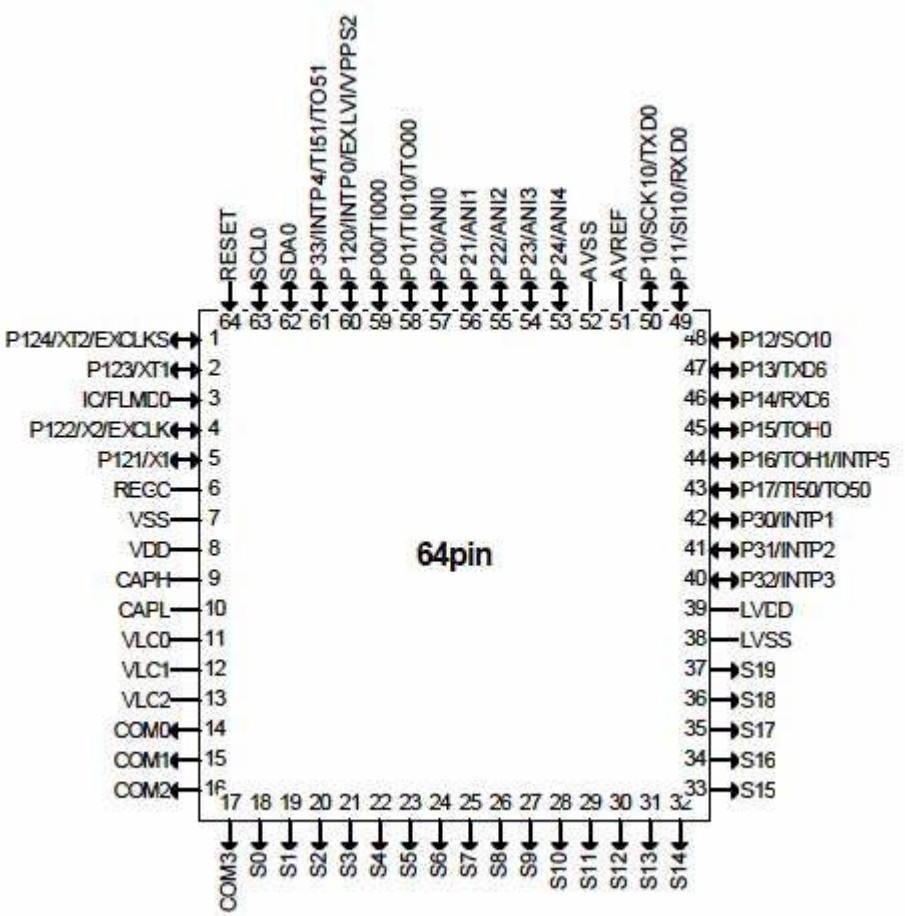


2. Pin Function (uPD78F0373, uPD78F0375)

PIN NAME	Function
VDD	Positive power supply
VSS	Ground potential
LVDD	Positive power supply
LVSS	Ground potential
RESET_B	System reset input
FLMD0	Flash EEPROM programming mode setting
REGC	Connecting regulator stabilization capacitor. Connect to GND via a capacitor (0.47 µF)
AVREF	A/D converter analog power supply and power supply for P20-P24
AVSS	Ground potential for A/D converter and P20 - P24
VLC0 VLC1 VLC2	LCD driving voltage • VLC0: Three times VLC2 output voltage • VLC1: Two times VLC2 output voltage • VLC2: Reference voltage
CAPH CAPL	Booster capacitor connection for LCD drive voltage
COM0-COM3	LCD controller/driver common signal output
P00 /TI000	I/O port
	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00 (TM00)
P01 /TI010 /TO00	I/O port
	Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00 (TM00)
	16-bit timer/event counter 00 output (TM00)
	16-bit timer/event counter 01 output (TM01)
P10 /SCK10 /TXD0	I/O port
	Clock input/ output for serial interface (CSI10)
	Serial data output from asynchronous serial interface (UART0)
P11 /SI10 /RXD0	I/O port
	Serial data input to serial interface (CSI10)
	Serial data input to asynchronous serial interface (UART0)
P12 /SO10	I/O port
	Serial data output form serial interface (CSI10)
P13 /TXD6	I/O port
	Serial data output from asynchronous serial interface (UART6)
P14 /RXD6	I/O port
	Serial data input to asynchronous serial interface (UART6)
P15 /TOH0	I/O port
	8-bit timer H0 output (TMH0)
P16 /TOH1 /INTP5	I/O port
	8-bit timer H1 output (TMH1)
	External interrupt request input with specifiable valid edges
P17 /TI50 /TO50	I/O port
	External count clock input to 8-bit timer/event counter 50 (TM50)
	8-bit timer/event counter 50 output (TM50)
P20/ANI0- P24/ANI7	I/O port
	port/Analog input of A/D converter
P30/INTP1 P31/INTP2 P32/INTP3	I/O port
	External interrupt request input with specifiable valid edges
P33 /TI51 /TO51 /INTP4	I/O port
	External count clock input to 8-bit timer/event counter 51(TM51)
	8-bit timer/event counter 51output(TM51)
	External interrupt request input with specifiable valid edges

(P60) /SCL0	(IIC only) Clock input/ output for serial interface (IIC0)
(P61) /SDA0	(IIC only) Serial data input/ output for serial interface (IIC0)
P120 /INTP0 /EXLVI	I/O port External interrupt request input with specifiable valid edges Reference voltage input for Low voltage Indicator
P121 /X1	I/O port (An external oscillation circuit is not used) Connecting resonator for main system clock oscillation
P122 /X2	I/O port (An external oscillation circuit is not used) Crystal connection for main system clock oscillation
P123 /XT1	I/O port (An external oscillation circuit is not used) Crystal connection for subsystem clock oscillation
P124 /XT2	I/O port (An external oscillation circuit is not used) Crystal connection for subsystem clock oscillation
S0-S19	LCD controller/driver segment signal output

3. Pin Lay Out


RESET
SCL0
SDA0
P33/INTP4/TI51/TO51
P120/INTP0/EXLVI/VPPS2
P00/TI000
P01/TI010/TO00
P20/ANI0
P21/ANI1
P22/ANI2
P23/ANI3
P24/ANI4
AVSS
AVREF
P10/SCK10/TXD0
P11/SI10/RXD0
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
P124/XT2/EXCLKS 1
P123/XT1 2
IC/FLMD0 3
P122/X2/EXCLK 4
P121/X1 5
REGC 6
VSS 7
VDD 8
CAPH 9
CAPL 10
VLC0 11
VLC1 12
VLC2 13
COM0 14
COM1 15
COM2 16
48 P12/SO10
47 P13/TXD6
46 P14/RXD6
45 P15/TOH0
44 P16/TOH1/INTP5
43 P17/TI50/TO50
42 P30/INTP1
41 P31/INTP2
40 P32/INTP3
39 LVDD
38 LVSS
37 S19
36 S18
35 S17
34 S16
33 S15
64pin
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
COM3 S0 S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14

4. Memory space

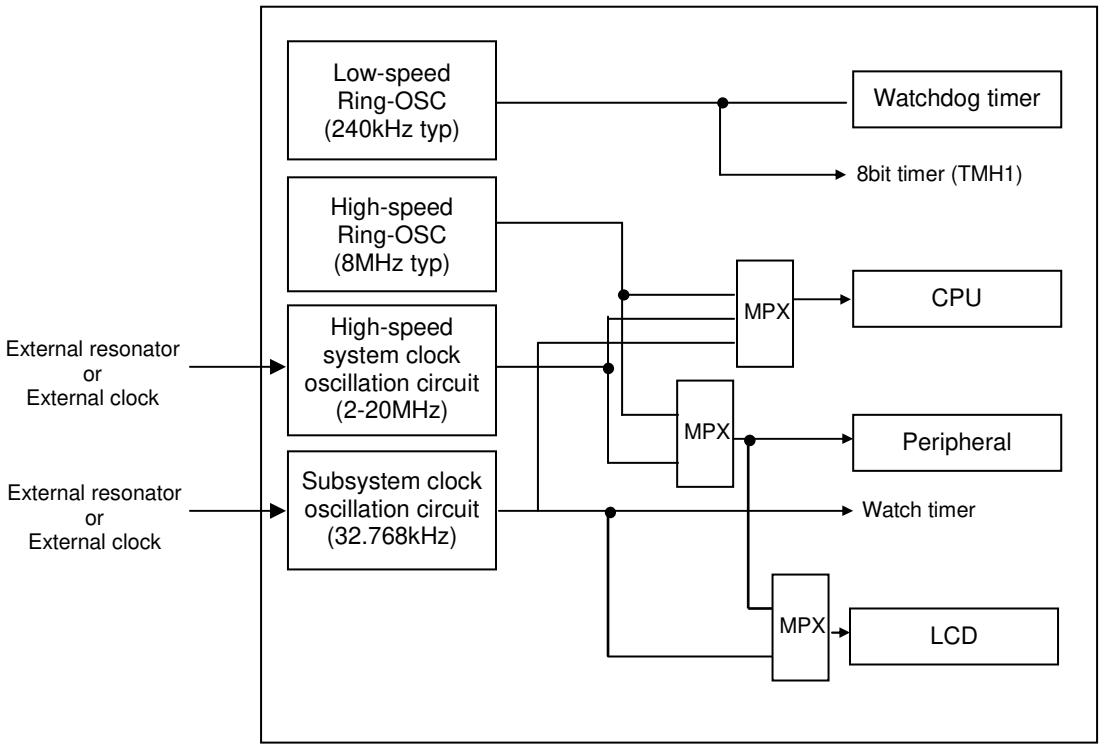
78K0/LE2 have 64KB linear address area.

Products	ROM size	ROM address	Common area address	Bank area address	Number of Bank
μPD78F0363	32KB	0000H-7FFFH	-	-	-
μPD78F0341	16KB	0000H-3FFFH	-	-	-

5. Clock

78K0/LE2 have 3 type internal Ring-OSC and 2 type external resonator oscillation circuit.
78K0/LE2 can be operated high-speed internal Ring-OSC only. 240KHz Ring-OSC can connect to Watch dog timer and 8bit timer (TMH1) only for high secure.

Fig. Clock connecting block image



6. Outline of Functions of 78K0/Lx2

Table 78K0/Lx2 Functions

			LE2	LF2		LF2F		LG2	
Package			64	80				100	
CPU			8bit CPU						
Oscillation circuit	Main	Cera/ Crystal	Vdd=4.0V-5.5V:20MHz Vdd=2.7V-5.5V:10MHz Vdd=1.8V-5.5V:5MHz						
		Ring OSC	Vdd=1.8V-5.5V:8MHz						
	Ring-OSC		Vdd=2.7V-5.5V:240KHz						
	Sub Clock		32.768KHz						
VDD			1.8V-5.5V						
Flash ROM (K byte)			16/32	32	60	32	60	32	60/128
RAM (K byte)			768/1	1	3	1	3	1	3/7
LCD Segment (MAX.)			80	104		144		160	
Timer	16bit	TM0	1		2	1	2	1	2
	8bit	TM5	2						
		TMH	2						
	WDT		1						
	WT		1						
Serial	3SIO/UART		1						
	3SIO		-						1
	UART		1						
	IIC*		1						
10bit A/D			5ch	8ch		-		8ch	
Key return			-	7pins				8pins	
Multiplier/Divider			-		Yes	-	Yes	-	Yes
LVI/POC			Yes						
Flash Self Programming			Yes						

*Shared with internal communication

7. Electrical specification of LE2 (Target)

Caution These specifications show target values, which may change after device evaluation. The operating voltage range may also change.

Absolute Maximum Ratings(T_A = 25° C)

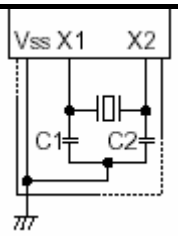
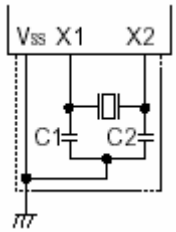
Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	VDD	VDD=LVDD		-0.5 to +6.5	V
	LVDD	VDD=LVDD		-0.5 to +6.5	V
	VSS			-0.5 to +0.3	V
	LVSS			-0.5 to +0.3	V
	AVREF			-0.5 to VDD+0.3 Note	V
	AVSS			-0.5 to +0.3	V
Input voltage	VI1	P00-P01,P10-P17,P20-P24,P30-P33, P120-P124, X1,X2,Xt1,Xt2,RESET_B		-0.3 to VDD+0.3 Note	V
	VI2	P60-P61(N-ch open drain)		-0.3 to +6.5	V
Output voltage	VO			-0.3 to VDD+0.3 Note	V
Analog input voltage	VAN			-0.3 to AVREF+0.3 Note and -0.3 to VDD+0.3 Note	V
Output current, high	IOH	Per pin		-10	mA
		Total of all pins -80 mA	P00-P01, P120-P124	-25	mA
			P05-P06,P10-P17,P30-P33	-55	mA
Output current, low	IOL	Per pin		30	mA
		Total of all pins 200 mA	P00-P01, P120-P124	60	mA
			P10-P17,P30-P33, P60-P61	140	mA
Operating ambient temperature	TA	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

High-Speed System Clock (Crystal/Ceramic) Oscillator Characteristics
(TA = -40 to +85°C, 1.8 V . VDD = LVDD . 5.5 V, 2.3 V < AVREF . VDD= LVDD, VSS = LVSS = AVSS = 0 V)

Resonator	Recommended Circuit	Conditions		MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency(f_{XH}) **Note**	4.0 V < V_{DD} < 5.5 V	2.0		20.0	MHz
			2.7 V < V_{DD} < 4.0 V	2.0		10.0	
			1.8 V < V_{DD} < 2.7 V	2.0		5.0	
Crystal resonator		Oscillation frequency(f_{XH})**Note**	4.0 V < V_{DD} < 5.5 V	2.0		20.0	MHz
			2.7 V < V_{DD} < 4.0 V	2.0		10.0	
			1.8 V < V_{DD} < 2.7 V	2.0		5.0	

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions
1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the Ring-OSC after reset is released, check the oscillation stabilization time of the high-speed system clock using the oscillation stabilization time status register (OSTC). Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

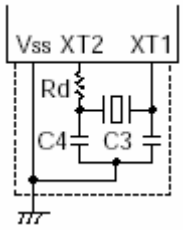
Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Ring-OSC Oscillator Characteristics
(TA = -40 to +85°C, 1.8 V < VDD = LVDD < 5.5 V, 2.3 V < AVREF . VDD= LVDD, VSS = LVSS = AVSS = 0 V)

Resonator	Parameter		MIN.	TYP.	MAX.	Unit
8MHz Ring-OSC oscillator	High-speed Ring-OSC Oscillation frequency(fRH) Note	2.7 V< VDD < 5.5 V	7.6 Note2	8.0 Note2	8.4 Note2	MHz
		1.8 V< VDD < 2.7 V		8.0 Note2		MHz
240KHz Ring-OSC oscillator	Low-speed Ring-OSC Oscillation frequency(fRL) Note	2.7 V< VDD < 5.5 V	216	240	264	KHz
		1.8 V< VDD < 2.7 V	TBD	240	TBD	KHz

Note
1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.
2. This is the frequency in the case of RSTS(RCM.7)=1. This is 5 MHz(TYP.) in the case of RSTS=0.

Subsystem Clock Oscillator Characteristics
(TA = -40 to +85°C, 1.8 V < VDD = LVDD < 5.5 V, 2.3 V < AVREF . VDD= LVDD, VSS = LVSS = AVSS = 0 V)

Resonator	Recommended Circuit	Conditions		MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency(f_{SUB})Note	1.8 V< V_{DD} < 2.7 V	32	32.768	35	KHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions
1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing power

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (1/3)

(TA = -40 to +85°C, 1.8V < VDD = LVDD < 5.5 V, VSS = EVSS = AVSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH1}	Per pin of P00-P01, P10-P17, P30-P33, P120	4.0 V< VDD < 5.5 V			-3.0	mA
			2.7 V< VDD < 4.0 V			-2.5	
			1.8 V< VDD < 2.7 V			-1.0	
		Total of P00-P01, P120	4.0 V< VDD < 5.5 V			-20.0	mA
			2.7 V< VDD < 4.0 V			-10.0	
			1.8 V< VDD < 2.7 V			-5.0	
		Total of P10-P17, P30-P33	4.0 V< VDD < 5.5 V			-30.0	mA
			2.7 V< VDD < 4.0 V			-19.0	
			1.8 V< VDD < 2.7 V			-10.0	
		Total of all pins	4.0 V< VDD < 5.5 V			-50.0	mA
			2.7 V< VDD < 4.0 V			-29.0	
			1.8 V< VDD < 2.7 V			-15.0	
	I_{OH2}	Per pin of P20-P24 **Note**	1.8 V< VDD < 5.5 V			-100	
	I_{OH3}	Per pin of P121-P124	4.0 V< VDD < 5.5 V			-1.0	mA
Output current, low	I_{OL1}	Per pin of P00-P06, P10-P17, P30-P33, P120	4.0 V< VDD < 5.5 V			8.5	mA
			2.7 V< VDD < 4.0 V			5.0	
			1.8 V< VDD < 2.7 V			2.0	
		Per pin of P60-P61	4.0 V< VDD < 5.5 V			15.0	mA
			2.7 V< VDD < 4.0 V			5.0	
			1.8 V< VDD < 2.7 V			2.0	
		Total of P00-P01, P120	4.0 V< VDD < 5.5 V			20.0	mA
			2.7 V< VDD < 4.0 V			15.0	
			1.8 V< VDD < 2.7 V			9.0	
		Total of P10-P17, P30-P33	4.0 V< VDD < 5.5 V			45.0	mA
			2.7 V< VDD < 4.0 V			35.0	
			1.8 V< VDD < 2.7 V			20.0	
		Total of all pins	4.0 V< VDD < 5.5 V			65.0	mA
			2.7 V< VDD < 4.0 V			50.0	
			1.8 V< VDD < 2.7 V			29.0	
	I_{OL2}	Per pin of P20-P24 **Note**	1.8 V< VDD < 5.5 V			400	uA
	I_{OL3}	Per pin of P121-P124	4.0 V< VDD < 5.5 V			1.0	mA
Input voltage, high	V_{IH1}	P12, P13, P15, P60-P61,P121-P124		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P10-P11, P14, P16-P17, P30-P33, P120, RESET_B		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P20-P24 **Note**		0.7AV_{REF}		AV_{REF}	V
Input voltage, high	V_{IH1}	P12, P13, P15, P60-P61,P121-P124		0		0.3V_{DD}	
	V_{IH2}	P00,P01, P10-P11, P14, P16-P17, P30-P33, P120, RESET_B		0		0.2V_{DD}	V
	V_{IH3}	P20-P24 **Note**		0		0.3AV_{REF}	V

Note When used as digital input ports, set $AV_{REF} = V_{DD}$. = LV_{DD}.

Caution This specification is Duty = 70% condition of I_{OH} and I_{OL}.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/3)

(TA = -40 to +85°C, 1.8V < VDD = LVDD < 5.5 V, VSS = LVSS = AVSS = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, high	I_{OH1}	I_{OH} = -3.0 mA	P00-P01, P10-P17, P30-P33, P120	4.0 V< VDD < 5.5 V	V_{DD}-0.7			V
		I_{OH} = -2.5 mA		2.7 V< VDD < 4.0 V	V_{DD}-0.5			
		I_{OH} = -1.0 mA		1.8 V< VDD < 2.7 V	V_{DD}-0.5			
	V_{OH2}	I_{OH} = -0.1 mA	P20-P24 P121-P124	1.8 V< VDD < 5.5 V $AV_{REF} = V_{DD} = LV_{DD}$	V_{DD}-0.5			V
Output voltage, low	V_{OL1}	I_{OL} = 8.5 mA	P00-P01, P10-P17, P30-P33, P120	4.0 V< VDD < 5.5			0.7	V
		I_{OL} = 1.0 mA		2.7 V< VDD < 4.0 V			0.5	
		I_{OL} = 0.5 mA		1.8 V< VDD < 2.7 V			0.4	
	V_{OL2}	I_{OL} = 0.4 mA	P20-P27* P121-P124	1.8 V< VDD < 5.5 V $AV_{REF} = V_{DD} = LV_{DD}$			0.4	V
	V_{OL3}	I_{OL} = 15 mA	P00-P01, P10-P17, P30-P33, P120	4.0 V< VDD < 5.5			2.0	V
		I_{OL} = 5.0 mA					0.4	V
		I_{OL} = 5.0 mA		2.7 V< VDD < 4.0 V				V
		I_{OL} = 2.0 mA		1.8 V< VDD < 2.7 V				V
Input leakage current, high	I_{LIH1}	$V_I = V_{DD} = LV_{DD}$	P00-P01, P10-P17, P30-P33, P120				1	µA
	I_{LIH2}	$V_I = AV_{REF}$	P20-P24				1	µA
	I_{LIH3}	$V_I = V_{DD} = LV_{DD}$	X1, X2, XT1, XT2 (When use External oscillator)				1	µA
Input leakage current, low	I_{LIL1}	$V_I = V_{SS} = LV_{SS}$	P00-P01, P10-P17, P30-P33, P120				-1	µA
	I_{LIL2}	$V_I = AV_{REF}$	P20-P24				-1	µA
	I_{LIL3}	$V_I = V_{SS} = LV_{SS}$	X1, X2, XT1, XT2 (When use External oscillator)				-1	µA
Pull-up resistance value	R_U	$V_I = V_{DD} = LV_{DD}$			10	20	100	kΩ
FLMD0 supply	V_{IL}	In normal operation mode			0		$0.2V_{DD}$	V
	V_{IH}	In flash memory programming mode			$0.8V_{DD}$		V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/3)
(TA = -40 to +85°C, 1.8V < VDD = LVDD < 5.5 V, VSS = LVSS = AVSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note1	I_{DD1}	Operation mode	f_{XH} = 20 MHz Note2, V_{DD} = 5.0 V		4.7	5.8	mA
			f_{XH} = 10 MHz Note2, V_{DD} = 5.0 V Note3		2.5	3.5	mA
			f_{XH} = 5 MHz Note2, V_{DD} = 3.0 V Note3		1.5	2.2	mA
			f_{RH} = 8 MHz Note2, V_{DD} = 5.0 V		1.9	2.7	mA
			f_{SUB} = 32.768 kHz Note2, V_{DD} = 5.0 V		17	T.B.D.	uA
	I_{DD2}	HALT mod	f_{XH} = 20 MHz Note2, V_{DD} = 5.0 V		2.2	2.6	mA
			f_{XH} = 10 MHz Note2, V_{DD} = 5.0 V Note3		1.0	1.2	mA
			f_{XH} = 5 MHz Note2, V_{DD} = 3.0 V Note3		0.55	0.65	mA
			f_{RH} = 8 MHz Note2, V_{DD} = 5.0 V		0.6	0.65	mA
			f_{SUB} = 32.768 kHz Note2, V_{DD} = 5.0 V		3.5	T.B.D.	uA
	I_{DD3}	STOP mode	V_{DD} = LV_{DD} = 5.0 V		1	20	uA
	I_{ADC}	A/D Converter operating current	A/D converter operating		0.57	1.3	mA
			A/D converter not operating		T.B.D.	T.B.D.	mA
	I_{WDT}	Watchdog Time operating current	240 kHz Ring-OSC operating		5	10	uA
	I_{LVI}	LVI operating current			9	T.B.D.	uA
Supply Current of LCD	ILCD1	Only When IIC operating	VDD = 5.0 V		150	300	uA
			VDD = 3.0 V		75	150	uA
	ILCD2	Only when LCD boost function is operating	VDD = 5.0 V		2	6	uA
			VDD = 3.0 V		1.5	6	uA
	ILCD3	When LCD is operating	VDD = 5.0 V		5	15	uA
			VDD = 3.0 V		4	12	uA
	ILCD4	When LCD stopped	VDD = 5.0 V		0.1	T.B.D	uA
			VDD = 3.0 V		0.05	T.B.D	uA

Notes
1. Total current flowing through the internal power supply (V_{DD}).
2. Input square-wave
3. When AMPH(OSCCTL.0) = 0.

Remark
1. f_{XH}: High-Speed System Clock oscillation frequency (X1 clock oscillation frequency or° External main system clock frequency).
2. f_{RH}: High-speed Ring-OSC oscillation frequency.
3. f_{SUB}: Subsystem Clock oscillation frequency (XT1 clock oscillation frequency or External° subsystem clock frequency).

AC Characteristics

(1) Basic operation

(TA = -40 to +85°C, 1.8V < VDD = LVDD < 5.5 V, VSS = LVSS = AVSS = 0 V)

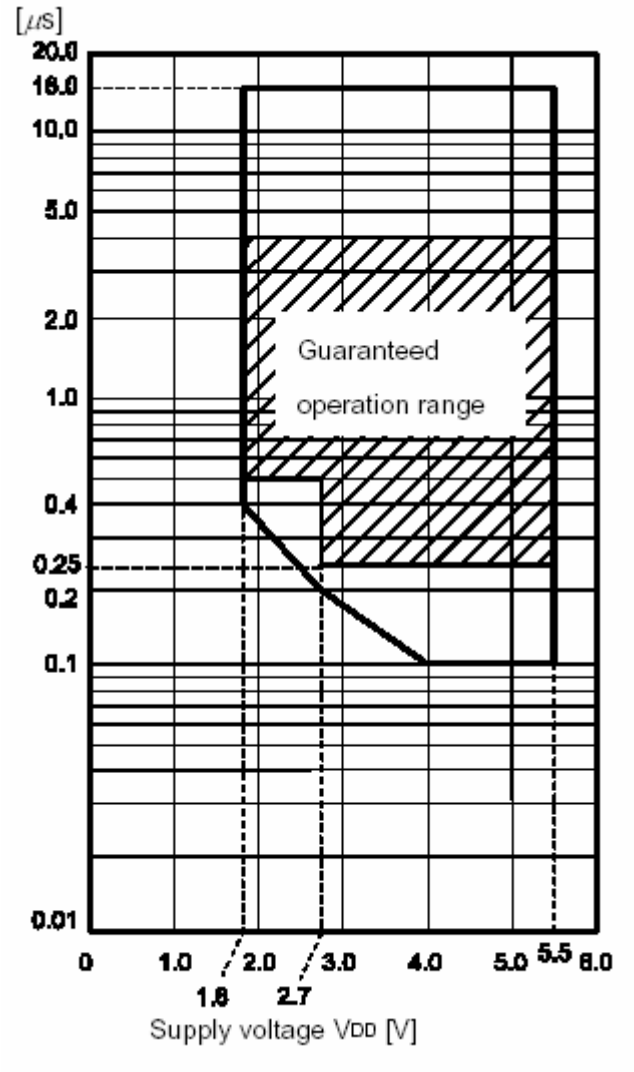
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock(f_{XP}) operation	High-speed system clock(f_{XH})	4.0 V< VDD < 5.5 V	0.1		16	uS
				2.7 V< VDD < 4.0 V	0.2		16	uS
				1.8 V< VDD < 2.7 V	0.4		16	uS
			High-speed Ring-OSC clock(f_{RH})	2.7 V< VDD < 5.5 V	0.25		4	uS
				1.8 V< VDD < 2.7 V	0.5		4	uS
		Subsystem clock(f_{SUB})operation			114	122	125	uS
External main system clock frequency	f_{EXCLK}	4.0 V< VDD < 5.5 V			2.0		20.0	MHz
		2.7 V< VDD < 4.0 V			2.0		10.0	MHz
		1.8 V< VDD < 2.7 V			2.0		5.0	MHz
External main system clock input high-/low-level width	t_{EXCLKH}, t_{EXCLKL}				(1/ f_{EXCLK} x 1/2) - 1			nS
External subsystem clock frequency	f_{EXCLKS}				32	32.768	35	kHz
External subsystem clock input high-/low-level width	$t_{EXCLKSH}$, $t_{EXCLKSL}$				(1/ f_{EXCLKS} x 1/2) - 5			nS
TI000, TI010, TI001, TI011 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	4.0 V< VDD < 5.5 V			$2/f_{sam}$ + 0.1**Note1**			nS
		2.7 V< VDD < 4.0 V			$2/f_{sam}$ + 0.2**Note1**			nS
TI50, TI51 input frequency	f_{TI5}	4.0 V< VDD < 5.5 V					10	MHz
		2.7 V< VDD < 4.0 V					10	MHz
		1.8 V< VDD < 2.7 V					5	MHz
TI50, TI51 input high-level width, low-level width	t_{TIH5}, t_{TIL5}	4.0 V< VDD < 5.5 V			50			nS
		2.7 V< VDD < 4.0 V			50			nS
		1.8 V< VDD < 2.7 V			100			nS
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}				1			uS
Key return input low-level Width	t_{KR}				250			nS
RESET low-level width	t_{RSL}				10 **Note2**			uS

Notes

1. Selection of $f_{sam} = f_{PRS}$, $f_{PRS}/4$, $f_{PRS}/256$ or f_{PRS}, $f_{PRS}/16$, $f_{PRS}/64$ is possible using bits 0 and 1 (PRM000, PRM001 or PRM010,PRM011) of prescaler mode register 00 and 01 (PRM00,PRM01). Note that when selecting the TI000 or TI001 valid edge as the count clock, $f_{sam} = f_{PRS}$.

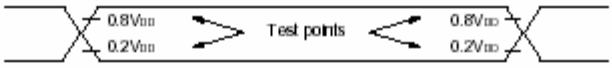
2. Input low level signal into RESET pin until power supply voltage is stabilized in the case of the power supply voltage rise time is slowly (more than 3.4ms).

TCY vs VDD (main system clock operation)

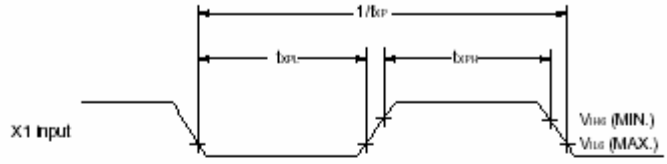


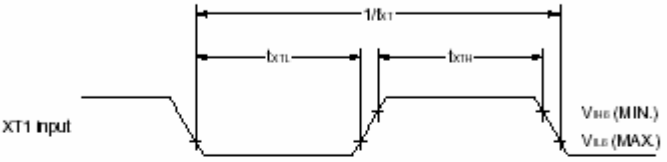
Remark The values indicated by the shaded section are only when the High-speed Ring-OSC clock is selected.

AC Timing Test Points (Excluding X1 Input)

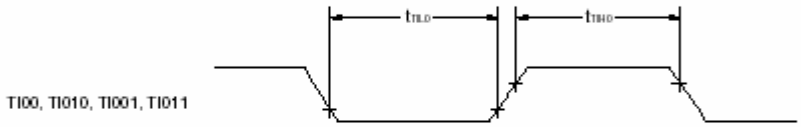


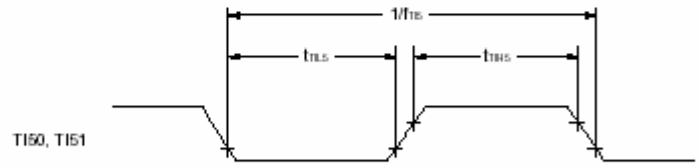
Clock Timing



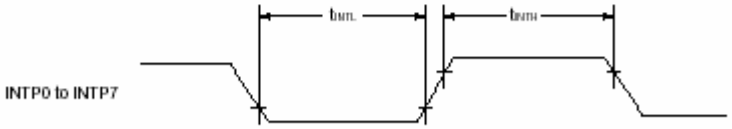


TI Timing

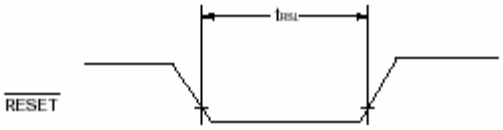




Interrupt Request Input Timing



RESET Input Timing



(2) Serial interface

(TA = -40 to +85°C, 1.8V < VDD = LVDD < 5.5 V, VSS = LVSS = AVSS = 0 V)

(a)UART mode (UART6, dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

(b) UART mode (UART0, dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

(c) IIC0 mode

Parameter	Symbol	Normal mode		High speed mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{CLK}	0	100	0	400	kbps
Start/restart condition setup time**Note1**	$t_{SU: STA}$	4.8		0.7		
hold time	$t_{HD: STA}$	4.1		0.7		
Hold time in SCL = ”L”	t_{LOW}	5.0		1.25		
Hold time in SCL = ”H”	t_{HIGH}	5.0		1.25		
Data setup time (reception)	$t_{SU: DAT}$	0		0		
Data hold time (sending)**Note2**	$t_{HD: DAT}$	0.47	4.0	0.23	1.0	

Notes

1. The first clock pulse is generated after this period in the case of the start/restart condition.

2. The MAX of $t_{HD:DAT}$ is normal transition value. Wait is occurred in the term of ACK(acknowledge) .

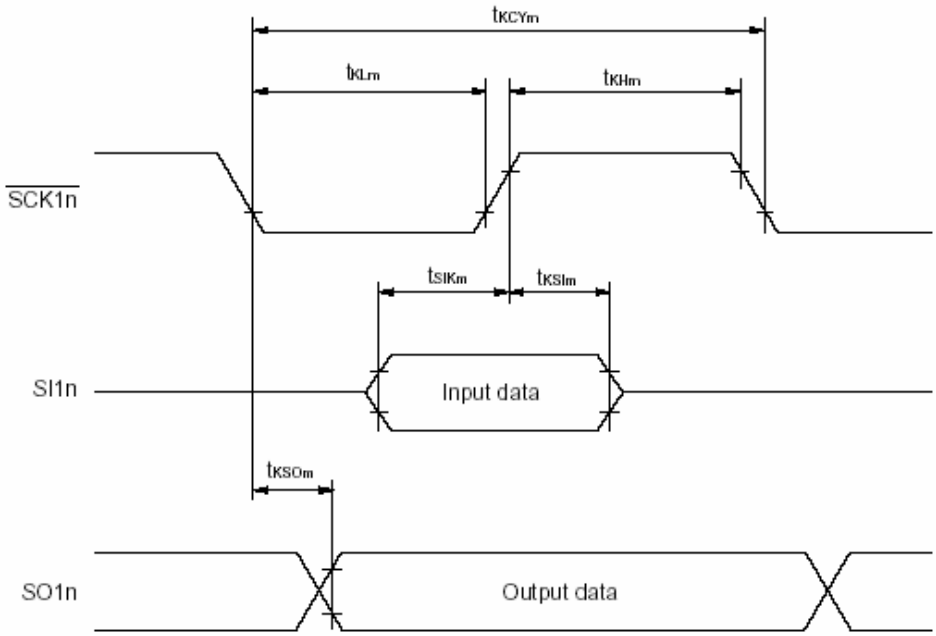
Caution Specification at 1.8 V ° V_{DD} < 2.7V is not fixed.

(d) 3-wire serial I/O mode (CSI10, CSI11 master mode, SCK1n…internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK1n cycle time t_{KCY1}	t_{KCY1}	4.0 V < V_{DD} < 5.5 V	100			ns
		2.7 V < V_{DD} < 4.0 V	200			ns
		1.8 V < V_{DD} < 2.7 V	400			
SCK1n high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 10$ Note1			ns
SI1n setup time (to SCK1n↑)	t_{SIK1}		30			ns
SI1n hold time (to SCK1n↑)	t_{KSI1}		30			ns
Delay time from SCK1n↓ to SO1n output	t_{KSO1}	C = 50 pF Note2			40	ns

Notes 1. This is the value when the high-speed system clock (f_{XH}) is operating.
2. C is the load capacitance of the SCK1n and SO1n output lines.

Serial Transfer Timing
3-wire serial I/O mode:



Remark m = 1, 2
n = 0, 1

A/D Converter Characteristics
(T_A = -40 to +85° C, 2.3 V<AV_{REF}<V_{DD} =EV_{DD} <V_{DD} = LV_{DD}, V_{SS} = LV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				10	Bit
Overall error Note1,2	AINL	4.0 V < V_{DD} < 5.5 V			±0.4	%FSR
		2.7 V < V_{DD} < 4.0 V			±0.6	%FSR
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Conversion time	tCONV	4.0 V < V_{DD} < 5.5 V	6.6		30	uS
		2.7 V < V_{DD} < 4.0 V	6.6		30	uS
		AV_{REF} < 2.7 V	11		T.B.D.	uS
Zero-scale error Note1,2	EZS	4.0 V < V_{DD} < 5.5 V			±0.4	%FSR
		2.7 V < V_{DD} < 4.0 V			±0.6	%FSR
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Full-scale error Note1,2	EFS	4.0 V < V_{DD} < 5.5 V			±0.4	%FSR
		2.7 V < V_{DD} < 4.0 V			±0.6	%FSR
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Integral linearity error Note1,2	ILE	4.0 V < V_{DD} < 5.5 V			±2.5	%FSR
		2.7 V < V_{DD} < 4.0 V			±4.5	%FSR
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Differential linearity error Note1,2	DLE	4.0 V < V_{DD} < 5.5 V			±1.5	%FSR
		2.7 V < V_{DD} < 4.0 V			±2.0	%FSR
		AV_{REF} < 2.7 V			T.B.D.	%FSR
Analog input voltage	VAIN		AVSS		AVREF	V

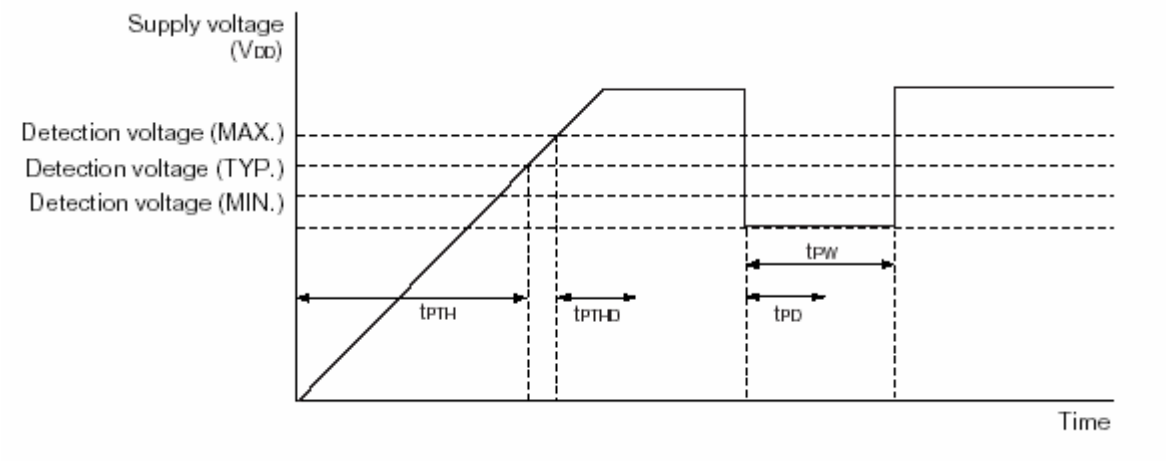
Notes
1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.

POC Circuit Characteristics (T_A = -40 to +85° C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOC		1.3	1.5	1.7	V
Power supply rise time	tPTH	V_{DD} : V_{POC} →1.8 V (MIN. value of V_{DD})		75	T.B.D	mV/ms
Minimum pulse width	tPW		T.B.D.	50		us

Notes
1. When voltage rises, time required from detection to reset release
2. When voltage drops, time required from detection to reset occur.

POC Circuit Timing



LVI Circuit Characteristics (T_A = -40 to +85° C)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.10	4.20	4.30	V
		V_{LVI1}		3.95	4.05	4.15	V
		V_{LVI2}		3.81	3.91	4.01	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.07	3.17	3.27	V
		V_{LVI8}		2.93	3.03	4.03	V
		V_{LVI9}		2.78	2.88	2.98	V
		V_{LVI10}		2.63	2.73	2.83	V
		V_{LVI11}		2.49	2.59	2.69	V
		V_{LVI12}		2.34	2.44	2.54	V
		V_{LVI13}		2.19	2.29	2.39	V
		V_{LVI14}		2.05	2.15	2.25	V
		V_{LVI15}		1.90	2.00	2.10	V
	External input pin**Note1**	EXLVI	EXLVI < V_{DD} = LV_{DD}		1.21		V
Minimum pulse width		t_{LW}		T.B.D.	50		us
Operation stabilization wait time **Note2**	T_{LWAIT1}				10	T.B.D.	us

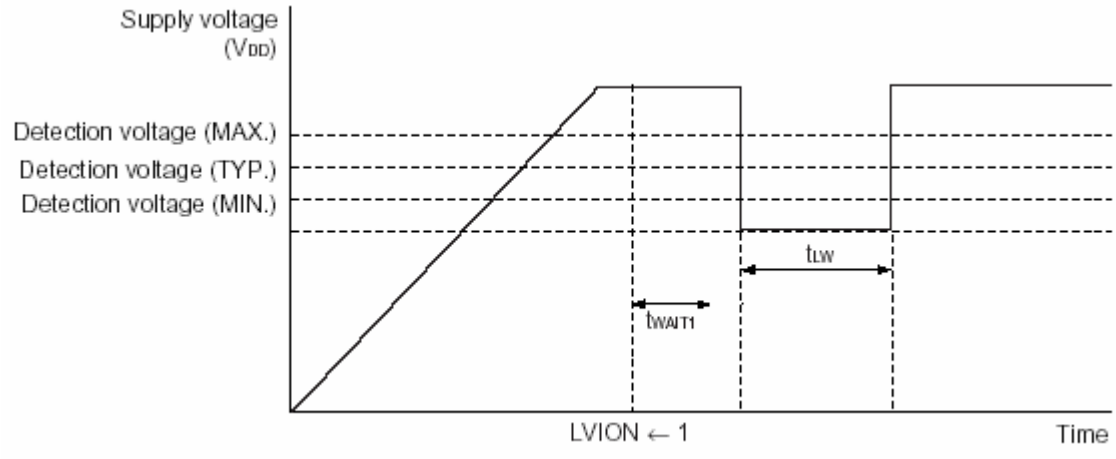
Note

1. Using EXLVI/P120/INTP0 pin

2. Time required from setting LVION to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1-15

LVI Circuit Timing



LCD

a) LCD Ladder type(T_A = -40 to +85°C , 2.0V<LVDD<5.5V)
(1) Static

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD power supply	VLCD		2.0		LVDD	V
LCD ladder resistance	RLCD		60.	100	150	kΩ
LCD output Deflection(COMON)	VODC	IO=+-5uA	0		+-0.2	V
LCD output Deflection(SEGMENT)	VODS	IO=+-1uA	0		+-0.2	V

(2) 1/3 bias

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD power supply	VLCD		2.5		LVDD	V
LCD ladder resistance	RLCD		60.	100	150	kΩ
LCD output Deflection(COMON)	VODC	IO=+-5uA	0		+-0.2	V
LCD output Deflection(SEGMENT)	VODS	IO=+-1uA	0		+-0.2	V

(3) 1/2 bias

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD power supply	VLCD		2.7		LVDD	V
LCD ladder resistance	RLCD		60.	100	150	kΩ
LCD output Deflection(COMON)	VODC	IO=+-5uA	0		+-0.2	V
LCD output Deflection(SEGMENT)	VODS	IO=+-1uA	0		+-0.2	V

a) LCD booster type(T_A = -40 to +85°C , 1.8V<LVDD<5.5V)

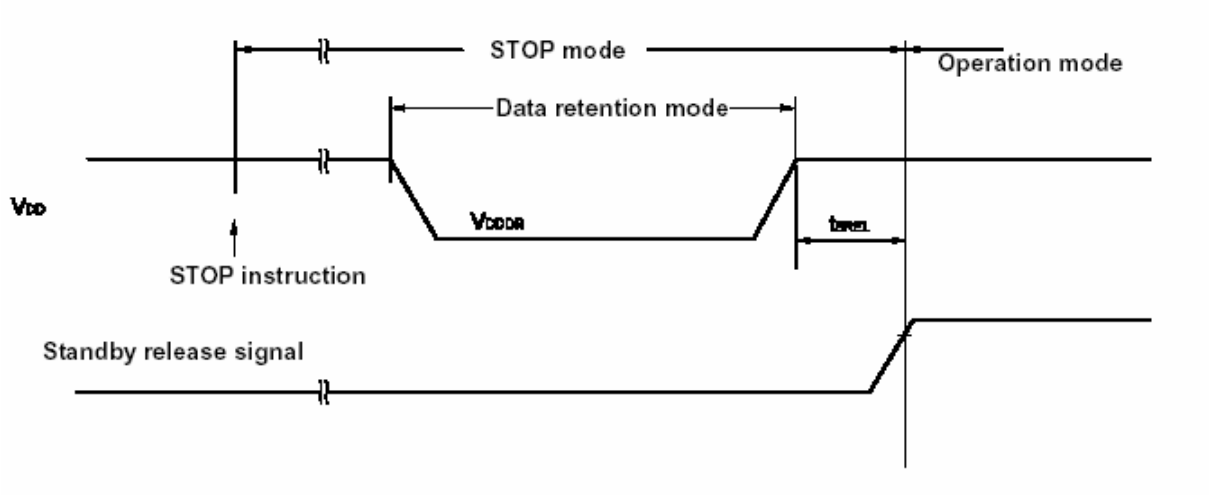
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage	VLCD2	C1-C4=0.47uF	GAIN=1	0.87	0.93	1	V
				0.94	1	1.06	V
				1	1.07	1.14	V
				1.16Note	1.13Note	1.2Note	V
			GAIN=1.5	1.35	1.43	1.51	V
				1.42	1.5	1.58	V
				1.48	1.57	1.66	V
				1.54	1.63	1.72	V
Two times voltage	VLCD1	C1-C4=0.47uF			2xVLCD2		
Three times voltage	LVCD2	C1-C4=0.47uF			3xVLCD2		
Booster wait time	tVAWAIT	GAIN=1	4.0 V < V_{DD} < 5.5 V	4			S
			2.7 V < V_{DD} < 4.0 V	0.5			S
		GAIN=1.5		0.5			S
LCD output resistor (COMMON)	RODC					40	kΩ
LCD output resistor (SEGMENT)	RODS					200	kΩ

Note 2.0V < LVDD <5.5V

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85° C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.3Note		5.5	V

Note Dependence on POC detection voltage. The data is held before POC reset, but is not held after POC reset when voltage drops.



Flash Memory Programming Characteristics

(1) Basic characteristics

(TA = -40 to +85°C, 2.7V < VDD = LVDD < 5.5 V, VSS = LVSS = AVSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}			4.5	11.0	mA
Erase time Note1	Chip unit	T_{eraca}			T.B.D	T.B.D	ms
	Sector unit	T_{erasa}			T.B.D	T.B.D	ms
Write time		T_{wrwa}			T.B.D	T.B.D	us
Number of rewrites per chip		C_{erwr}	1 erase + 1 write after erase = 1 rewrite Note2	T.B.D			time

Notes

1. The prewrite time before erasure and the erase verify time (writeback time) are not included.

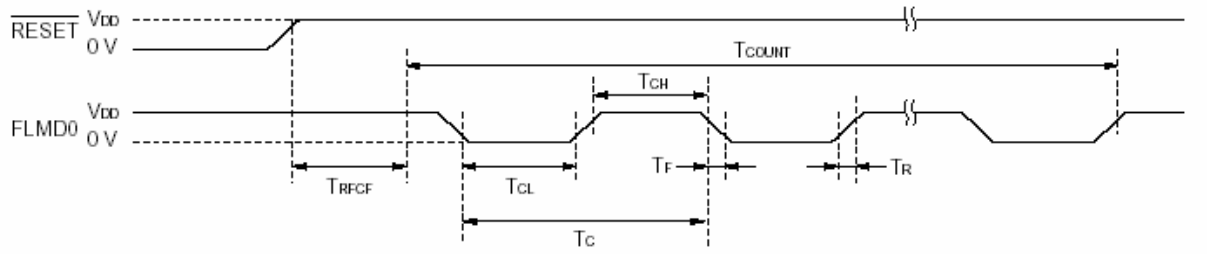
2. When a product is first written after shipment, "erase →° write" and "write only" are both taken as one rewrite.

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time from RESET↑ to FLMD0 count start	T_{RFCF}		4.1		17.1	mA
Count execution time	T_{COUNT}		10.8		13.2	ms
FLMD0 counter high-/low-level width	T_{CH}/T_{CL}		Tc x 0.45			us
FLMD0 counter rise/fall time	T_R/T_F		12.5			time

Remark These values may change after evaluation.

Serial Write Operation



NOTES FOR CMOS DEVICES

1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

2 HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3 PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4 STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5 POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.
The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6 INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.