HARRIS SEMICONDUCTOR

DG444, DG445

Monolithic, Quad SPST, CMOS Analog Switches

August 1997

Features

- ON-Resistance (Max) 85Ω
- Low Power Consumption (P_D) . . . . . <35µW)
- Fast Switching Action
  - t_{ON} . . . . . <250ns
  - t_{OFF} (DG444) . . . . . <120ns
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG444DJ	-40 to 85	16 Ld PDIP	E16.3
DG444DY	-40 to 85	16 Ld SOIC	M16.15
DG445DJ	-40 to 85	16 Ld PDIP	E16.3
DG445DY	-40 to 85	16 Ld SOIC	M16.15

Description

The DG444 and DG445 monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole single throw (SPST) analog switches and TTL and CMOS compatible digital inputs.

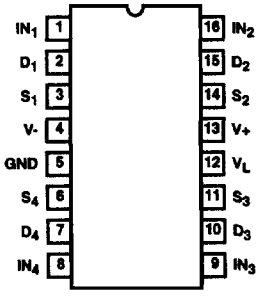
These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} <250ns) compared to the DG211 and DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG444 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling ±20V signals when operating with ±20V power supplies.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG444 and DG445 are identical, differing only in the polarity of the selection logic.

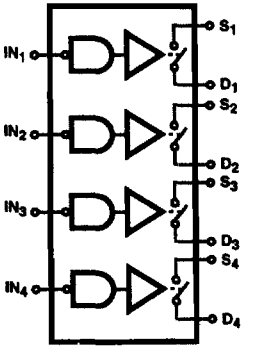
Pinout

DG444, DG445
(PDIP, SOIC)
TOP VIEW

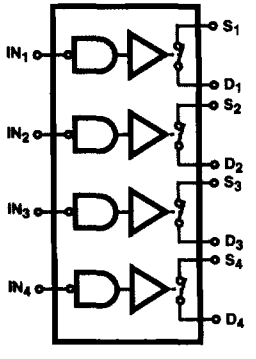


Functional Diagrams

DG444



DG445

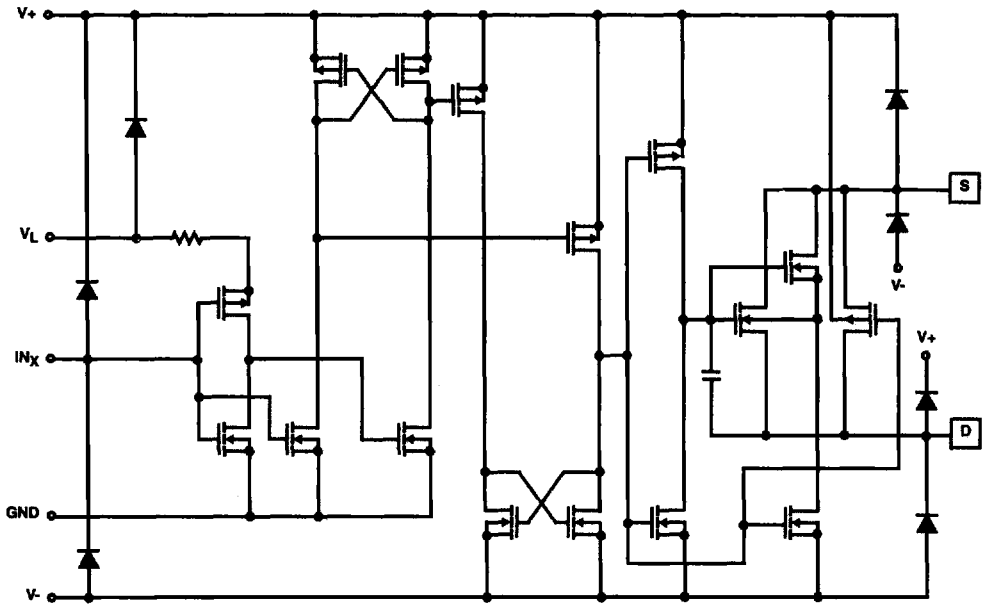


SWITCHES SHOWN FOR LOGIC "1" INPUT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3586.4**

Typical Schematic Diagram (One Channel)



Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L ..... (GND - 0.3V) to (V+) + 0.3V
Digital Inputs, V_S, V_D (Note 1) ..... (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle) 100mA

Operating Conditions

Temperature (D Suffix) ..... -40°C to 85°C
Voltage Range ..... ±20V (Max)
Temperature Range ..... -55°C to 125°C
Input Low Voltage ..... 0.8V (Max)
Input High Voltage ..... 2.4V (Min)
Input Rise and Fall Time ..... ≤20ns

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	115

Maximum Junction Temperature (PDIP, SOIC) ..... 150°C
Maximum Storage Temperature Range (D Suffix) ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:
1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V, (See Figure 18)	25	-	120	250	ns
Turn-OFF Time, t_{OFF}						
DG444		25	-	110	140	ns
DG445		25	-	160	210	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, V_{GEN} = 0V, R_{GEN} = 0Ω	25	-	-1	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	60	-	dB
Crosstalk (Channel-to-Channel)	Any Other Channel Switches R_L = 50Ω, C_L = 5pF, f = 1MHz	25	-	100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz	25	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz	25	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$	V_{ANALOG} = 0	25	-	16	-	pF
DIGITAL CONTROL						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = ∓10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	25	-	50	85	Ω
		Full	-	-	100	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	25	-0.5	0.01	0.5	nA
		Hot	-5	-	5	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V $V_S = V_D = \pm 15.5V$	25	-0.5	0.08	0.5	nA
		Hot	-10	-	10	nA
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	25	-	0.001	1	µA
		Hot	-	-	5	µA
Negative Supply Current, I-		25	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		25	-	0.001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		25	-1	-0.001	-	µA
		Hot	-5	-	-	µA

Electrical Specifications (Unipolar Supplies) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = 8V, (See Figure 18)	25	-	300	450	ns
Turn-OFF Time, t_{OFF}		25	-	60	200	ns
Charge Injection, Q	C_L = 1nF, V_{GEN} = 6V, R_{GEN} = 0Ω	25	-	2	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = -10mA, V_D = 3V, 8V V+ = 10.8V, V_L = 5.25V	25	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 13.2V, V_{IN} = 0V or 5V	25	-	0.001	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-	V_{IN} = 0V or 5V	25	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L	V_L = 5.25V, V_{IN} = 0V or 5V	25	-	0.001	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}	V_{IN} = 0V or 5V	25	-1	-0.001	-	µA
		Full	-5	-	-	µA

NOTES:

3. V_{IN} = Input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Performance Curves

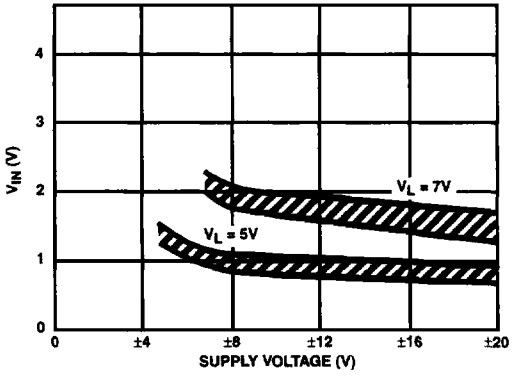


FIGURE 1. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

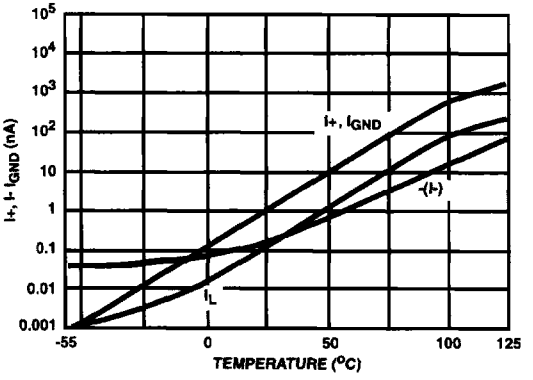


FIGURE 2. SUPPLY CURRENT vs TEMPERATURE

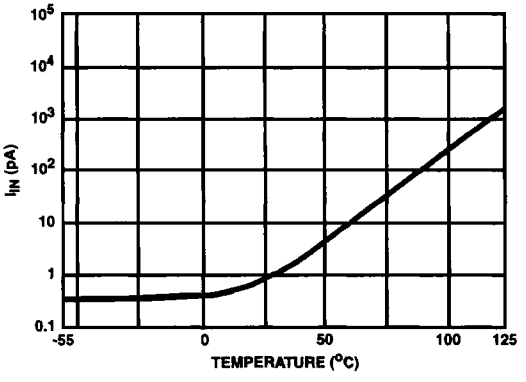


FIGURE 3. INPUT CURRENT vs TEMPERATURE

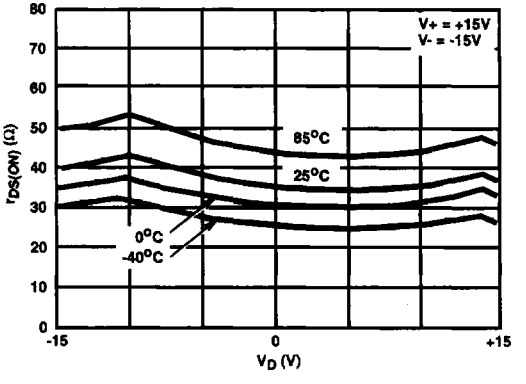


FIGURE 4. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

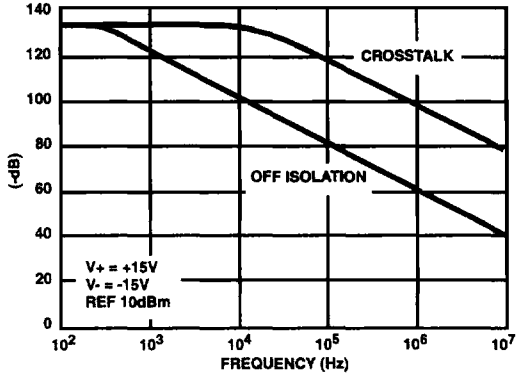


FIGURE 5. CROSSTALK AND OFF ISOLATION vs FREQUENCY

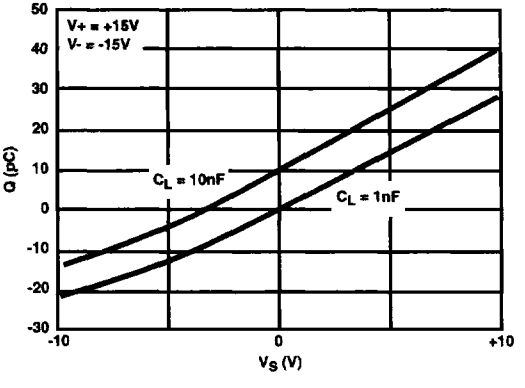


FIGURE 6. CHARGE INJECTION vs SOURCE VOLTAGE

Typical Performance Curves (Continued)

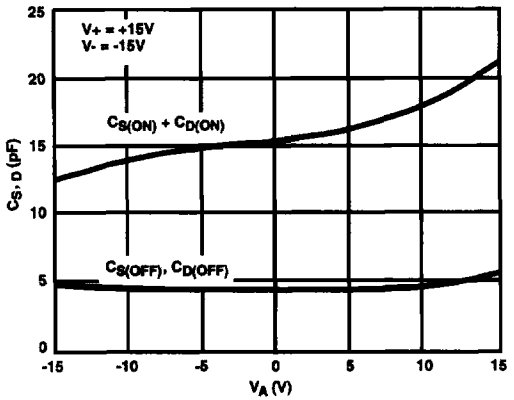


FIGURE 7. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

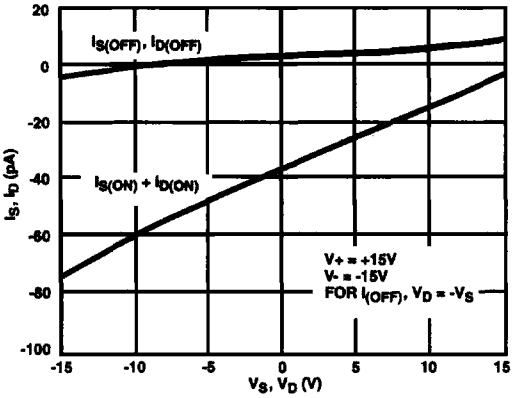


FIGURE 8. SOURCE/DRAIN LEAKAGE CURRENTS

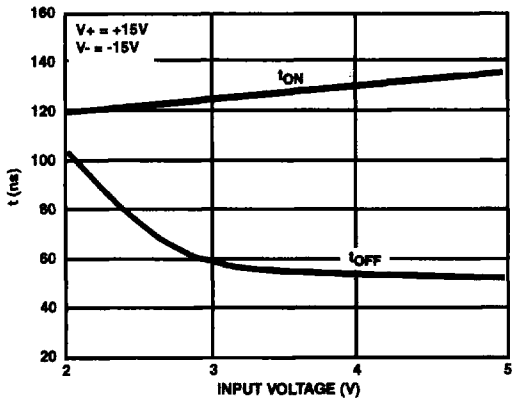


FIGURE 9. SWITCHING TIME vs INPUT VOLTAGE

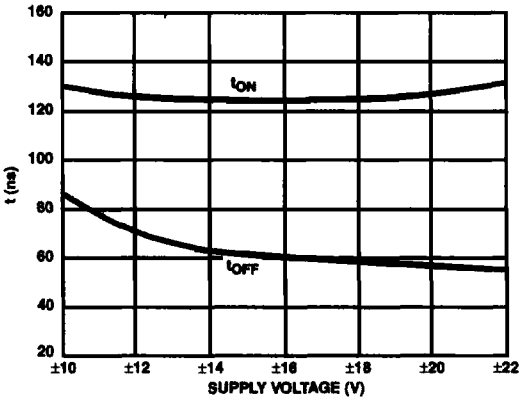


FIGURE 10. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG444)

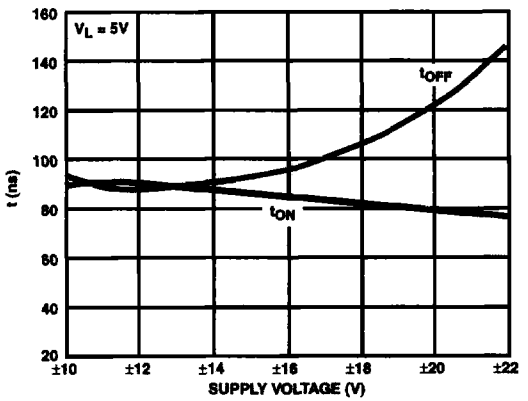


FIGURE 11. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG445)

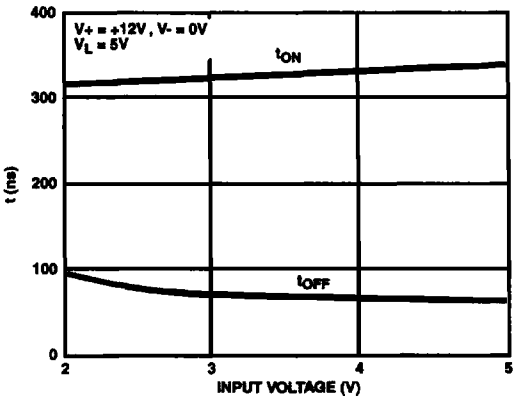


FIGURE 12. SWITCHING TIME vs INPUT VOLTAGE (DG444)

Typical Performance Curves (Continued)

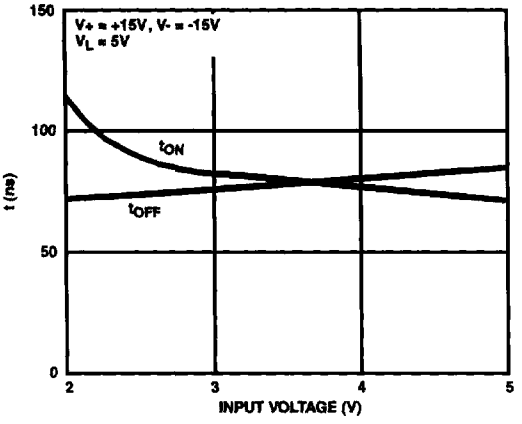


FIGURE 13. SWITCHING TIME vs INPUT VOLTAGE (DG445)

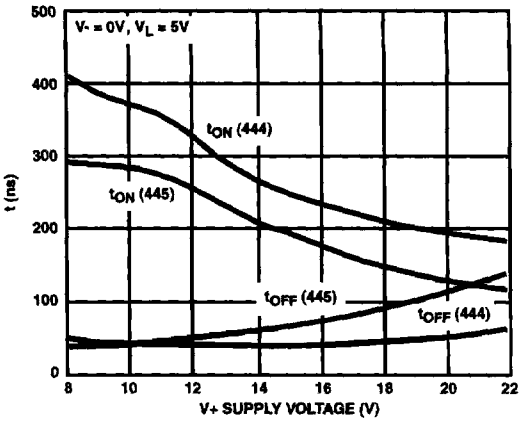


FIGURE 14. SWITCHING TIMES vs POWER SUPPLY VOLTAGE

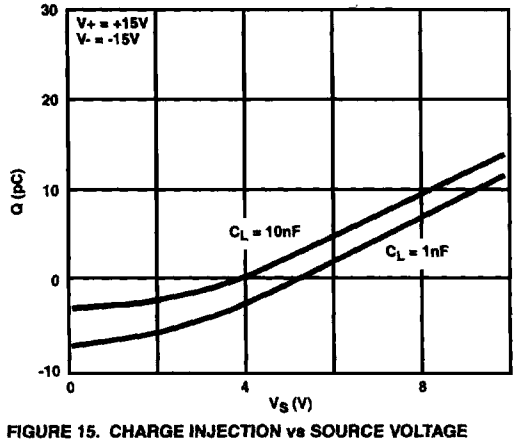


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE (SINGLE 12V SUPPLY)

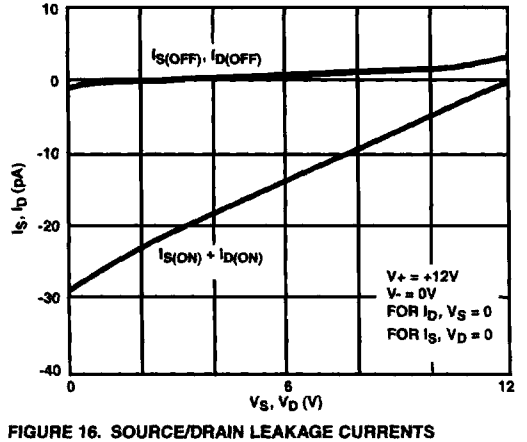


FIGURE 16. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

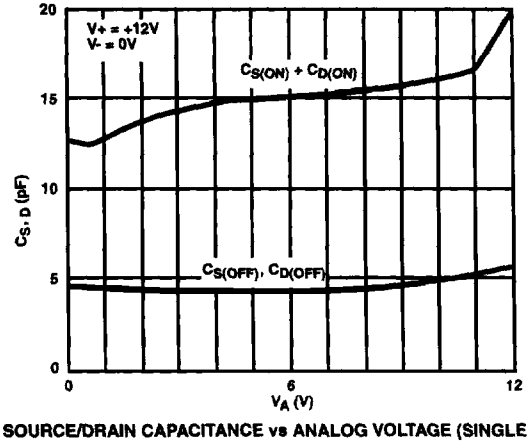


FIGURE 17. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

Pin Descriptions

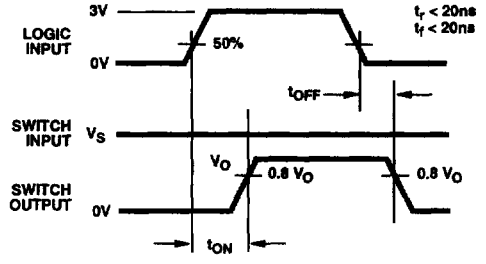
PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	V_L	Logic Reference Voltage.
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

TRUTH TABLE

LOGIC	V_{IN}	DG444	DG445
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

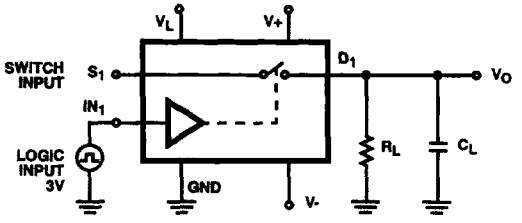
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 18A.



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

FIGURE 18. SWITCHING TIME

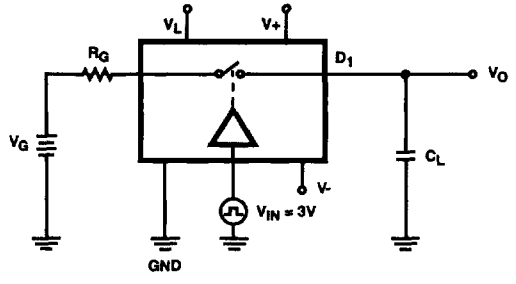


FIGURE 19A.

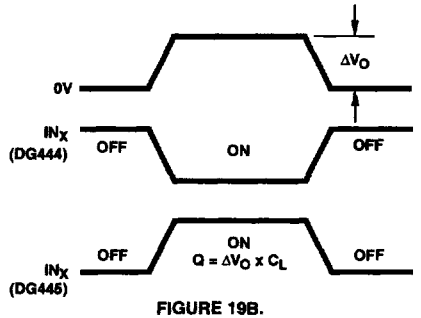


FIGURE 19B.

FIGURE 19. CHARGE INJECTION

13 SWITCHES

Test Circuits and Waveforms (Continued)

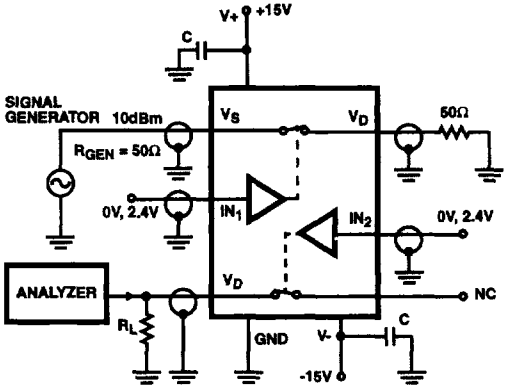


FIGURE 20. CROSSTALK

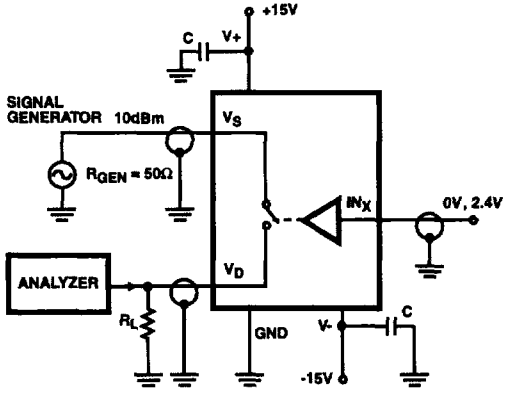


FIGURE 21. OFF ISOLATION

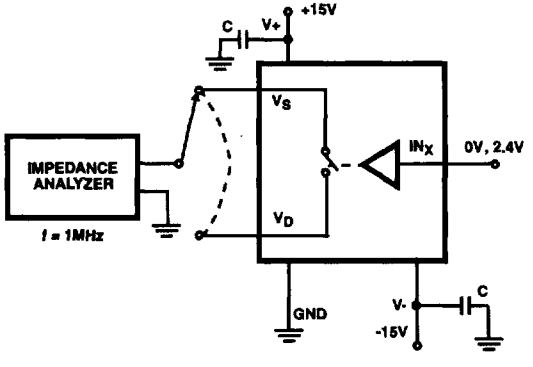
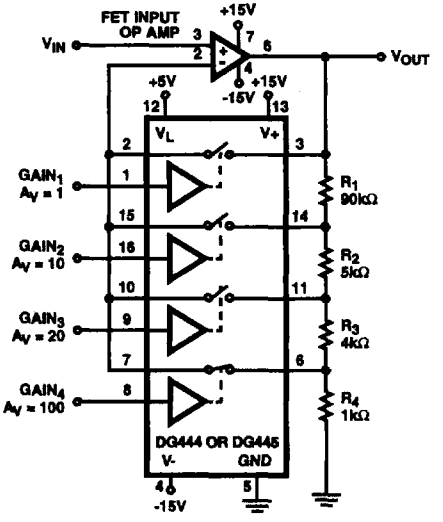


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Typical Applications



GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE, OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OR CIRCUIT

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW_4 CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

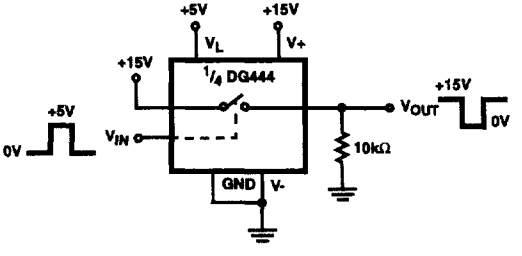


FIGURE 24. LEVEL SHIFTER

Die Characteristics

DIE DIMENSIONS:

2160µm x 1760µm x 485 ±25µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG444, DG445