DA7211

Ultra-Low Power Stereo Codec

General Description

DA7211 features a high fidelity and powerful 72 mW per channel headphone amplifier. The device may be operated from a single 1.8 V supply. Total device consumption is only 2.5 mW which helps extend music playback time for battery operated equipment.

The fully integrated fractional PLL has been designed to use minimal power while supporting a wide range of input and output frequencies. Internal suppression circuits help maintain audio synchronisation in the presence of system noise on the external clock.

Six analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimise the dynamic range prior to digitisation. This provides hardware support for ambient noise cancellation.

The DA7211 provides two volume-controlled differential/single-ended stereo line-out drivers and ground-centred stereo amplifiers to directly drive standard 3-wire 16 Ω headphones. For example the dc coupled, dedicated pop-free drivers may be connected simultaneously to stereo headphones, stereo speakers and a mono line out without external switches.

All filtering functions are performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters. A configurable signal processing engine allows various audio enhancements and effects such as acoustic filtering, transducer equalisation, wind noise suppression and 3D sound

The multi-slot I2S/PCM interface supports all common sample rates between 8 and 96 kHz in master or slave mode operation.

Key Features

- Stereo multi-bit Delta Sigma DAC with SNR 100 dB ('A' weighted @ 48 kHz)
- Stereo multi-bit Delta Sigma ADC with SNR 96 dB ('A' weighted @ 48 kHz)
- Ultra low-power stereo headphone driver with
  - Stereo DAC to HP playback power: 2.5 mW
  - 2x58 mW output power (16 Ω)
  - ‘Capless’ output via GND centred signals
  - Four level charge pump with continuous tracking of audio signal (Class G)
  - Short circuit protection
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 and 96 kHz sample rates
- On-chip PLL with signal shaper and audio Sample Rate Matching
- 2-wire software control interface
- Audio serial data bus supports I2S, left/right justified, DSP and TDM modes
- Stereo or mono differential microphone interface
- Programmable ultra-low noise bias supply for electret microphones
- Volume controlled stereo auxiliary inputs and outputs supporting FM Radio and fixed gain speaker amplifiers
- Multi-mode audio routing and mixers
- Pop & click suppression circuitry
- ASSP DSP filter engine for digital audio enhancements (acoustic filtering, wind noise suppression, 5-band equaliser, 3D sound, automatic gain control)
- Supports supply from single voltage (1.8/2.5 V)
- Extensive modular power control
- Package: 36 bump WL-CSP 3x3 – 0.5 mm pitch

Applications

- Personal media players
- Portable consumer devices
- Music handsets
- Personal navigation devices

Contents

Figures

Tables

1 Terms and Definitions

ADC	Analogue to Digital Converter
ALC	Automatic Level Control
ASSP	Application Specific Standard Product
DAC	Digital to Analogue Converter
DAI	Digital Audio Interface
DMIC	Digital microphone
DSP	Digital Signal Processor or Digital Signal Processing
FIR	Finite Impulse Response (Filter)
I2C	Inter-Integrated Circuit interface
I2S	Inter-IC Sound
IIR	Infinite Impulse Response (Filter)
GP	General Purpose (Filter)
LDO	Low Dropout regulator
MCLK	Master Clock
PCM	Pulse Code Modulation
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
RDL	Redistribution Layer
RC	Resistance-Capacitance
SC	System Controller
SDM	Sigma Delta Modulator
SNR	Signal to Noise Ratio
SRM	Sample Rate Matching
TDM	Time Division Multiplexing
THD+N	Total Harmonic Distortion plus Noise
VCO	Voltage-Controlled Oscillator
WL-CSP	Wafer Level-Chip Scale Packaging

2 Block Diagram

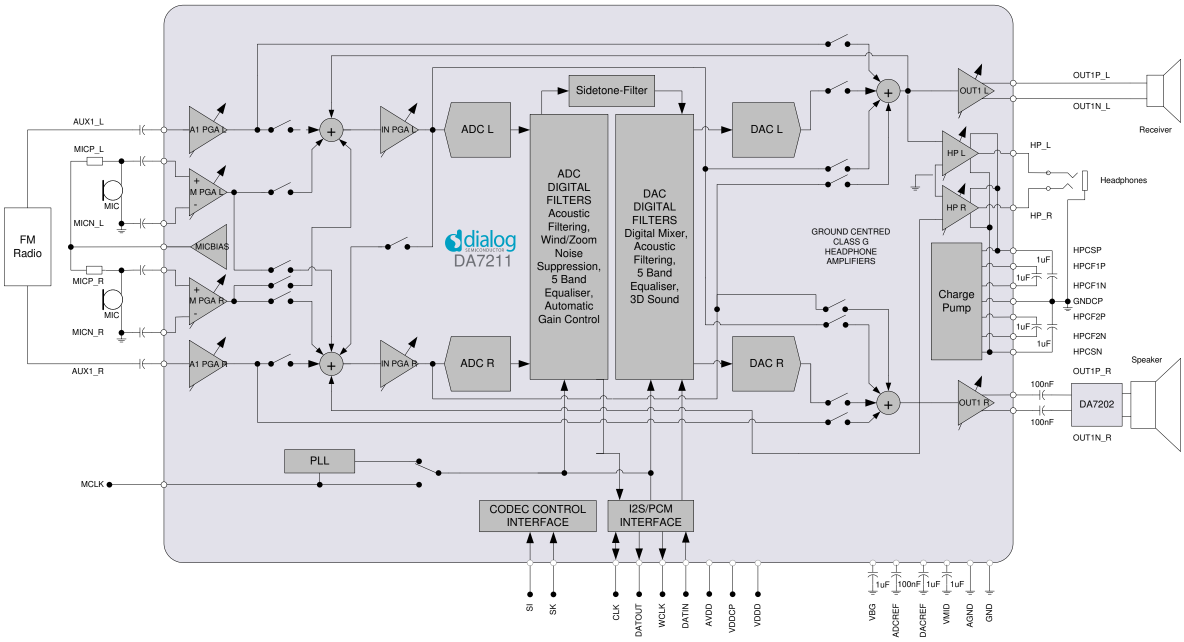


Figure 1: DA7211 Block Diagram

3 Pinout

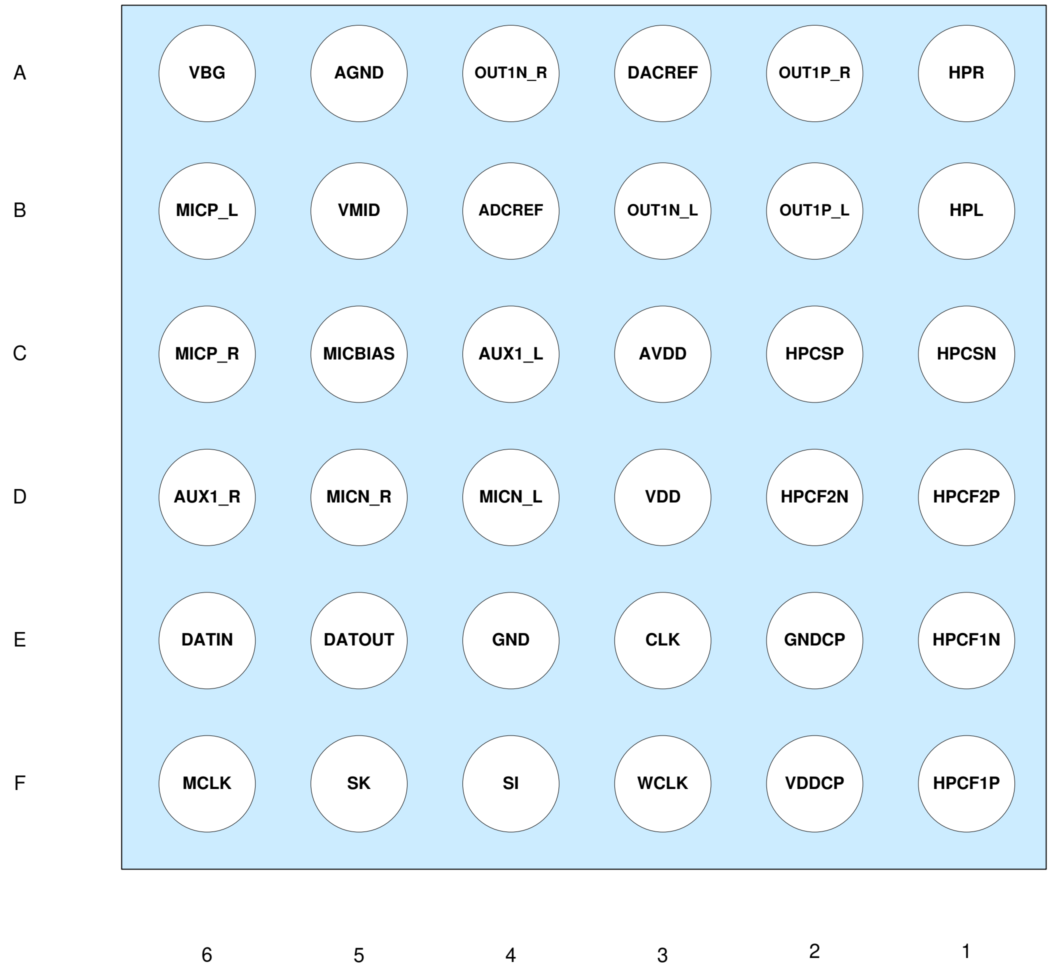


Figure 2: DA7211 Pad Arrangement (Bottom Eiew Ball Side Up)

Table 1: Pin Description

Pin no.	Pin Name	Description
5A	AGND	Analogue ground
3C	AVDD	Analogue supply
3D	VDD	Digital and input supply
4C	AUX1_L	Left channel single-ended auxiliary input
6B	MICP_L	Left channel differential microphone +ve input
4D	MICN_L	Left channel differential microphone –ve input
5C	MICBIAS	Current supply for microphone
6C	MICP_R	Right channel differential microphone +ve input

Pin no.	Pin Name	Description
5D	MICN_R	Right channel differential microphone -ve input
6D	AUX1_R	Right channel single-ended auxiliary input
6F	MCLK	Master clock input (reference to PLL)
6E	DATIN	I2S digital data input
5E	DATOUT	I2S digital data output
5F	SK	Digital clock for 2-wire
4F	SI	2-wire input and open drain output
3E	CLK	Digital bit clock for I2S
3F	WCLK	Digital word clock for I2S
2F	VDDCP	Headphone charge pump supply
1F	HPCF1P	Head phone amp charge pump floating cap1 +ve
1E	HPCF1N	Head phone amp charge pump floating cap1 –ve
2E	GNDCP	Headphone and digital ground
1D	HPCF2P	Head phone amp charge pump floating cap2 +ve
2D	HPCF2N	Head phone amp charge pump floating cap2 –ve
1C	HPCSN	Head phone amp charge pump storage cap –ve
2C	HPCSP	Head phone amp charge pump storage cap +ve
1B	HPL	Left head phone amp output
1A	HPR	Right head phone amp output
4E	GND	Ground bump
3A	DACREF	Decoupling capacitor for DAC
2A	OUT1P_R	Differential or single ended +ve line out right
4A	OUT1N_R	Differential –ve line out right
2B	OUT1P_L	Differential or single ended +ve line out left
3B	OUT1N_L	Differential –ve line out left
4B	ADCREF	Decoupling capacitor for ADC
5B	VMID	Decoupling capacitor for VMID
6A	VBG	Decoupling capacitor for VBG

3.1 The 36-Ball DA7211 Device

The VDDIO and the digital core supplies are joined in the RDL layer, so the internal LDO is unusable and should remain disabled. Separating the digital supply voltages from the AVDD allows a digital supply as low as 1.2 V to be used.

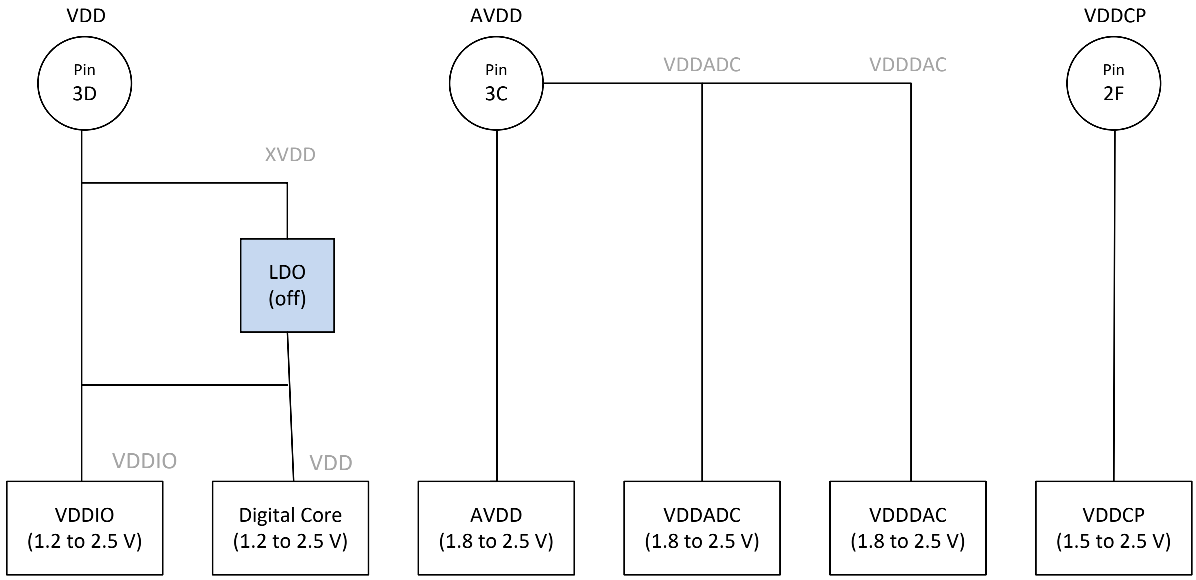


Figure 3: DA7211 Power Supply Topology

4 Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
	Storage temperature		-40	+95	°C
Ta	Operating temperature		-40	+85	°C
AVDD VDDCP	Power Supply Input		-0.3	2.75	V
	Supply voltage all input pins except power		-0.3	AVDD+ 0.3	V
	Maximum power dissipation			200	mW
	Package thermal resistance			40	k/W
	ESD susceptibility	Human body model		2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Operating temperature		-40		+85	°C
VDD	Supply voltage digital and I/O	Min and max values can accept +/-5% tolerances	1.2		2.5	V
AVDD	Supply voltage analogue	Min and max values can accept +/-5% tolerances	1.8		2.5	V
VDDCP	Supply voltage headphone	Max value can accept +/-5% tolerances	1.8		2.5	V

6 Electrical Characteristics

Table 4: Power Dissipation

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
	All registers at default values	Powerdown		6		µA
	Digital playback to lineout	DACL/R to OUT1L/R		3.15		mW
	Digital playback to HP no load	DACL/R to HPL/R quiescent		2.54		mW
	Digital playback to HP with load	DACL/R to HPL/R 16 Ω load 0.1 mW		4.66		mW
	Analogue bypass to lineout	AUX1L/R to OUT1L/R		2.87		mW
	Analogue bypass to HP no load	AUX1L/R to HPL/R quiescent		2.43		mW
	Analogue bypass to HP with load	AUX1L/R to HPL/R 16 Ω load 0.1 mW		4.57		mW
	Microphone stereo record	MICL/R to ADCL/R		2.38		mW
	Mic one channel record and digital playback to lineout	MICR to ADCR		3.10		mW
	Mic stereo record and digital playback to HP no load	MICL/R to ADCL/R and DACL/R to HPL/R quiescent		4.35		mW
	Mic stereo record and digital playback to HP with load	MICL/R to ADCL/R and DACL/R to HPL/R 16 Ω load 0.1 mW		6.49		mW

Note 1 SC_CLK_DIS, 0x03[7] = 1 for all measurements
VMID_BUFF_EN, 0x96[2:0] = 000 for all modes not using DAC
AVDD and VDDCP = 1.8 V. Internal regulator configured for 1.2 V, 0xB7 [5:4] = 11

Table 5: Power Consumption Figures 1

AVDD and VDDCP = 1.8 V (Note 1)

DA7211	Current (mA)			Power (mW)			
	AVDD 1.8 V	VDDC P 1.8 V	VDD 1.2 V	AVDD	VDDC P	VDD	Total
Powerdown	0.005	0	0.006	0.009	0	0.007	0.016
DACL/R to HPL/R quiescent no load Class G On	0.303	0.191	0.686	0.545	0.344	0.823	1.712
DACL/R to HPL/R 16 Ω load 0.1 mW Class G On	0.336	1.357	0.726	0.605	2.443	0.871	3.918
DACL/R to HPL/R "Love Comes Around" 16 Ω	0.298	0.279	0.731	0.536	0.503	0.877	1.915
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC	0.331	0.365	0.84	0.595	0.657	1.008	2.26
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & PLL	0.762	0.365	1.13	1.372	0.657	1.356	3.385
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & MICBIAS (2 k load,1.5 V) & PLL	0.776	0.365	1.13	1.397	0.657	1.356	3.41

Table 6: Power Consumption Figures 2

AVDD and VDDCP = 2.5 V (Note 1)

DA7211	Current (mA)			Power (mW)			
	AVDD 2.5 V	VDDC P 2.5 V	VDD 1.2 V	AVDD	VDDC P	VDD	Total
Powerdown	0.303	0.204	0.685	0.758	0.509	0.822	2.089
DACL/R to HPL/R quiescent no load Class G On	0.336	1.416	0.724	0.839	3.54	0.869	5.248
DACL/R to HPL/R 16 Ω load 0.1 mW Class G On	0.306	0.306	0.728	0.765	0.764	0.874	2.403
DACL/R to HPL/R "Love Comes Around" 16 Ω	0.311	0.3	0.833	0.777	0.75	1	2.527
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC	0.824	0.298	1.01	2.06	0.745	1.212	4.017
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & PLL	0.832	0.298	1.003	2.08	0.745	1.204	4.029
DACL/R to HPL/R "Love Comes Around" 16 Ω & MIC2ADC & MICBIAS (2 k load,1.5 V) & PLL	0.303	0.204	0.685	0.758	0.509	0.822	2.089

Note 1 Corinne Bailey Rae, 'Love Comes Around' 44.1 kHz, volume referenced to a 0.1 mW sine wave. The gain from a pure sine wave input is adjusted to give 0.1 mW output. Power consumption measurements are then made while playing the music track played at the same volume.

Test conditions: VDD=2.5 V, Ta=25°C, fs=48 kHz, 24-bit audio data unless specified otherwise.

Table 7: Electrical Characteristics: Microphone Bias

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BIAS}	Bias Voltage	No load, AVDD = 2.5 V No load, AVDD = 1.8 V	2.2 1.5	Pro-grammable	2.3 1.6	V
I_{BIAS}	Maximum Current	Voltage drop < 50 mV		2		mA
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 50			dB
V_N	Output Noise Voltage			5		µV_{RMS}
	Capacitive Load	I_{BIAS} < 100 µA, 100 µA < I_{BIAS} < 2 mA		100 200		pF

Table 8: Electrical Characteristics: Input Mixing Units

(MICP_L, MICN_L, AUX_L, MICP_R, MICN_R, AUX1_R)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Input Signal	single-ended differential MIC-PGA=0 dB IN-PGA=0 dB		0.8*AVDD 1.6*AVDD		V_{PP}
R_{IN}	Input resistance	Mic, single-ended AUX1	12 6	15 variable	18 40	kΩ
	Frequency Response	+/- 0.5 dB	20		20k	Hz
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain Note 1	MIC-PGA AUX1-PGA IN-PGA	-6 -48 -4.5		24 21 18	dB
	Programmable Gain Step Size	MIC-PGA AUX1-PGA, IN-PGA		6 1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-1.0		1.0	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
V_{NOISE}	Input Noise Level	Inputs connected to GND A-weighting input referred, measured @ ADC output Mic (Gain = 42 dB) AUX1 (Gain = 21 dB)		5 6.5		µV_{RMS}
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz, single-ended input	80 70			dB

Note 1 The gain describes the ratio of input and output signal level at the related amplifier stage (independent of whether the connection is single ended or differential).

Table 9: Electrical Characteristics: Analogue to Digital Converter (ADC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Input Signal	Corresponding digital level 0 dBFS		1.6* AVDD		V_{PP}
SNR	Signal to Noise Ratio	A-weighting, no input selected		96		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS		-89		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 32 kHz PLL mode		-80		dB
	Channel separation			90		dB
B_{PASS}	Pass band				0.45*fs	kHz
B_{STOP}	Stop band	fs ≤ 48 kHz fs = 88.2/96 kHz	0.56*fs		7*fs 3.5*fs	kHz
	Pass band Ripple	Voice Mode Music Mode			+/-0.3 +/-0.1	dB
	Stop band Attenuation	Voice Mode Music Mode	70 55			dB
	Group delay	Voice Mode Music Mode (Note 1) fs= 88.2/96 kHz		4.3/fs 18/fs 9/fs	600	µs
	Group delay mismatch	Between left and right channel			2	µs
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	80 70			dB

Note 1 5-band-equaliser disabled.

Table 10: Electrical Characteristics: Digital to Analogue cConverter (DAC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Output Signal	Corresponding digital level 0 dBFS		1.6*AV DD		V_{PP}
SNR	Signal to Noise Ratio	A weighting		102		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS		-85		dB
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 32 kHz PLL mode		-80		dB
	Channel separation			90		dB
B_{PASS}	Pass band				0.45*fs	kHz
B_{STOP}	Stop band	fs ≤ 48 kHz fs = 88.2/96 kHz	0.56*fs		7*fs 3.5*fs	kHz
	Pass band Ripple	Voice Mode Music Mode			±0.15 ±0.1	dB
	Stop band Attenuation	Voice Mode Music Mode	70 55			dB
	Group delay	Voice Mode Music Mode fs = 88.2/96 kHz		4.8/fs 18.5/fs 9/fs	650	µs
	Group delay variation	20 Hz to 20 kHz			1	µs
	Group delay mismatch	Between left and right channel			2	µs
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 60			dB

Table 11: Electrical Characteristics: Line Out and Receiver Amplifier

(OUT1P_L, OUT1N_L, OUT1P_R, OUT1N_R)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Input Signal	No load, single-ended No load, differential		0.8*AVDD 1.6 *AVDD		V_{PP}
	Load Impedance	single-ended output mode	500	2k	 1 200	Ω µH pF
		differential output mode	25	32	 1 200	Ω µH pF
	Frequency Response	+/- 0.5 dB	20		20k	Hz
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain		-54		15	dB
	Mute Attenuation			100		dB
	Programmable Gain Step Size			1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-0.8		0.8	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
	Signal to Noise Ratio	A weighting		102		dB
V_{NOISE}	Output Noise Level	20 - 20 kHz, unweighted gain < -15 dB single-ended differential		 <5.5 <4.5		µV
THD+N	Total Harmonic Distortion Plus Noise	-1 dBFS, 44.1 kHz slave mode non A-weighting		-90		
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz single-ended output	70 47			dB
		20 Hz - 2 kHz 2 kHz - 20 kHz differential output	90 70			dB

Table 12: Electrical Characteristics: Dynamic Charge Pump

(HPCSP, HPCSN)

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDDCSP	Positive dynamic supply voltage	Positive dynamic supply voltage		VDDCP VDDCP/2 (VDDCP/3, VDDCP/4)		
VDDCSN	Negative dynamic supply voltage	Negative dynamic supply voltage		-VDDCP -VDDCP/2 (-VDDCP/3, -VDDCP/4)		
	Floating capacitors			1.0		µF
	Storage capacitors			1.0		µF

Table 13: Electrical Characteristics: Headphone Amplifier

(HPL, HPR)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale Output Signal	No load		1.6*VDD CP		V_{PP}
	DC output offset			100		µV
P_{MAX}	Output Power per channel	VDDCP = 1.8 V, THD < 0.1%, R_L=16 Ω 1 kHz	25	30		mW_{RMS}
		VDDCP = 2.5 V, THD < 0.1%, R_L=16 Ω 1 kHz	50	58		mW_{RMS}
	Dynamic internal supply voltages	VDD/3 or VDD/4 can optionally be selected if two flying caps are available		±VDD ±VDD/2 (±VDD/3 (±VDD/4)		
IQ	Quiescent current per channel	from VDDCP		100		uA
	Load Impedance	13 < R_L < ∞	13	16	 400 500	Ω µH pF
	Frequency Response	+/- 0.5 dB	20		20k	
	Amplitude Ripple	20 Hz – 20 kHz	-0.5		0.5	dB
	Programmable Gain		-54		15	dB
	Mute Attenuation			100		dB
	Programmable Gain Step Size			1.5		dB
	Absolute Gain Accuracy	0 dB @ 1 kHz	-0.8		0.8	dB
	Input Gain L/R-Mismatch	20 Hz – 20 kHz	-0.1		0.1	dB
	Input Gain Step Error	20 Hz – 20 kHz	-0.1		0.1	dB
SNR	Signal to Noise Ratio	A weighting, gain = 0 dB		100		dB
V_{NOISE}	Output Noise Level	20 to 20 kHz, unweighted, gain < -15 dB		<4.5		μV_{rms}
THD+N	Total Harmonic Distortion Plus Noise	VDDCP = 1.8 V, -5 dBFS, R_L=16 Ω		-70		dB
PSRR with respect to AVDD	Power Supply Rejection Ratio	20 Hz - 2 kHz 2 kHz - 20 kHz	70 50			dB
	Output power per channel	VDDCP=2.5 V, THD<1%, R_L=16 Ω, 1 kHz		72		mW

Table 14: Electrical Characteristics: Phase Locked Loop (MCLK)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Input Jitter	cycle to cycle			35	ps
		rms			100	ps
	Input Impedance	DC impedance > 10 MΩ	300 0.5	1	2	Ω pF
Interface Mode (MCLK is 256 Fs, PLL off)						
F_{in}	Input frequency	256 Fs 128 Fs (96 kHz)	11.289		12.288	MHz
Oscillator Mode (MCLK from Standard Oscillator, PLL on)						
F_{in}	Input frequency		10		80	MHz
		32 kHz mode		32.768		kHz
	I2S tracking range (SRM)	Maximum mismatch of I2S word-clock			4	%
	I2S clock drift	Maximum frequency drift of I2S word clock			50	ppm/s
$V_{IN\ AC}$	MCLK Shaper range	For AC coupling with internal clock shaping	300	500	1000	mV_{PP}

Table 15: Electrical Characteristics: Digital I/O

(Ta = -40 to +85°C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
VIH	CLK, WCLK, DATIN, SK, SI, PD, MCLK Input High Voltage		0.7*VDD		VDD	V
VIL	CLK, WCLK, DATIN, SK, SI, PD, MCLK, Input Low Voltage		-0.3		0.3*VDD	V
VOH @ 1 mA	CLK, WCLK, DATOUT Output High Voltage		0.8*VDD		VDD	V
VOL @ 1 mA	CLK, WCLK, DATOUT Output Low Voltage		0		0.3	V
	MCLK Input High Voltage	DC-coupled TTL signal	0.7*VDD		VDD	V
	MCLK Input Low Voltage		-0.3		0.3*VDD	V

7 Timing Characteristics

7.1 Digital Audio Interface Timing - I2S/DSP (in Master/Slave Mode)

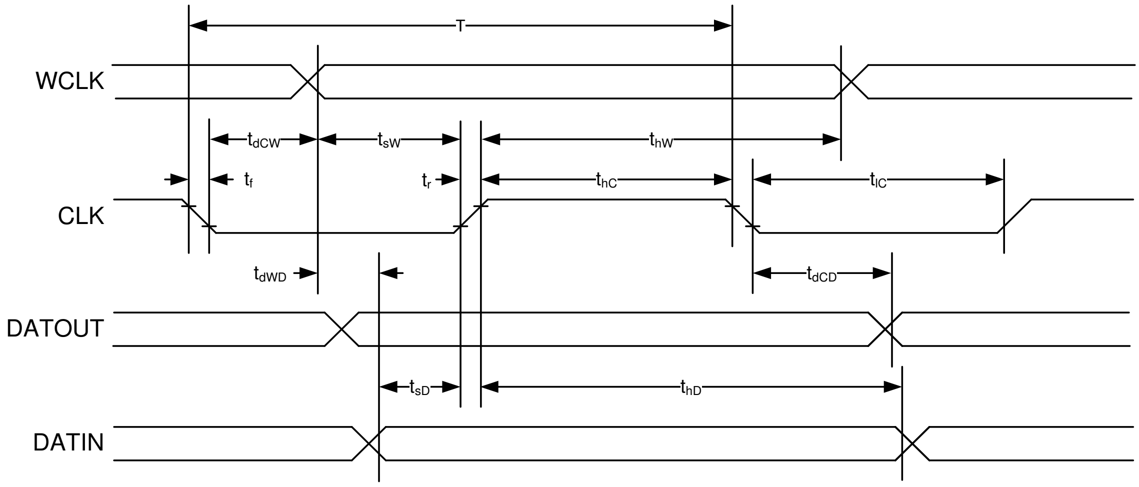


Figure 4: I2S/DSP Timing Diagram

Table 16: I2S/DSP Timing Characteristics

(Ta = -40 to +85ºC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Input impedance	DC impedance > 10 MΩ	300 1.0		 2.5	Ω pF
T	CLK period		75			ns
t_r	CLK rise time				8	ns
t_f	CLK fall time				8	ns
t_{hC}	CLK high period		40%		60%	T
t_{lC}	CLK low period		40%		60%	T
t_{dCW}	CLK to WCLK delay		-30%		+30%	T
t_{dCD}	CLK to DATOUT delay		-30%		+30%	T
t_{hW}	WCLK high time	DSP mode	100%			T
		Non-DSP mode	Word length			T
t_{lW}	WCLK low time	DSP mode	100%			T
		Non-DSP mode	Word length			T
t_{sW}	WCLK setup time	Slave mode	7			ns
t_{hW}	WCLK hold time	Slave mode	2			ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{sD}	DATIN setup time		7			ns
t_{hD}	DATIN hold time		2			ns
t_{dWD}	DATOUT to WCLK delay		DATOUT is synchronised to CLK			

7.2 Digital Audio Control Timing - 2-Wire Control Timing

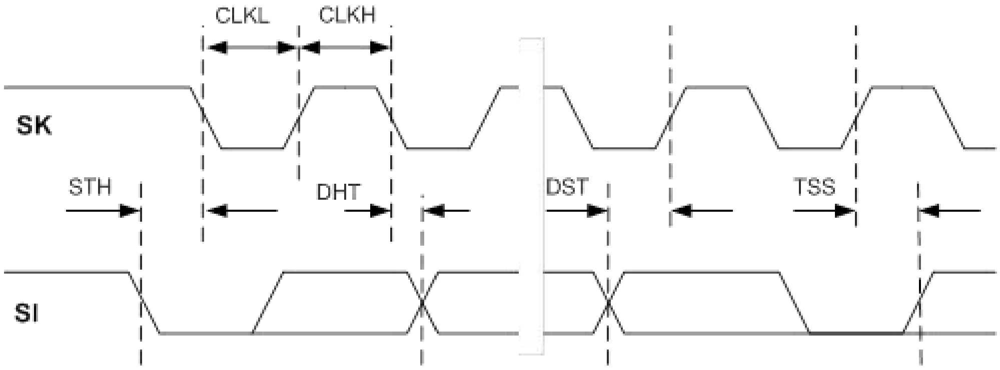


Figure 5: 2-Wire Control Timing Diagram

Table 17: 2-Wire Control Timing Characteristics

(Ta = -40 to +85ºC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Bus free time STOP to START		1.3			µs
	Bus Line Capacitive load				100	pF
Standard/Fast Mode						
	SK clock frequency		1		400	kHz
	Bus free time STOP to START		1.3			µs
	Start condition set-up time		0.6			µs
STH	Start condition hold time		0.6			µs
CLKL	SK low time		1.3			µs
CLKH	SK high time		0.6			µs
	2-wire SK and SI rise/fall time				300	ns
DST	SI set-up time		100			ns
DHT	SI hold-time		0			ns
TSS	Stop condition set-up time		0.6			µs
High Speed Mode						
	SK clock frequency		1		1700	kHz

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Start condition set-up time		160			ns
STH	Start condition hold time		160			ns
CLKL	SK low time		160			ns
CLKH	SK high time		60			ns
	HS-2-wire SK rise/fall time				40	ns
	HS-2-wire SI rise/fall time				80	ns
DST	SI set-up time		10			ns
	SI hold-time		0			ns
TSS	Stop condition set-up time		16			ns

Table 18: Start-Up Times after Setting SC_MST_EN = 1

Source	Output	Comment	Min	Typ	Max	Unit
	VBG	VBG voltage >90% with 1 µF VBG capacitor		25		ms
All analogue inputs and DACL/R	HPL/R	Slave mode; 200 ms added delay required	200	200		ms
All analogue inputs and DACL/R	HPL/R	32 kHz PLL master mode; 200 ms added delay required		500		ms
All analogue inputs and DACL/R	OUT1L/R	Slave mode		250		ms
All analogue inputs	ADCL/R	Slave mode		200		ms
All analogue inputs	ADCL/R	32 kHz PLL master mode		600		ms

8 Functional Description

DA7211 is an ultra-low power audio codec with a true ground headphone, mixing capability and a programmable ASSP filter engine. It offers Hi-Fi audio quality with class-leading power consumption for portable media applications.

Featuring a high-efficiency headphone amplifier and a minimum supply voltage of 1.8 V, the ultra-low 2.5 mW power consumption extends music playback time for battery operated equipment.

The integrated PLL uses a FRACT-N PLL architecture that supports a large range of input and output frequencies. This can accept standard mobile phone/USB system clock frequencies, thus enabling audio data synchronisation when no master clock is readily available.

Eight analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimise dynamic range prior to digitisation. This allows a diverse variety of analogue audio sources such as baseband voice, mobile TV, Wi-Fi and FM radio to be managed.

Input and output mixers with stereo-to-mono conversion also support mono configurations such as headset/baseband line outputs.

Three output drivers are available in the output stage of the DA7211. One output driver will directly drive standard 3-wire 16 Ω headphones whilst the other two provide two adjustable, fully differential stereo lineout channels. For example the dc-coupled, dedicated pop-free drivers may be connected simultaneously to stereo headphones, stereo speakers and a mono line out without external switches.

All filtering and sidetone functions are performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters.

The multi-slot I2S/PCM interface supports all common sample rates between 8 and 96 kHz in master or slave modes.

8.1 Stereo Codec

8.1.1 Input Signal Chain

The DA7211 has three flexible stereo analogue inputs that can be set up as line inputs, microphone inputs, or both. They can be configured as differential or single ended. Line inputs (AUX1_L/R) and microphone outputs can be routed to the ADC or directly to the output mixers via a bypass path.

8.1.2 Microphone Inputs

The DA7211 includes two analogue microphone inputs, which can be used as a stereo or two mono microphones. These can either be connected in (i) fully differential mode for improved common mode noise rejection and (ii) single ended or in pseudo-differential (by connecting MICN to GND). The larger signal should be always connected to MICPL or MICPR and the smaller should be connected to MICNL or MICNR.

The microphone PGAs are enabled by the MIC_L_EN/MIC_R_EN controls (address 0x07/0x08, (Table 44 and Table 45). For maximum flexibility each microphone channel includes an individual gain setting MIC_L_VOL (address 0x7, Table 44), which have a range of -6 dB to +24 dB in 6 dB steps. A maximum gain from microphone to ADC input of +42 dB can be selected with a resolution of 1.5 dB.

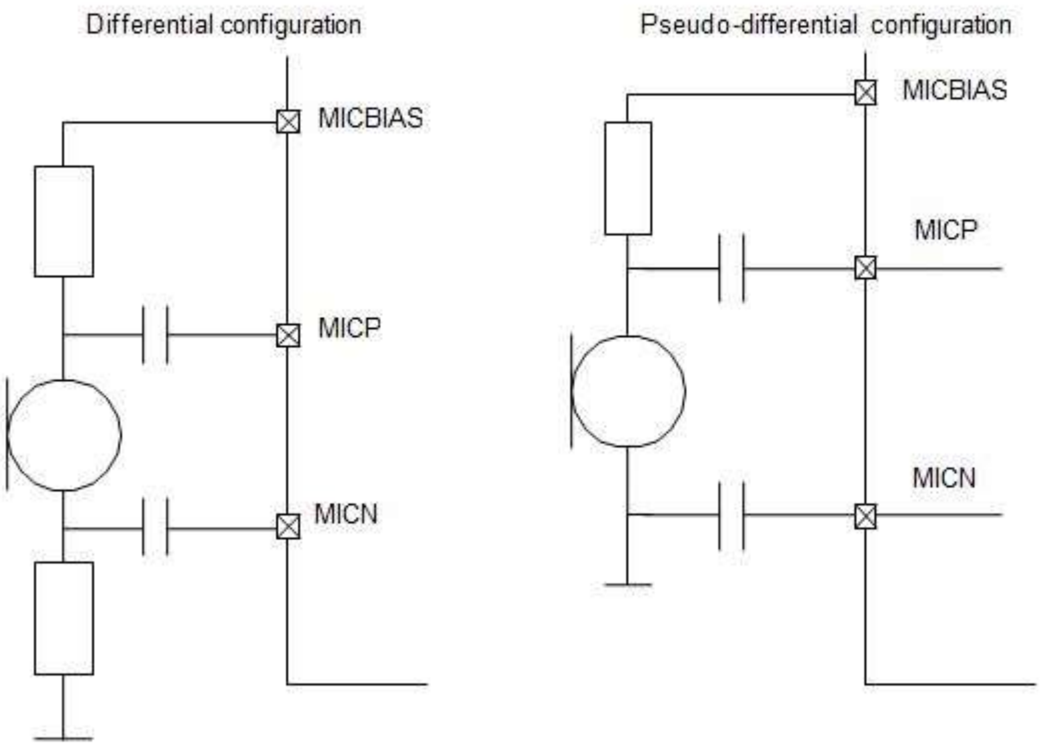


Figure 6: Typical Microphone Applications

Standard electret microphones can be supplied from an on chip microphone bias. This generates an ultra-low noise voltage to feed several electret microphones with up to 2 mA. Depending on the provided AVDD level, the bias voltage can be configured via MICBIAS_SEL (address 0x07, Table 44). If it is not needed then the microphone bias can be powered down using MICBIAS_EN (address 0x07, Table 44).

8.1.3 Auxiliary Inputs

Standard analogue sources are supported via the stereo line inputs AUX1_L and AUX1_R. Mono sound sources are intended to be connected to the right channel of AUX1. Each channel includes individual gain settings of 48 to 21 dB in 1.5 dB steps using AUX1_L_VOL and AUX1_R_VOL (address 0x09/0x0A, Table 46 and Table 47). A maximum gain from auxiliary to ADC input of +36 dB with a resolution of 1.5 dB can be selected. The gain describes the overall input signal to output signal ratio (independent whether the path is single ended or differential).

8.1.4 Stereo Audio ADC

DA7211 includes a low power 24 bit high quality stereo audio ADC, which uses a continuous time delta-sigma modulator providing improved robustness against uncorrelated environmental noise. The ADC supports sampling rates from 8 kHz to 96 kHz. A master clock has to be provided at MCLK whenever the ADC or DAC are in operation.

Dependent on the intended recording path, the stereo ADC can power down one channel at a time via controls ADC_L_EN and ADC_R_EN (address 0x10, Table 52) to provide optimal power dissipation. To enable saturation free maximum signal-to-noise, the input levels of the ADC are adjusted with input PGAs.

The inputs to left and right input mixers are controlled by the bits in the INMIX_L and INMIX_R registers (addresses 0x0D and 0x0E, Table 49 and Table 50). Gain settings for the left and right PGAs are controlled by INPGA_L_VOL and INPGA_R_VOL (address 0x0C, Table 48), with a range of 4.5 dB to 18 dB with 1.5 dB resolution.

For smooth volume changes the gain update can be synchronised to signal zero crossings enabled using INZX_L_EN and INZX_R_EN (address 0x24, Table 71). Disabling the left ADC saves power for mono recordings of stereo input signals by using the analogue stereo to mono conversion from the input mixer. This configuration requires setting the INPGA_L_VOL to 0 dB (‘0011’) and the assertion of IN_R_IN_L (address 0x0E, Table 50).

The IIR filters are enabled using ADC_HPF_EN (address 0xF, Table 51, and see blocks ‘ADC HP’ in Figure 15). The filters (typ. <2 Hz roll-off) are configurable by control ADC_HPF_F0 (address 0x0F, Table 51) and, if enabled, will remove any DC offset from the input path. After Reset, the filters for both channels are enabled by default. Enabling the high pass filter is especially important if the ADC output is fed back into the DAC.

By default the ADC bias current is minimised, but it is possible to improve the THD+N performance of the ADC by approximately 4 dB by increasing this current. The bias current is increased by setting the ADC_T2 bit (address 0x95[3], Table 175).

Also by default the VMID buffer current is enabled for DAC operation, but this buffer is not required for analogue only paths and for ADC only operation. The VMID bias current can be disabled by setting the VMID_BUFF_EN bits (address 0x96[2:0], Table 176) and a significant power saving can be made.

Table 19: ADC Digital High Pass Filter Specifications

Sampling Frequency (kHz)	Cut-Off Frequency (Hz) at ADC_HPF_F0 Setting			
	00	01	10	11
48	2	4	8	16
44.1	1.8	3.7	7.3	14.7
32	1.3	2.7	5.3	10.7
24	1	2	4	8
22.05	0.9	1.8	3.7	7.3
16	0.7	1.3	2.7	5.3
12	0.5	1	2	4

11.025	0.4	0.9	1.8	3.7
8	0.3	0.7	1.3	2.7

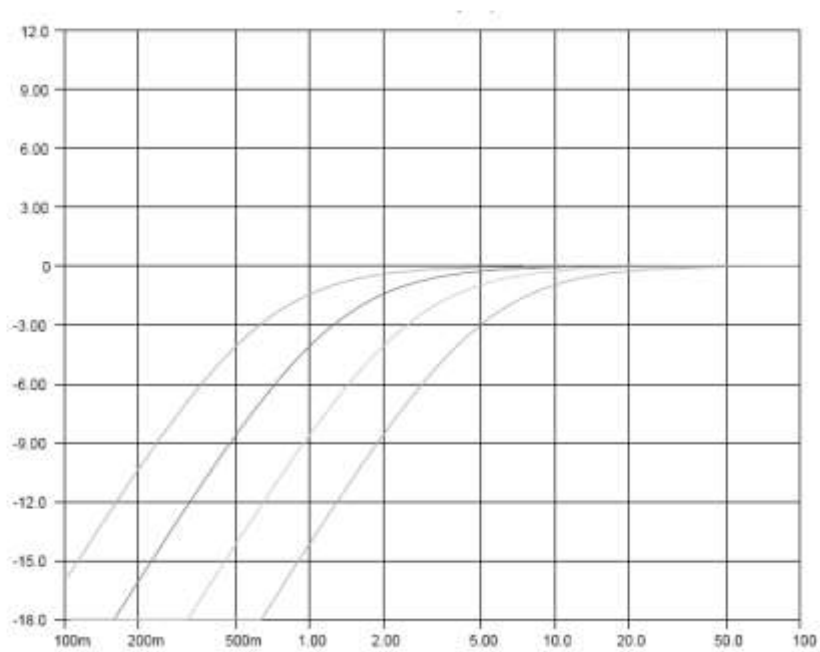


Figure 7: ADC and DAC DC Blocking (Cut-Off Frequency Setting '00' to '11', 16 kHz)

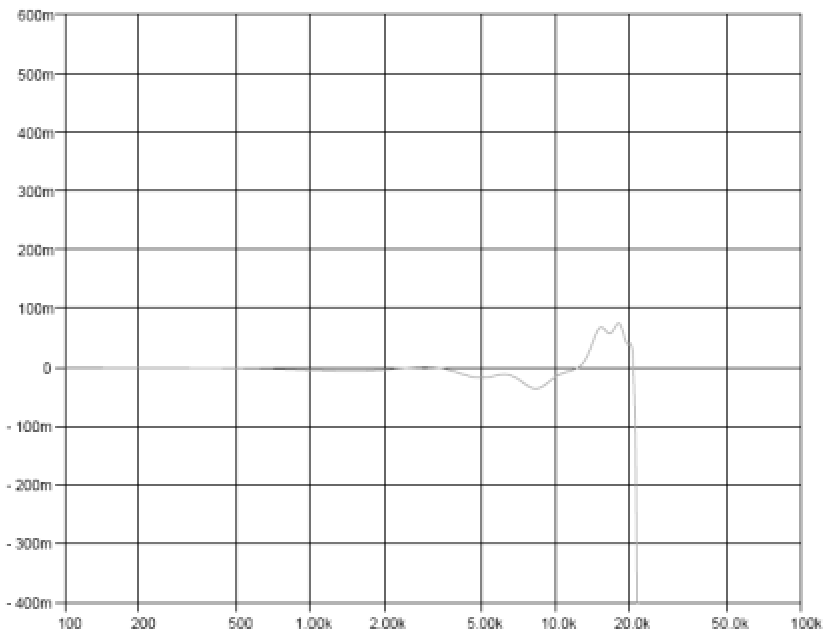


Figure 8: ADC Pass Band Attenuation (Audio Mode, 48 kHz)

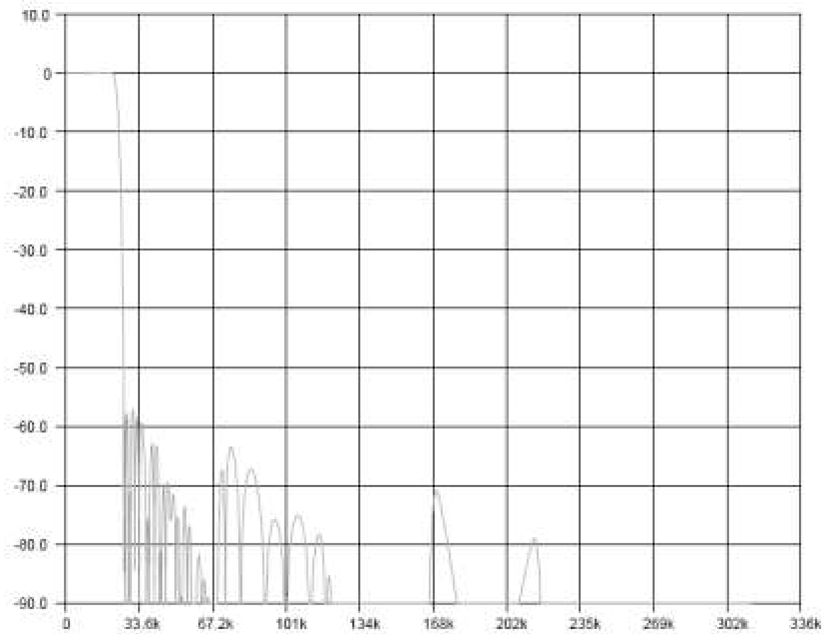


Figure 9: ADC Pass Band Suppression (Audio Mode, 48 kHz)

8.1.5 Automatic lLevel Control (ALC)

For improved sound recordings of signals with a widely changing loudness the DA7211 offers an automatic recording level control (ALC).

It is enabled via ALC_EN (address 0x10, Table 52) and monitors the analogue signal before it enters the ADC and adapts the input gain to keep a constant recording volume irrespective of the analogue input signal level.

Figure 10 (below) illustrates the operation of the ALC. It shows an input signal with high level. The output level is reduced when its level is above the upper threshold, and increased when it falls below the minimum threshold.

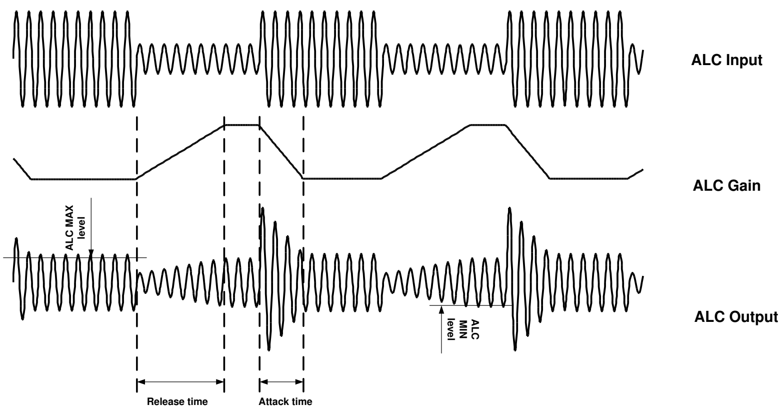


Figure 10: Operation of ALC

If this absolute value of an analogue signal is greater than ALC_MAX (address 0x83, Table 165), then the gain is ramped down at a rate determined by the ALC_ATT (address 0x86, Table 168).

If this absolute value is lower than a level set in ALC_MIN (address 0x84, Table 166), the gain is ramped up at a rate determined by ALC_REL (address 0x87, Table 169).

ALC_MAX needs to be greater than ALC_MIN (minimum delta 1.5 dB). The target level is best achieved by setting these values close to each other. A wider delta allows for a larger input range, and that will reduce the ALC activity. The value of ALC_REL is configured in increments of 4 sample periods. The gain-ramping is performed inside the input PGA in steps of 1.5 dB. To prevent audible clicks each analogue gain step is interpolated by 8 digital volume steps of 0.25 dB inside the ADC (the rate refers to the intermediate steps inside the ADC). However, the level must be lower than ALC_MIN for a time greater than the hold time in order for this gain increase to take place.

The hold time is determined by ALC_DEL (address 0x88, Table 170) in increments of ALC_REL periods, which allows long hold periods to be programmed for a reduction of potential 'gain pumping' during dynamic signal content.

For ALC noise value, refer to Table 20.

Table 20: Permitted Register Values for ALC_NOIS (0x85 [5:0])

Dec	Bin	Hex	Level (dB)		Dec	Bin	Hex	Level (dB)
60	111100	3C	-0.5		29	011101	1D	-47
59	111011	3B	-2		28	011100	1C	-48.5
58	111010	3A	-3.5		27	011011	1B	-50
57	111001	39	-5		26	011010	1A	-51.5
56	111000	38	-6.5		25	011001	19	-53
55	110111	37	-8		24	011000	18	-54.5
54	110110	36	-9.5		23	010111	17	-56
53	110101	35	-11		22	010110	16	-57.5
52	110100	34	-12.5		21	010101	15	-59
51	110011	33	-14		20	010100	14	-60.5
50	110010	32	-15.5		19	010011	13	-62
49	110001	31	-17		18	010010	12	-63.5
48	110000	30	-18.5		17	010001	11	-65
47	101111	2F	-20		16	010000	10	-66.5
46	101110	2E	-21.5		15	001111	0F	-68
45	101101	2D	-23		14	001110	0E	-69.5
44	101100	2C	-24.5		13	001101	0D	-71
43	101011	2B	-26		12	001100	0C	-72.5
42	101010	2A	-27.5		11	001011	0B	-74
41	101001	29	-29		10	001010	0A	-75.5
40	101000	28	-30.5		9	001001	09	-77
39	100111	27	-32		8	001000	08	-78.5
38	100110	26	-33.5		7	000111	07	-80
37	100101	25	-35		6	000110	06	-81.5
36	100100	24	-36.5		5	000101	05	-83
35	100011	23	-38		4	000100	04	-84.5
34	100010	22	-39.5		3	000011	03	-86

33	100001	21	-41		2	000010	02	-86
32	100000	20	-42.5		1	000001	01	-86
31	011111	1F	-44		0	000000	00	-86
30	011110	1E	-45.5					

Examples for ALC_ATT (address 0x86, Table 168).

(fs=44.1 kHz; sample period = 22.67 µs)

Setting	ms per 1 dB step
11111111 (FF)	23.2
10111111 (BF)	17.4
01111111 (7F)	11.6
00111111 (3F)	5.8
00011111 (1F)	2.9
00001111 (0F)	1.5
00000100 (04)	0.5

Examples for ALC_REL (address 0x87,Table 169).

(fs=44.1 kHz; sample period = 22.67 µs)

Setting	ms per 1 dB step
11111111 (FF)	92.9
10111111 (BF)	69.7
01111111 (7F)	46.4
00111111 (3F)	23.2
00011111 (1F)	11.6
00001111 (0F)	5.8
00000100 (04)	0.5

8.1.6 Noise Gate

A noise gate feature is provided to avoid 'noise pumping' where the gain of the channel is increased to the maximum when there is no signal is present (i.e. only noise). If the level of the input signal drops below the threshold configured inside control ALC_NOIS (address 0x85, Table 167) the channel gain is held.

8.2 Output Signal Chain

8.2.1 Stereo Audio DAC

The integrated stereo DAC is suitable for high quality audio playback of MP3 files and portable multimedia files of all kinds. The DAC has individually enabled channels via controls DAC_L_EN and DAC_R_EN (address 0x17, Table 59).

The DA7211 supports the option of individually phase inverted output signals using controls DAC_L_INV (address 0x15, Table 57).and DAC_R_INV (address 0x16, Table 58).

A digital high pass filter for each DAC channel is implemented (configurable by control DAC_HPF_F0 (address 0x14, Table 56) that can be enabled via control DAC_HPF_EN (address 0x14, Table 56, see blocks 'DAC HP' in Figure 15). After Reset, the high pass filters for both channels are enabled by default.

Table 21: DAC Digital High Pass Filter Specifications

Sampling Frequency (kHz)	Cut-Off Frequency (Hz) at DAC_HPF_F0 Setting			
	00	01	10	11
48	2	4	8	16
44.1	1.8	3.7	7.3	14.7
32	1.3	2.7	5.3	10.7
24	1	2	4	8
22.05	0.9	1.8	3.7	7.3
16	0.7	1.3	2.7	5.3
12	0.5	1	2	4
11.025	0.4	0.9	1.8	3.7
8	0.3	0.7	1.3	2.7

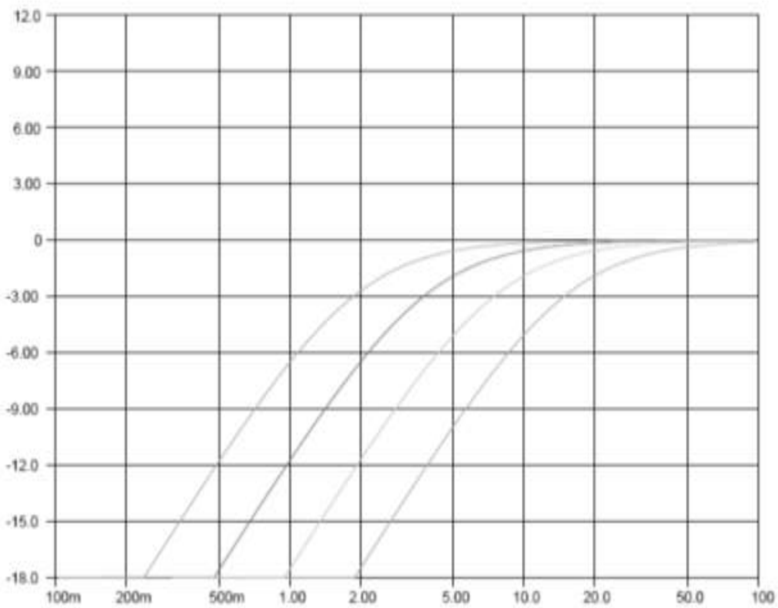


Figure 11: DAC DC Blocking (Cut-Off Frequency Setting '00' to '11', 48 kHz)

8.2.2 Soft Mute

To improve the user's perception of audio reconfigurations, the DAC channel signals may be soft muted by asserting control SOFT_MUTE (address 0x18, Table 60). The soft mute function attenuates the digital input to the DAC, ramping the gain down in steps of 0.1875 dB from the nominal level to -77.25 dB, before completely muting the channel.

When SOFT_MUTE is released, the attenuation is set to -77.25 dB, and then ramped up to the initial gain. Both left and right channels are muted simultaneously. The ramping speed is dependent on the audio sample rate and can be configured by control MUTE_RATE (address 0x18, Table 60). Status bits SOFTMUTED and MUTING may be read from the system status register (address 0x02, Table 40).

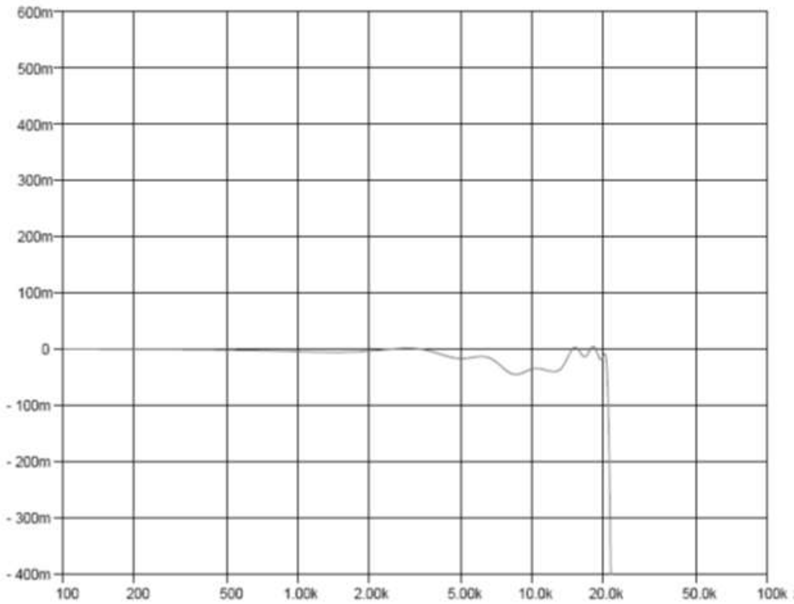


Figure 12: DAC Pass Band Attenuation (Audio Mode, 48 kHz)

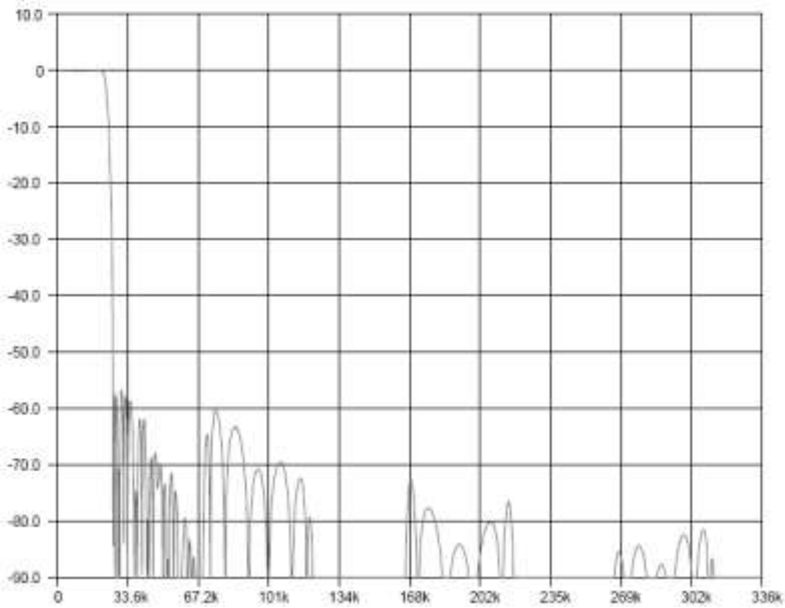


Figure 13: DAC Pass Band Suppression (Audio Mode, 48 kHz)

8.2.3 Output Mixer and Line-Out Amplifier

For playback the output mixer has to be enabled via OUT1_L_EN and OUT1_R_EN (addresses 0x1C, Table 64 and 0x1D, Table 65). The audio signal can be mixed from all sources and listened to via headphones/speakers and recorded simultaneously if required.

OUTMIX_L and OUTMIX_R (addresses 0x1C, Table 64 and 0x1D, Table 65) are independent of the input path, thus allowing recording of a different audio signal when listening to stereo sources like FM Radio or MP3 playback. The playback sound can be mixed with background or inverted background microphone signals (side tone) to enable a basic headphone environmental noise reduction or to compensate unwanted damping of environmental sound happening with sealed headphones. Playback signals can be inverted individually for left and right channel via OUT_L_INV (address 0x1C, Table 64), OUT_R_INV (address 0x1D, Table 65) or for playback of signals from the DAC via DAC_L_INV/DAC_R_INV (address 0x15, Table 57).

A stereo to mono conversion can either be realised by the input or the output mixer. This allows direct feeding of phone earpiece receivers, high power speaker amplifiers and other mono devices with the complete audio content. Unused channels of the stereo line out can be switched off to reduce power consumption using OUT1_L_EN (address 0x1E, Table 66) and OUT1_R_EN (address 0x1F, Table 67). The mixer allows listening to mono signals like baseband or Bluetooth voice also at both channels of stereo headphones.

Each differential channel of OUT1 can alternatively be individually configured to be single ended via OUT1_L_SE (address 0x1E, Table 66) and OUT1_R_SE (address 0x1F, Table 67). Typical earpiece receivers with an impedance > 32 Ω can be driven directly in differential mode at all outputs. This amplifier offers individual programmable volume control from +15 dB to –54 dB in 1.5 dB steps, then mute for steps below -54 dB using controls OUT1_L_VOL (address 0x1E, Table 66) and OUT1_R_VOL (address 0x1F, Table 67). For smooth volume changes, the gain update can be synchronised to zero-crossing of the signal using OUTZX_L_EN and OUTZX_R_EN (address 0x24, Table 71). If no zero-crossing is detected within 2048 sample periods, the gain change is applied unconditionally. The left and right channels are synchronised independently.

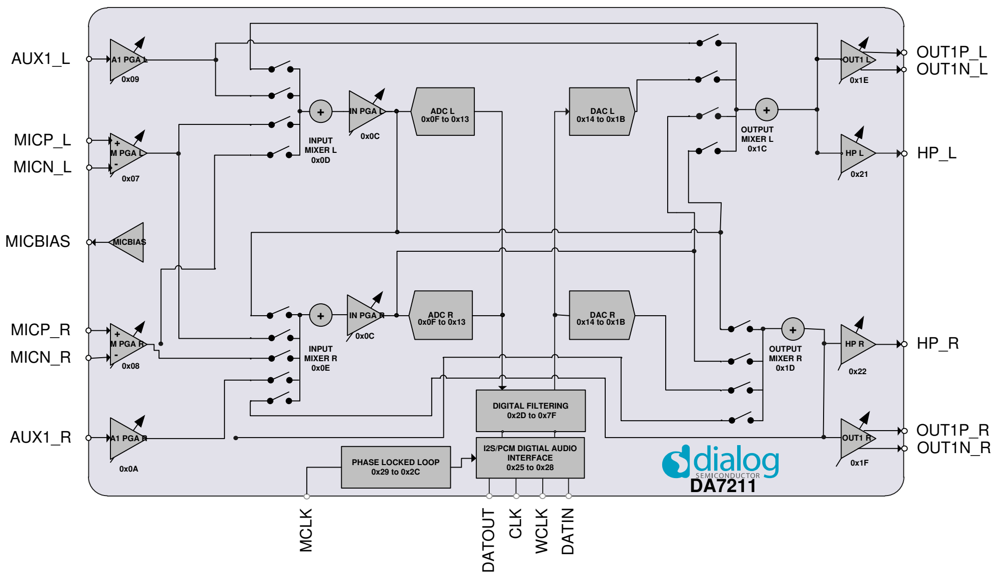


Figure 14: DA7211 Audio Signal Paths

8.2.4 Headphone Amplifier

The headphone Class G amplifiers are enabled by controls HP_L_EN and HP_R_EN (address 0x23, Table 70) and their output can be set to high impedance mode using HP_HIGHZ_L and HP_HIGHZ_R (address 0x23, Table 70).

They offer 'true ground' technology, which allows cost and space optimisation by removing the need for large capacitors in the headphone paths. This also enhances the bass performance, which is typically reduced by conventional AC-coupling. In comparison to alternative approaches like ‘phantom ground’, the ‘true ground’ technology generates real ground-centred output signals, and provides common GND as required for Mini-USB connectors and CEA-936-A compliant interfaces.

Integrated short-circuit protection enables a ‘resistors free’ connection to a standard audio jack to achieve a maximum output power of up to 58 mW per channel (referenced to VDDCP). The output mixing units enable the support of single-ended mono and stereo, as well as differential headphones selected by OUT_R_INV (address 0x1D, Table 65).

Headphone load impedance is typically 16 Ω, but the paths can also be used as volume controlled lineout signals for external speaker amplifiers and audio devices. The headphone Class G amplifiers are supplied from the positive VDDCP rail via a capacitive charge pump that generates the negative rail required for ‘true ground’ mode. For improved power efficiency it provides dynamically adjusted supply voltage levels VDD, VDD/2, VDD/3 and VDD/4, which are automatically adjusted by DA7211 from the average left and right level of the headphone audio signals see control HP_CFG (address 0x23, Table 70).

To minimise the number of external components the charge pump provides a restricted mode enabled via HP_2CAP_MODE (address 0x23, Table 70), which removes the need for the second flying cap (at pins HPCF2P and HPCF2N), but disables the VDD/3 and VDD/4 supply voltage levels.

Unlike conventional solutions DA7211 does not require any coupling capacitors at the ‘true ground’ headphone amplifier input. An embedded offset compensation circuit suppresses click and pop noise during both start-up and dynamic supply-voltage adjustments.

Table 22: Headphone/OUT1 Amplifier Gain Settings

GAIN	CODE	GAIN	CODE
MUTE	0x10	-19.5 dB	0x28
-54.0dB	0x11	-18.0 dB	0x29
-52.5dB	0x12	-16.5 dB	0x2A
-51.0dB	0x13	-15.0 dB	0x2B
-49.5dB	0x14	-13.5 dB	0x2C
-48.0dB	0x15	-12.0 dB	0x2D
-46.5dB	0x16	-10.5 dB	0x2E
-45.0dB	0x17	-9.0 dB	0x2F
-43.5dB	0x18	-7.5 dB	0x30
-42.0dB	0x19	-6.0 dB	0x31
-40.5dB	0x1A	-4.5 dB	0x32
-39.0dB	0x1B	-3.0 dB	0x33
-37.5dB	0x1C	-1.5 dB	0x34
-36.0dB	0x1D	0 dB	0x35
-34.5dB	0x1E	1.5 dB	0x36
-33.0dB	0x1F	3.0 dB	0x37
-31.5dB	0x20	4.5 dB	0x38

-30.0dB	0x21	6.0 dB	0x39
-28.5dB	0x22	7.5 dB	0x3A
-27.0dB	0x23	9.0 dB	0x3B
-25.5dB	0x24	10.5 dB	0x3C
-24.0dB	0x25	12.0 dB	0x3D
-22.5dB	0x26	13.5 dB	0x3E
-21.0dB	0x27	15.0 dB	0x3F

Table 22 relates to the registers shown below

- HP_L_VOL: 0x21[5:0]
- HP_R_VOL: 0x22[5:0]
- OUT1_L_VOL: 0x1e[5:0]
- OUT1_R_VOL: 0x1f[5:0]

To enable volume balance settings the gain of the headphone buffers can be programmed independently for both channels by controls HP_L_VOL (addresses 0x21, Table 68) and HP_R_VOL (addresses 0x22, Table 69) according to Table 22. The gain steps are 1.5 dB from +15 dB down to –54 dB, and mute for the steps below -54 dB. Alternatively the channels' gain settings can be combined with bit STEREO_TRACK (address 0x23, Table 70) and controlled for both channels with volume register HP_R_VOL (address 0x22, Table 69).

For smooth volume changes the gain update can be synchronised to audio signal zero-crossings by enabling HPZX_L_EN and HPZX_R_EN (address 0x24, Table 71). If no zero-crossing is detected within 2048 sample periods, the gain change is applied unconditionally. The left and right channels are synchronised independently.

The headphone outputs are supported by DC offset compensation circuitry to minimise any possible pop and click artefacts during power up/down. To ensure sufficient time for the DC compensation circuitry to operate, a delay of 200 ms must be added after SC_MST_EN (address 0x03, Table 41) bit is enabled.

8.2.5 Ambient Noise Suppression

DA7211 supports stereo noise suppression by subtracting inverted noise signals from the AUX1 inputs at the headphone outputs. The noise signal must pass through the input PGA, be inverted and then mixed with the outputs from the DAC. The signal at the AUX1 inputs for example, can be from microphones picking up ambient noise at the user's ears.

This mode is enabled via control NOISE_SUP (address 0x01 CONTROL, Table 39) and then offers a modified headphones volume control via a combination of three gain stages:

1. Headphones gain settings > 0 dB

All headphone gains settings > 0 dB will be applied to the headphone PGA, but the equivalent gain will be synchronously subtracted from the input PGA to equalise the overall net gain in the ambient noise signal path.

For sufficient range of operation, the starting values of INPGA_L_VOL and INPGA_R_VOL (address 0x0C, Table 48) must be configured >= 10.5 dB (settings '1010' to '1111') before enabling the noise suppression mode.

2. Headphones gain settings <= 0 Db

When DAC is selected to the headphone output any update of the gain less than or equal to 0 dB, using controls HP_L_VOL/HP_R_VOL (address 0x21, Table 68 and address 0x22, Table 69), will be implemented instead using the controls DAC_L_GAIN and DAC_R_GAIN (address 0x15, Table 57 and address 0x16, Table 58). If this were not the case then a large signal on AUX1 could cause clipping at the headphone output.

For the ambient noise signals from the AUX1 path all headphones gain changes <= 0 dB will be implemented using the settings of AUX1_L_VOL and AUX1_R_VOL (address 0x09, Table 46). To allow the full minimum headphone volume of -54 dB, these AUX1_L_VOL and AUX1_R_VOL controls need to be set to >= 6 dB (setting > 110101'b) before enabling the noise suppression mode.

NOTE – The ALC has to be disabled during noise suppression mode and it is recommended to enable zero-crossing for gain updates at the headphone amplifier and the AUX1 PGA (see the register ZEROX (address 0x24, Table 71)). Headphone volume changes should enable digital gain ramping for DAC playback. The controls INPGA_L_VOL, INPGA_R_VOL, AUX1_L_VOL, AUX1_R_VOL, DAC_L_GAIN, and DAC_R_GAIN should not be written to when noise suppression is enabled.

8.2.6 Digital Signal Processing Engine

The digital signal processing engine includes a configurable audio processor that offers flexible routing and extensive audio enhancement and effects. Linear phase FIR filters perform the interpolation and decimation for the required sigma-delta sample rates. Configurable high-pass filtering (optionally enabled) removes any signal DC offset (see blocks 'ADC HP' and 'DAC HP' in Figure 15) and offers 5-band equalisation during recording and sound playback.

Alternatively it can provide dedicated voice band filtering at samples rates ≤ 16 kHz (see blocks 'ADC IIR' and 'DAC IIR' in Figure 15).

An additional general purpose (GP) filter engine offers up to eight second-order biquad filter stages with configurable 16-bit coefficients, and supports flexible digital audio routing and mixing arrangements. Figure 15 shows some possible routings (a subset of the available settings) for filter blocks GP1A to GP2D with the related control registers. Typical use cases with example configurations are explained in the section 8.3.

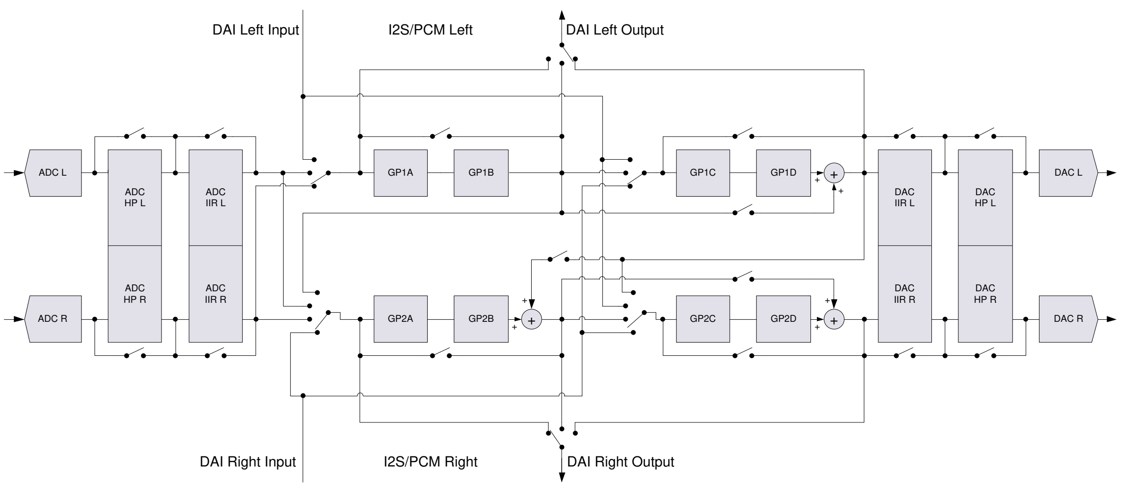


Figure 15: Digital Signal Processing Engine (Simplified Block Diagram)

The GP filter sections are implemented using a Direct Form 1 architecture, as shown in Figure 16.

This structure implements the transfer function:

$$H(z) = \frac{a0 + a1\ z + a2\ z2}{1 - b1\ z - b2\ z2}$$

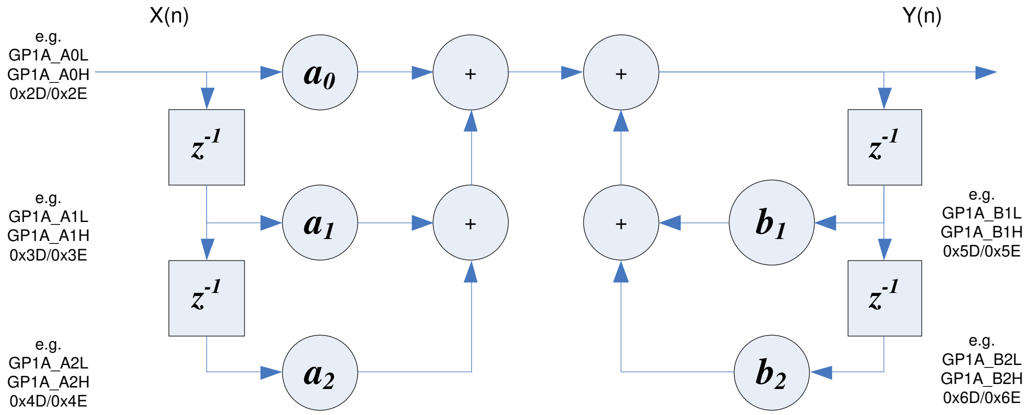


Figure 16: Direct Form I Implementation of a Second Order IIR Filter

Each of the five coefficients may be configured by the user, for each filter section. The coefficients are specified as 16-bit two's-complement numbers, ranging from -2 to +2. Denominator coefficients must be negated, that is, if b1 is positive then a negative value (-b1) must be programmed, and conversely, if b1 is negative then a positive value (+b1) must be programmed. Coefficients must be selected carefully to specify a stable filter.

The filter sections are arranged in four groups, where the input to each filter group can be programmed to be one of up to seven possible sources:

- The two digital audio interface (DAI) output ports (left or right)
- The output from the two ADC channels (left or right)
- The output from a previously processed filter group (one of the up to three remaining groups)

If the processing function of a filter is not required the group can be disabled. In this case, the output path of the filter group is connected directly to the input source. Disabling a filter group reduces the power consumption of the filter group to a minimum.

8.3 Programming the General Purpose Filter

The general purpose filter is configured using two groups of registers. These are coefficient programming and path selection. The coefficients should be programmed using the registers GP1A_A0L (address 0x2D, Table 80) to GP2D_B2H (address 0x7C, Table 159). Coefficients are programmed as two 8-bit registers of signed values representing the range +2 to -2.

Example

GP1A_B1L and GP1A_B1H contain the two's complement low and high bytes of the -b1 coefficient of the filter illustrated in Figure 16. If a coefficient value of 1.45 is required, -b1 is programmed as the coefficient number multiplied by a scaling factor.

The scaling factor 214 is used to convert the floating point number into an integer value for programming. The low byte will always be an 8-bit unsigned hexadecimal value, while the high byte contains the sign bit of the two's complement word.

Scale the unsigned decimal coefficient value:

b1 = 1.45 x 214 = 23756.8 ≈ 23757

The unsigned scaled value in binary:

b1 = 0101110011001100b

Convert to two's complement; invert the binary value and add the MSB sign bit:

b1 = 10100011001100112 = A333h

GP1A_B1L = 33h = 00110011

GP1A_B1H = A3h = 10100011, where MSB is the two's complement sign-bit

Note that the denominator coefficient is explicitly negated. The value of the -b1 term is positive, so a negative value must be programmed. There are eight fully programmable, second-order IIR biquad filter sections grouped in the following pairs:

- 1AB
- 1CD
- 2AB
- 2CD

The output of the first section in each group is cascaded with the second section. The filter sections are processed in a fixed order: 1A, 1B, 1C, 1D, 2A, 2B, 2C, 2D.

Each filter group can be programmed to take its input from one of seven possible sources, that is, from either an ADC or an I2S channel, or from any filter section that has been previously processed using GP_1AB_SRC and GP_2AB_SRC (address 0x7D, Table 160) and GP_1CD_SRC and GP_2CD_SRC (address 0x7E, Table 161) It is possible to cascade all eight GP filters together using these registers. Each filter block can be enabled or disabled in register DSP_CFG (address 0x7F, Table 162).

Table 23: GP Filter Section Enable Bits

Control	Definition
GP1AB_EN	Enable GP section 1AB
GP1CD_EN	Enable GP section 1CD
GP2AB_EN	Enable GP section 2AB
GP2CD_EN	Enable GP section 2CD

The outputs of some groups can be summed together, as controlled by register DSP_CFG (address 0x7F, Table 162).

Table 24: Band-Equaliser Corner Frequencies

Control	Definition
DSP_MIX_1	Output of group 1AB is summed with 1CD
DSP_MIX_2	Output of group 1CD is summed with 2AB
DSP_MIX_3	Output of group 2AB is summed with 2CD

When using the summing facility, the user must ensure that the source signal filter sections are activated and their output levels are such that clipping does not occur.

At 88.2 kHz and 96 kHz sample rates, the number of useable filter sections is halved. Only sections 1B, 1D, 2B and 2D are available.

8.4 Hi-Fi Recording

8.4.1 5-band Equaliser for Recording Path

To allow user-specific sound control, the recording path includes a programmable 5-band equaliser (combined in the ADC IIR blocks in Figure 15). This is enabled using control ADC_EQ_EN (address 0x13, Table 55).

A low-pass filter, three band-pass filters and a high-pass filter with turn over frequencies at approximately 50 Hz, 300 Hz, 1.2 kHz and 5 kHz (bandpass centre frequencies at 150, 500 and 2500 Hz) are controlled using the registers ADC_EQ1_VOL to ADC_EQ5_VOL (addresses: 0x11, Table 53; 0x12, Table 54; 0x13, Table 55). These registers boost or damp each frequency band from -10.5 dB to +12 dB in 1.5 dB steps. Saturation of the signal from boosted frequencies can be prevented by an overall damping control ADC_EQ_GAIN (address 0x13, Table 55), which provides attenuation from -18 dB to 0 dB in 6 dB steps.

Table 25: 5-Band-Equaliser Turn-Over/Centre Frequencies

Sampling Frequency kHz	Low Pass 50 Hz	Band Pass 150 Hz	Band Pass 500 Hz	Band Pass 2500 Hz	High Pass 5000 Hz
96.0	n.a.	n.a.	n.a.	n.a.	n.a.
88.2	n.a.	n.a.	n.a.	n.a.	n.a.
48.0	67	143	627	2565	5100
44.1	62	131	576	2357	4686
32.0	45	95	418	1710	3400
24.0	67	144	659	2953	6230
22.05	62	132	605	2713	5724
16.0	45	96	439	1969	4153
12.0	67	147	726	2230	3050
11.025	62	135	667	2049	2802
8.0	45	98	484	1486	2033

The 5-band equaliser cannot be used at 88.2 kHz and 96 kHz sampling rates, and is automatically disabled if the ADC is configured to Voice Mode using control ADC_HPF_F0 (address 0x0F, Table 51). The frequency responses of the 5-band equaliser are illustrated in Figure 17 to Figure 21.

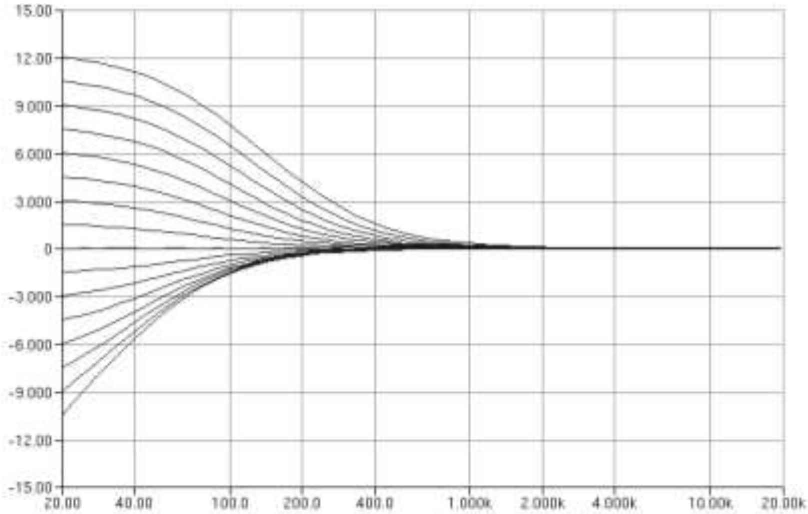


Figure 17: Band 5 (LP 50 Hz) Frequency Response at FS = 48 kHz

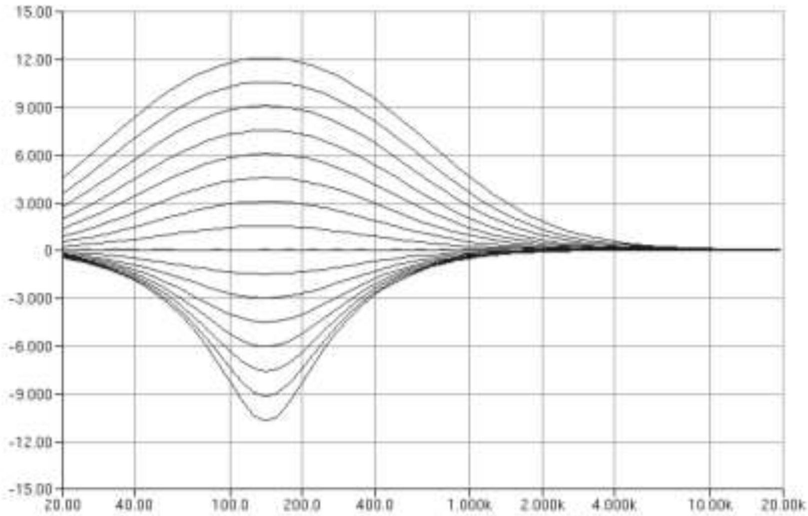


Figure 18: Band 5 (BP 150 Hz) Frequency Response at FS = 48 kHz

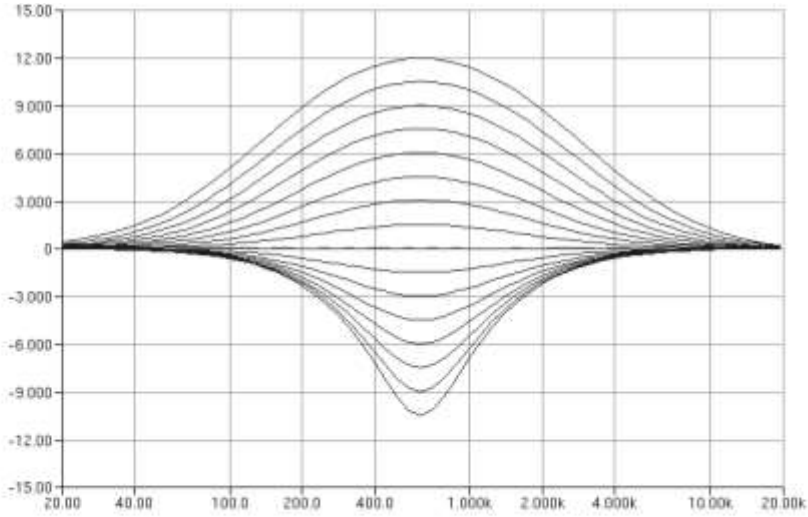


Figure 19: Band 5 (BP 500 Hz) Frequency Response at FS = 48 kHz

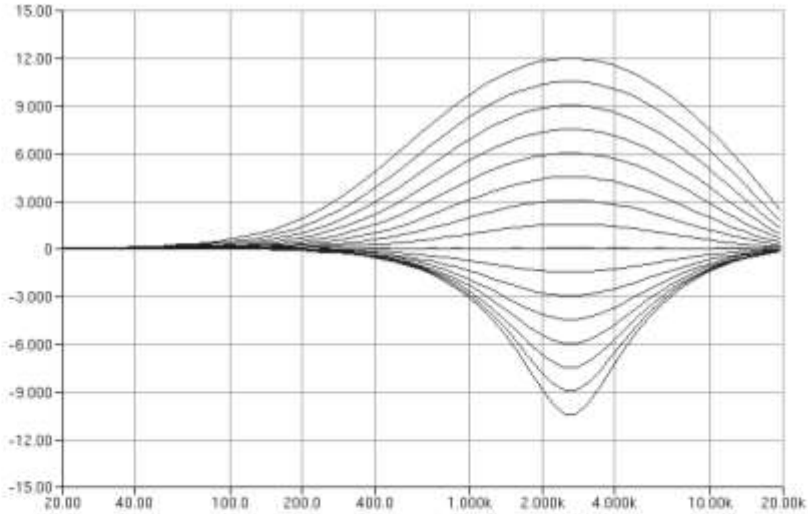


Figure 20: Band 5 (BP 2500 Hz) Frequency Response at FS = 48 kHz

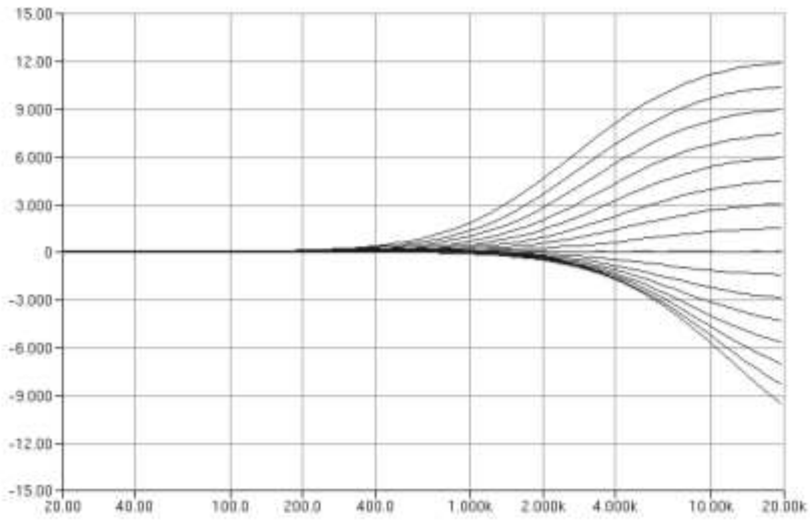


Figure 21: Band 5 (HP 5000 Hz) Frequency Response at FS = 48 kHz

8.4.2 Digital Audio Processing for the Record Path

When Record only is selected, the DAC and playback filter units can be powered down. The general purpose filter engine can offer 8th order stereo filters to correct the acoustic frequency response of the connected microphone (Figure 22).

If less filtering is required, filter stages can be bypassed using the filter enable controls described in Table 23.

For mono playback, this can also be achieved by switching off a complete channel (blocks not required are highlighted in the following figures in light grey).

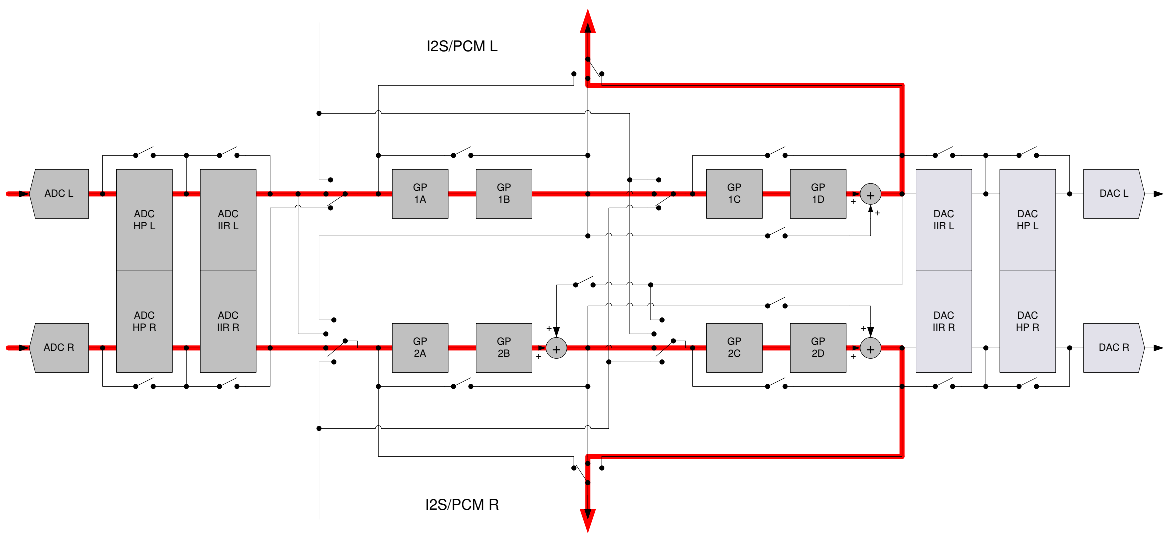


Figure 22: Record Only

If it is intended to listen to the recording as it is being made, or to listen to another sound at the same time as the recording, the general purpose filter engine offers a split mode for parallel record and playback equalisation. This mode supports applications that perform active noise cancellation.

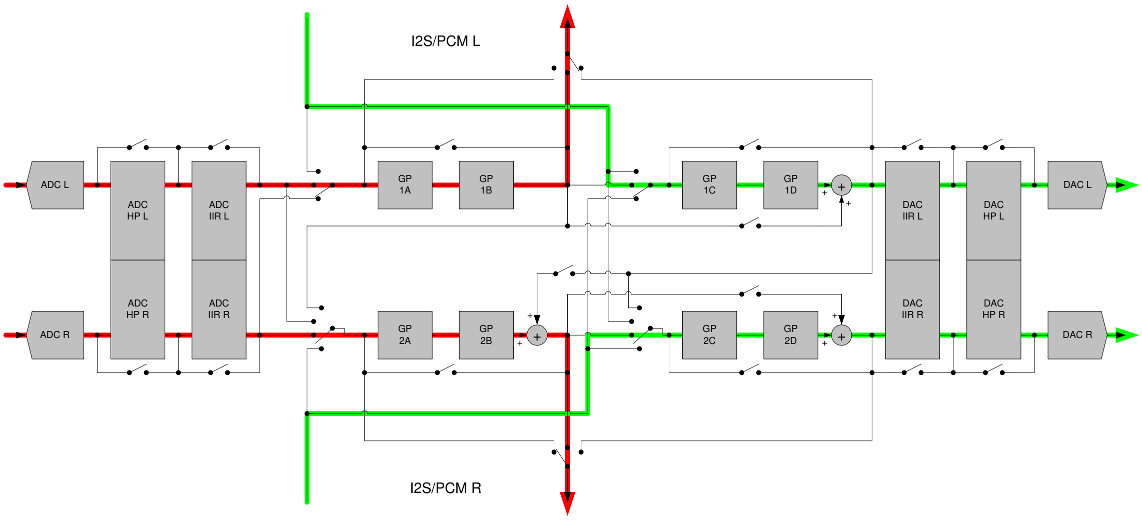


Figure 23: Record with Sound Monitor

8.5 Hi-Fi Playback

8.5.1 5-Band Equaliser for Playback Path

To allow user-specific sound settings, the digital playback path includes a programmable 5-band equaliser, which is enabled using control DAC_EQ_EN (address 0x1B, Table 63).

A low-pass filter, three band pass filters and a high-pass filter, with corner frequencies at approximately 100 Hz, 300 Hz, 1 kHz, 3 kHz and 3 kHz (for FS = 44.1 kHz) are controlled by the registers DAC_EQ1_VOL to DAC_EQ5_VOL (addresses: 0x19, Table 61; 0x1A, Table 62; 0x1B, Table 63). These registers boost or damp each frequency band from -10.5 dB to +12 dB in 1.5 dB steps. Saturation of the signal from boosted frequencies can be prevented by an overall damping control ADC_EQ_GAIN (address 0x1B, Table 63).

The 5-band equaliser cannot be used at a 96 kHz sampling rate and is automatically disabled if the ADC is configured to Voice Mode using control DAC_VOICE_EN (address 0x14, Table 56). Details of corner frequencies are shown in Table 25. Frequency responses are illustrated in Figure 17 to Figure 21.

8.5.2 Digital Audio Processing for Playback Path

In addition to the user selectable sound settings offered by the 5-band equaliser, the playback path offers up to 8th order configurable audio filtering, for example, to correct the frequency response of connected receivers, speakers or headphones.

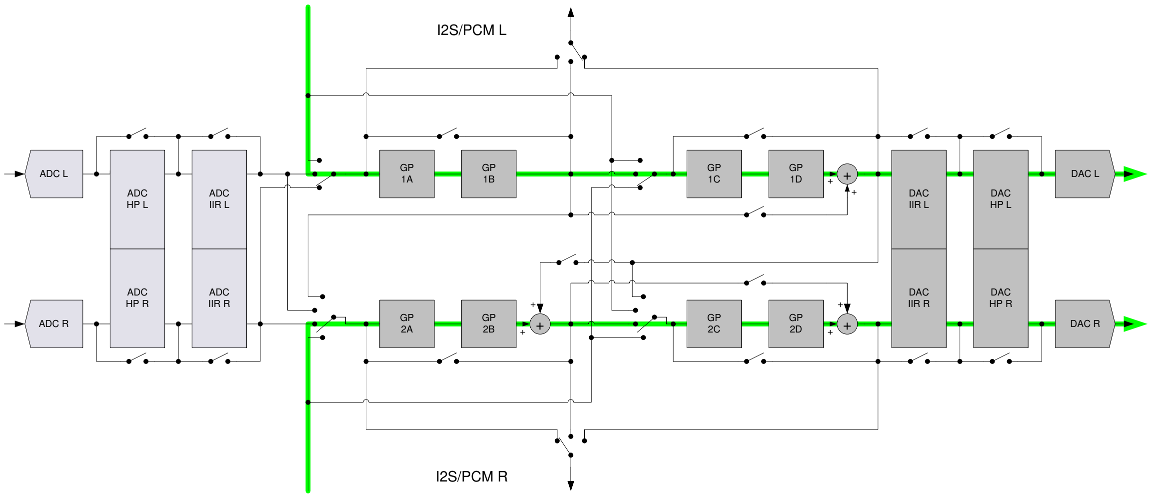


Figure 24: Stereo Playback (for Example, Freefield Headphone Equalisation)

For applications with stereo speakers the digital signal processing offers stereo widening with 3D audio effects.

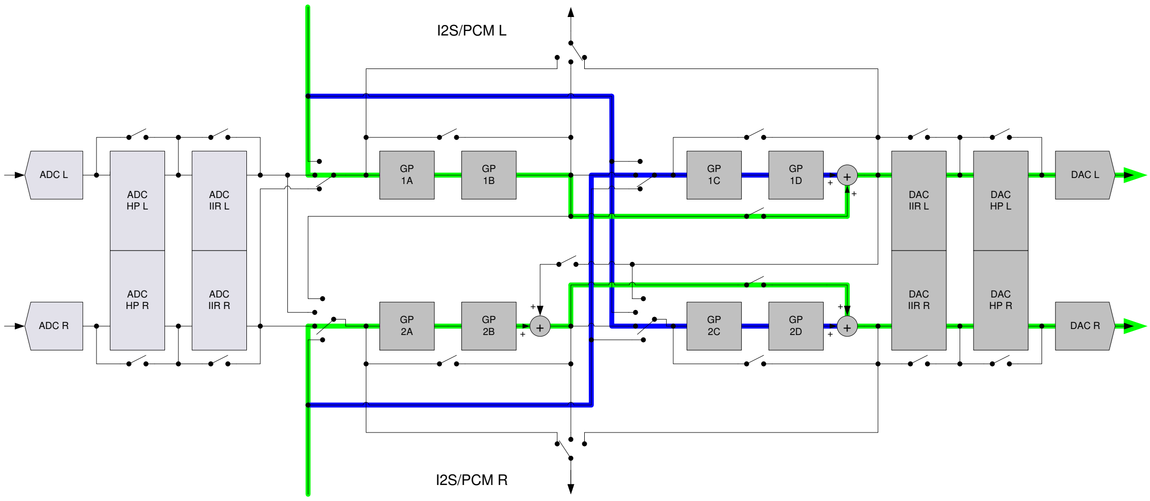


Figure 25: Sound Spatialiser for Stereo Speaker

8.6 Telephone/Bluetooth Voice Recording/Playback at Low Sample Rates

DA7211 offers a dedicated Voice Mode with configurable voice in-band and enhanced out-of-band suppression for sample rates up to 16 kHz.

8.6.1 Voice Filtering for Recording at Low Sample Rates

When the sampling frequency is 8, 11.025, 12 or 16 kHz, a Voice Mode can be enabled via ADC_VOICE_EN (address 0xF, Table 51) where the low frequency roll off is configured using control ADC_VOICE_F0 (address 0xF, Table 51).

NOTE
Voice filter setting takes precedence over the 5 band equaliser. If the voice filter is enabled for the ADC path, the 5 band equaliser for recording is disabled.

Table 26: Voice Mode Recording High Pass Filter Specifications

Cut-off frequency [Hz] at setting								
Fs [kHz]	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
8.0	2.5	25	50	100	150	200	300	400
11.025	3.4	34.5	69	138	207	276	413	551
12.0	3.75	37.5	75	150	225	300	450	600
16.0	5	50	100	200	300	400	600	800

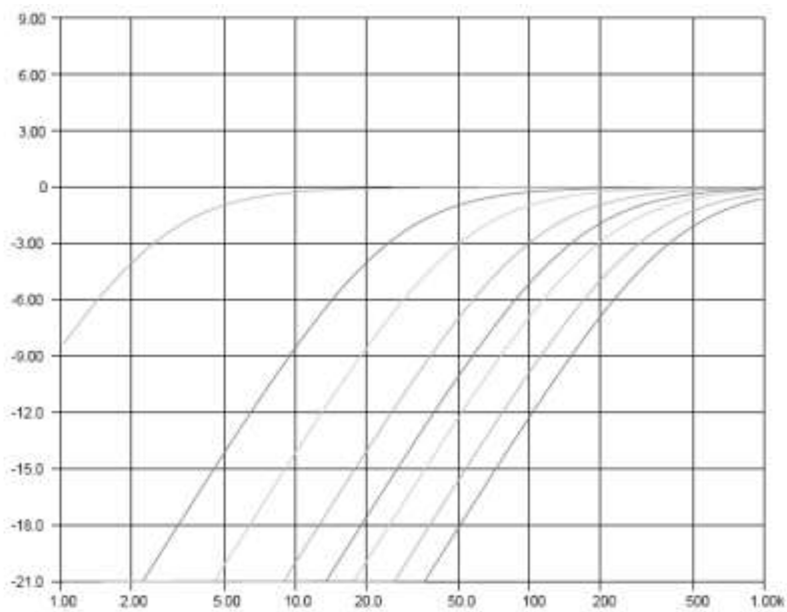


Figure 26: Voice Mode Recording High Pass Filter (Cut-Off Frequency Setting '000' to '111', 8 kHz)

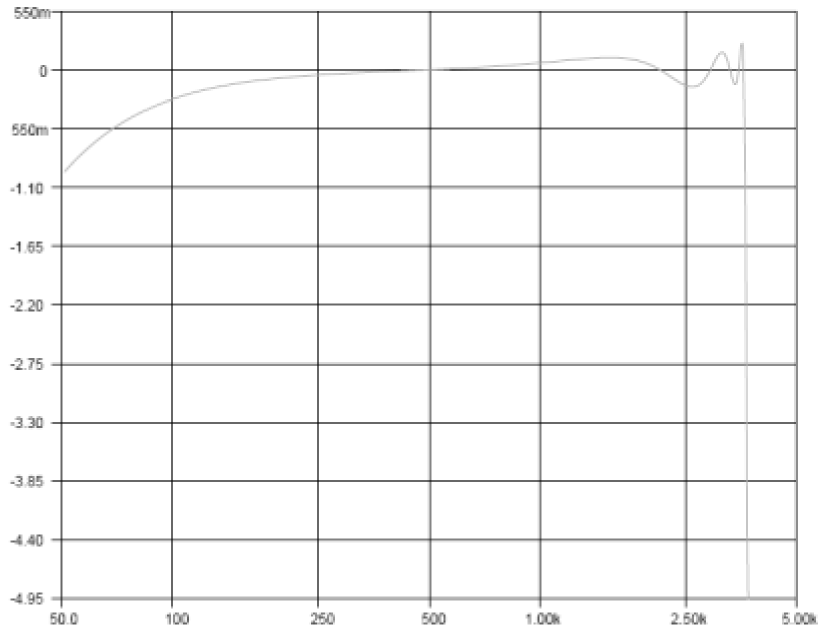


Figure 27: Voice Mode Recording Frequency Response (Setting '001', 8 kHz)

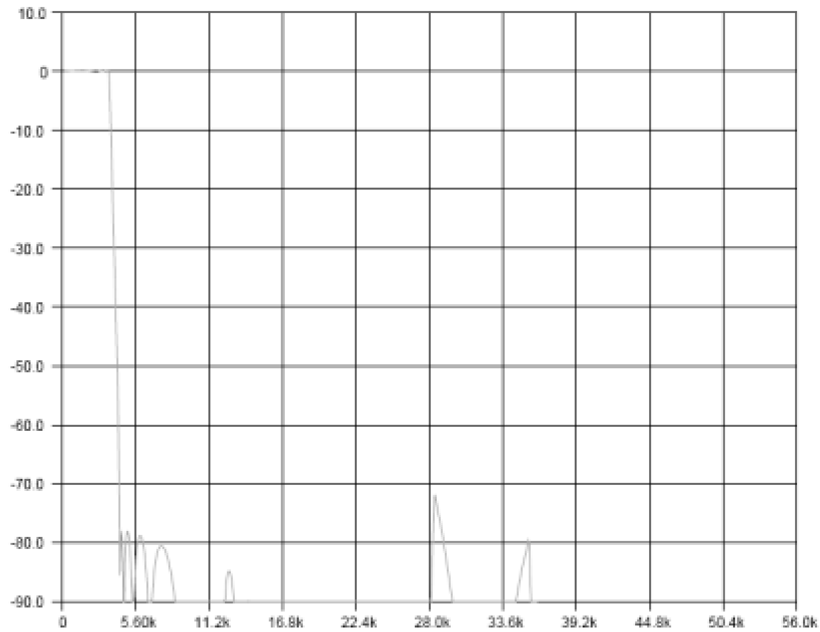


Figure 28: Voice Mode Recording Stop Band Suppression (8 kHz)

8.6.2 Voice Filtering for Playback at Low Sample Rates

For playback the voice mode is enabled via DAC_VOICE_EN (Address 0x14, Table 56) where the low frequency roll off is configured via control DAC_VOICE_F0 (Address 0x14, Table 56).

NOTE
Voice filter setting takes precedence over the 5 band-equaliser. If the voice filter is enabled for the DAC signal the 5-band-equalizer for playback is automatically disabled.

Table 27: Voice Mode Playback High-Pass Filter Specifications

Cut-Off Frequency [Hz] at DAC_VOICE_F0 Setting								
Fs [kHz]	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
8.0	2.5	25	50	100	150	200	300	400
11.025	3.4	34.5	69	138	207	276	413	551
12.0	3.75	37.5	75	150	225	300	450	600
16.0	5	50	100	200	300	400	600	800

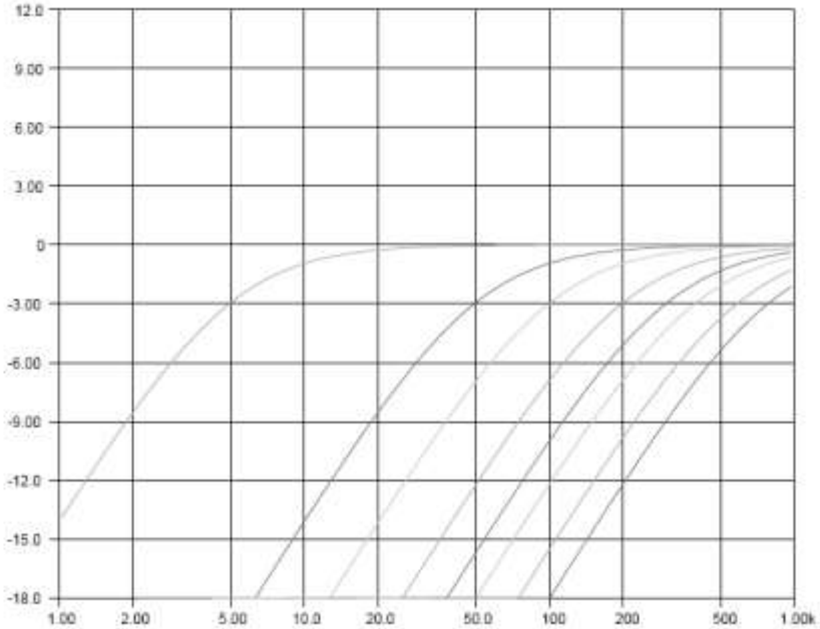


Figure 29: Voice Mode Playback High-Pass Filter (Cut-Off Frequency Setting ‘000’ to ‘111’, 16 kHz)

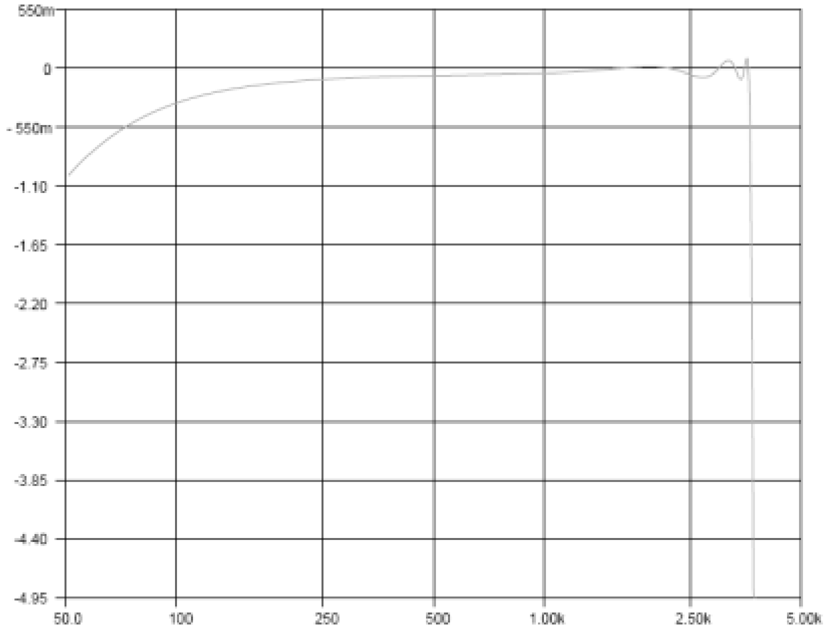


Figure 30: Voice Mode Playback Frequency Response (Setting '001', 8 kHz)

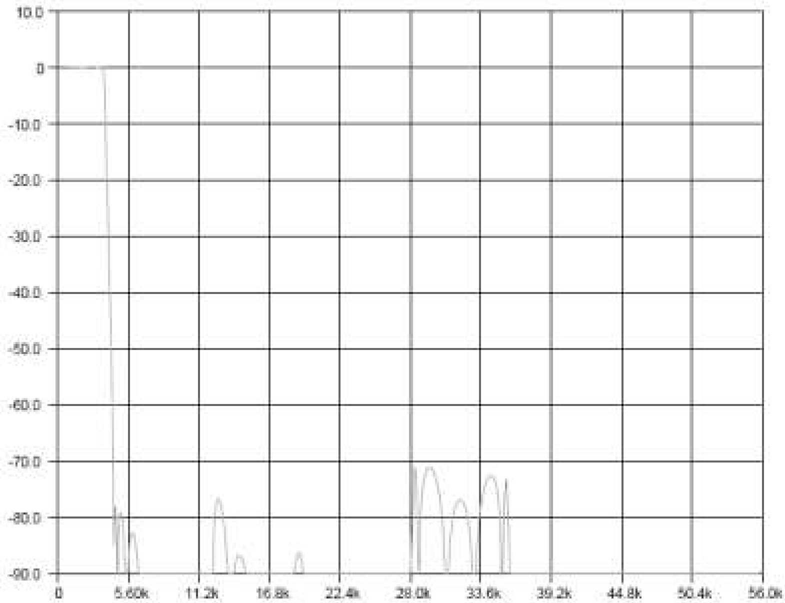


Figure 31: Voice Mode Playback Stop Band Suppression (8 kHz)

8.6.3 Digital Audio Processing for Phone Applications

The general purpose filter engine offers a parallel 4th order acoustic equalisation of microphone and receiver/speaker, and filtering of the sidetone signal to suppress oscillations from any acoustic feedback loop. This allows corrections to the frequency response of acoustic transducers and their mechanical environment that is required for GSM/3GPP type approval of mobile phone applications.

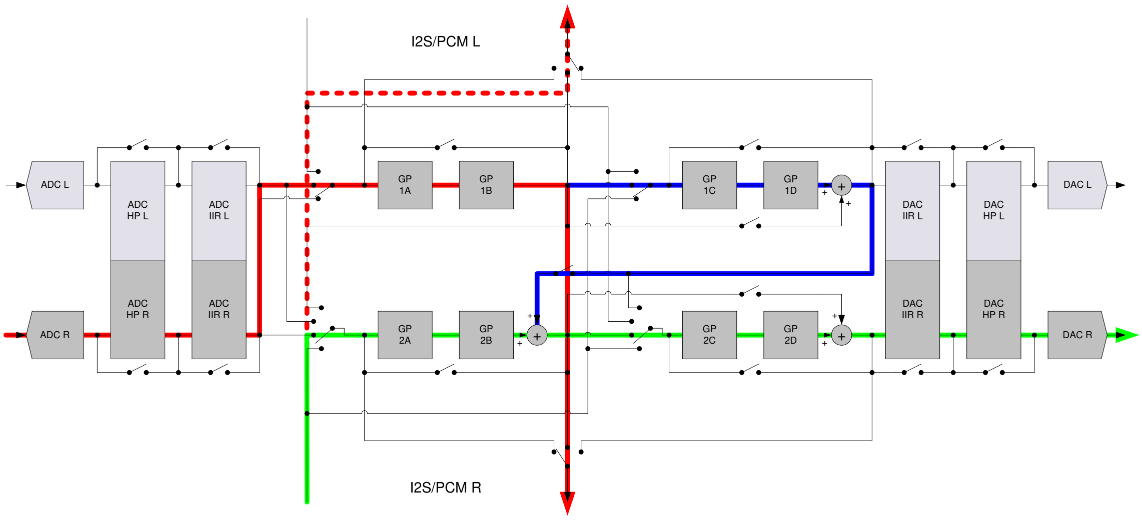


Figure 32: Transmit (Red), Receive (Green) and Sidetone (Blue) Sound Filtering for Phone Applications

9 INTERFACES

9.1 Digital Audio Interface (DAI)

Audio data is transferred to and from DA7211 via a serial 2-wire digital audio interface, which is enabled with bit DAI_EN. It is compatible with the Phillips I2S bus specification in normal, left justified, and right justified modes, and operates in both master and slave modes. In addition to I2S, the codec supports the DSP/PCM format of Bluetooth and mobile phone voice links, and offers a multi device TDM mode. The four bus lines are the clock (CLK), the serial data-in line (DATAIN), the serial data-out line (DATAOUT), and the word select line (WCLK).

For voice stream monitoring within dual processor architectures, DA7211 includes loop back modes that allow merging of the mono (left) RX and TX data into the PCM/I2S TX data stream configured via control DAI_OUT_R_SRC (address 0x25, Table 72).

Serial data and control signals are clocked onto the bus at the falling edge of the CLK clock signal. This guarantees that they are stable at the rising edge of CLK. The serial data is sampled into DA7211 on the rising edge of the CLK clock signal.

The interface is enabled via DAI_EN (address 0x28, Table 75) and can operate as either the bus master or as a slave (see control DAI_MODE (address 0x26, Table 73). In master mode, DA7211 generates the WCLK and CLK signals, whereas in the default slave mode these are inputs to the device. If the output from the ADC is not required, the serial data output from this pin can be disabled using control DAI_OE (address 0x28, Table 75).

The device may also be used in a system where several devices are connected to the master, using Time Division Multiplexing (TDM). The serial input and output data for each device is valid at a certain offset from the start of the frame. The serial data output from the device is tri-stated until the data from the device is valid, thus allowing several devices to have their serial data out pins connected together.

9.1.1 Operation Modes DAI Interface

Serial data is transferred as two's complement with the MSB first. The protocol format is selected via control DAI_FORMAT (address 0x28, Table 75). DA7211 is configured to operate with data word lengths of 16, 20, 24, or 32 bits using control DAI_WORD (address 0x26, Table 73).

In master mode the device can be configured via DAI_FRAME (address 0x26, Table 73) to generate either twice the selected word-length bit clocks per frame, or 256, 128, or 64 bit clocks per frame. In slave modes, the device may be clocked by any number of bit clocks per frame provided that there are sufficient clocks to transfer all the data bits, which are defined by the word length configuration register.

In loop mode, the RX right data overrides available TX left data using control DAI_SRC_SEL (address 0x25, Table 72).

9.1.2 Right Justified Mode

In right-justified mode the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. The LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

WCLK = 1; left channel data
WCLK = 0: right channel data

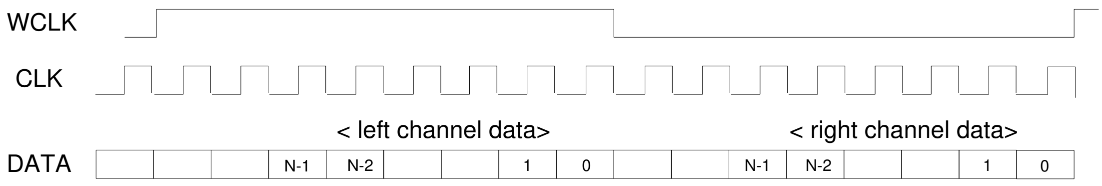


Figure 33: Right Justified Format

9.1.3 Left Justified Mode

In left-justified mode the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock.

The MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

WCLK = 1; left channel data
WCLK = 0: right channel data

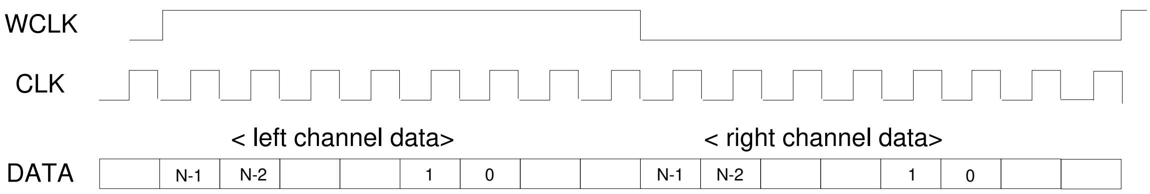


Figure 34: Left Justified Format

9.1.4 I2S Mode

In I2S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock.

Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

WCLK = 1; right channel data
WCLK = 0: left channel data

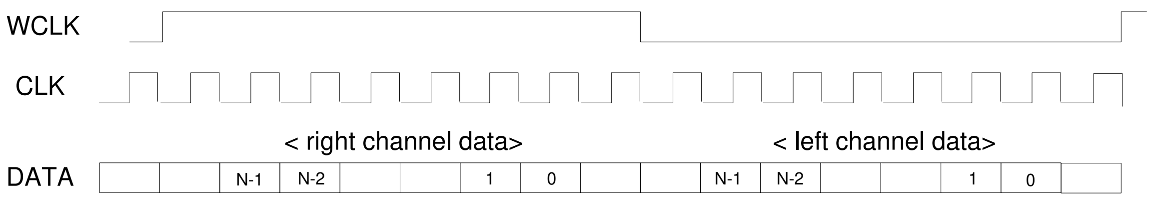


Figure 35: I2S Format

9.1.5 DSP Mode

In DSP mode, the rising edge of the word clock starts the data transfer, first with the left channel data, and followed immediately by the right channel data. Each data bit is valid on the falling edge of the bit clock.

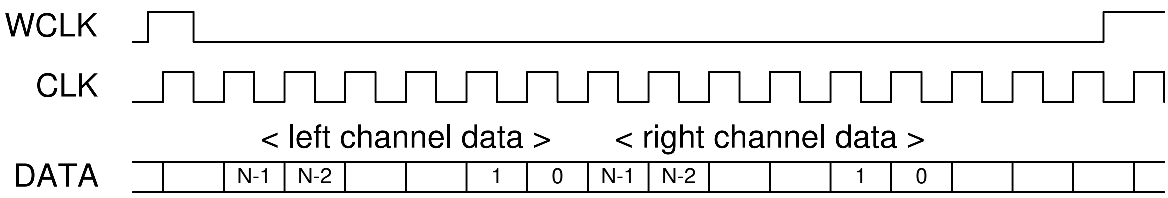


Figure 36: DSP Format

9.1.6 TDM Mode

TDM modes are implemented by defining the data to be valid a certain number of bit clock periods after the start of the frame. This is configured using the offset value DAI_TDM_OFFS (address 0x27, Table 74). It is recommended that TDM is used in either the Left Justified or DSP mode.

In the Left Justified TDM mode, the left channel data is valid DAI_TDM_OFFS clock cycles after the rising edge of the word clock, and the right channel data is valid after the same DAI_TDM_OFFS number of clock cycles after the falling edge of the word clock.

In the DSP TDM mode, the left channel data is valid DAI_TDM_OFFS clock cycles after the rising edge of the word clock pulse, and the right channel data is valid immediately after the left channel data. The number of bits of the data is determined by the word length setting in the configuration registers. The serial data output pin will be tri-stated when the output is not valid.

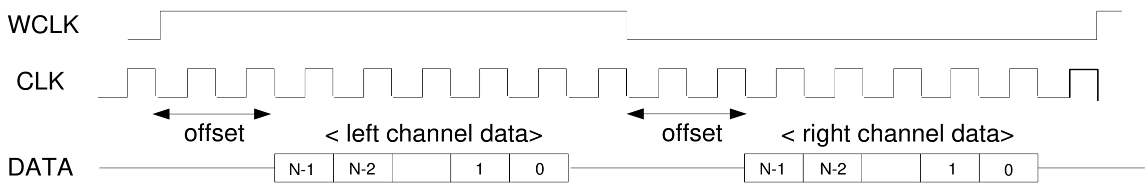


Figure 37: TDM Left Justified Format

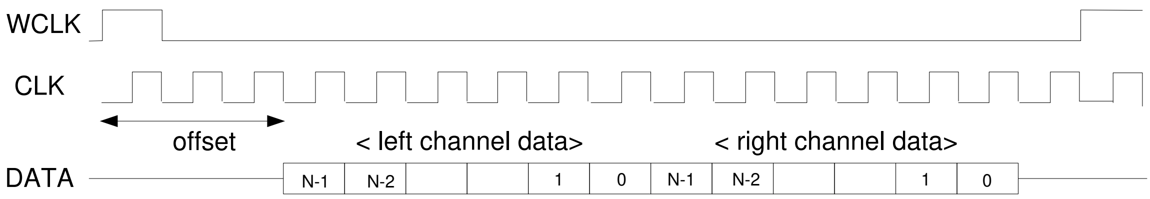


Figure 38: TDM DSP Format

TDM mode is enabled via DAI_TDM (address 0x28 Table 75) and may be configured to operate in mono only using the control DAI_TDM_MONO (address 0x26 Table 73). In this case, only one channel data is received from the bus and placed on the bus. Other devices may place data on the bus immediately after the left channel data.

9.1.7 Clocking Schemes

The internal system clock of the DA7211 runs at either 12.288 MHz or 11.2896 MHz. Which of these two system clock speeds is used depends on the audio sample rate as shown in Table 28. However, the external MCLK input choice has a number of options that depend on the sample rate, the MCLK_RANGE setting, whether the device is operating in Master or Slave Mode, and whether the PLL has been enabled.

For all DA7211 operations, the device must be started with an external MCLK input to allow register settings to be made. The DA7211 will not start up correctly unless this external clock is available. The initial frequency of the MCLK input during register set up is unimportant as long as it is within the 10 to 80 MHz range, but the frequency must be valid for DAC, ADC and filter operation.

Note: In PLL-enabled modes, register writes are clocked into the register map by the control interface clock (SK) until the PLL clock is locked and available.

Table 28: Internal System Clock Frequency

Sample Rate (kHz)	System Clock Rate FSYS (MHz)	ADC/DAC Clock Rate FSDM (MHz)
8	12.288	3.072
16	12.288	3.072
32	12.288	3.072
48	12.288	3.072
96	12.288	3.072
11.025	11.2896	2.8224
25.05	11.2896	2.8224
44.1	11.2896	2.8224
88.2	11.2896	2.8224

Table 29: Block Enable and System Standby Bits

I/O	Block Enable Register Bit	SC_MST_EN = 1 Required to Enable I/O Block Bit?	Start-Up Register Bit for Setting I/O to Standby
MIC_L	0x07[7]	Yes	0x05[0]
MIC_R	0x08[7]	Yes	0x05[1]
AUX1_L	0x09[7]	Yes	0x05[3]
AUX1_R	0x0A[7]	Yes	0x05[2]
ADC_L	0x10[3]	Yes	0x05[5]
ADC_R	0x10[7]	Yes	0x05[6]
OUT1_L	0x1E[7]	Yes	0x04[0]
OUT1_R	0x1F[7]	Yes	0x04[1]
HP_L	0x23[7]	Yes	0x04[3]
HP_R	0x23[3]	Yes	0x04[4]
DAC_L	0x17[7]	Yes	0x04[5]
DAC_R	0x17[3]	Yes	0x04[6]
INMIX_L mixer	0x0D[7]	No	n/a
INMIX_R mixer	0x0E[7]	No	n/a
OUT_L mixer	0x1C[7]	No	n/a

OUT_R mixer	0x1D[7]	No	n/a

Table 29 summarises the registers bits that must be enabled before SC_MST_EN is enabled if that block operation is required. Each block can be set in and out of standby after SC_MST_EN = 1.

9.1.8 Master Mode

In Master mode (controlled by DAI_MODE - address 0x26, Table 73) DA7211 can generate all supported audio sampling rates directly from a provided MCLK signal at either 12.288 MHz or 11.2896 MHz. In this case the PLL is not required and it should be bypassed and disabled with PLL_EN (address 0x2C, Table 79).

DA7211 can also generate all internal clocks without offset, as well as the sample rate, the CLK signal, and the WCLK signal from an MCLK signal in the range of 10 MHz to 80 MHz. This is done using the embedded fractional-N PLL (see controls MCLK_RANGE and PLL_DIV_L to PLL_DIV_H.

Table 30: ADC and DAC Clock Frequencies

Sample Rate [kHz]	Voice Mode (Note 1)	ADC Decimation	DAC SDM Oversample	SDM Rate Fs	FSDM Frequency [kHz]
8		96	32	384	3072
8	Y	96	16	384	3072
11.025	Y	64	32	256	2822.4
12	Y	64	32	256	3072
16		48	16	192	3072
16	Y	48	8	192	3072
22.05		32	16	128	2822.4
24		32	16	128	3072
32		24	8	96	3072
44.1		16	8	64	2822.4
48		16	8	64	3072
96 Note 2		8	4	32	2822.4

Note 1 Voice filter has stopband attenuation of >75 dB. The IIR engine implements voice filtering, or 5-band equalisation. For rates other than 44.1 kHz, the 5-band equalisation turnover frequencies scale with the sampling rate.

Note 2 No TDM on digital audio interface.

Table 31: Master Mode PLL-DIV Look Up Table

Input MCLK [MHz]	PLL_DIV_H	PLL_DIV_M	PLL_DIV_L	Audio Frequency [kHz]
12.0	0xE8	0x6C	0x2	44.1 (Note 1)
12.0	0xF3	0x12	0x7	48.0 (Note 2)
13.0	0xDF	0x28	0xC	44.1 (Note 1)
13.0	0xE8	0xFD	0x5	48.0 (Note 2)
13.5	0xDB	0x0A	0xD	44.1 (Note 1)
13.5	0xE4	0x82	0x3	48.0 (Note 2)
14.4	0xD4	0x5A	0x2	44.1 (Note 1)
14.4	0xDD	0x3A	0x0	48.0 (Note 2)
19.2	0xBB	0x43	0x9	44.1 (Note 1)
19.2	0xC1	0xEB	0x8	48.0 (Note 2)
19.68	0xB9	0x6D	0xA	44.1 (Note 1)
19.68	0xBF	0xEC	0x0	48.0 (Note 2)
19.8	0xB8	0xFB	0xB	44.1 (Note 1)
19.8	0xBF	0x70	0x0	48.0 (Note 2)

Note 1 Including harmonics such as 11.025, 22.05 and 88.2 kHz sample rates.

Note 2 Including audio frequencies such as 8.0, 12.0, 16.0, 32.0, 24.0, 36.0, 48.0, 96.0 kHz sample rates.

Table 32: SRM Mode PLL-DIV Look Up Table

Input MCLK [MHz]	PLL_DIV_H	PLL_DIV_M	PLL_DIV_L
0.032768	0xD4	0x99	0x0
12.0	0xED	0xBF	0x5
13.0	0xE4	0x13	0x0
13.5	0xDF	0xC6	0x8
14.4	0xD8	0xCA	0x1
19.2	0xBE	0x97	0x9
19.68	0xBC	0xAC	0xD
19.8	0xBC	0x35	0xE

9.1.9 Programming Master and 32 kHz Mode – PLL Enabled

If DA7211 is to be used in Master Mode with the PLL, a clock signal must first be applied to the MCLK pin. The frequency of this clock must either be 32.768 kHz (32 kHz Mode), or within the range 10 to 80 MHz.

MCLK_RANGE (address 0x2B[5:4]) must be set to the appropriate frequency range at the MCLK pin.

The Sample Rate Matching (SRM) only needs to be enabled if 32 kHz Mode is being used. SRM is enabled by asserting MCLK_SRM_EN (address 0x26[7]).

For the PLL to assume initial lock, it is necessary to set the PLL division ratio bits in registers 0x29, 0x2A, 0x2B. The settings for PLL Master Mode differ from those of PLL 32 kHz Mode. For 32 kHz mode, MCLK_RANGE (address 0x2C[5:4]) = 00. For all other PLL Master Mode operations, MCLK_RANGE (address 0x2C[5:4]) = 01, 10 or 11. These settings will allow the PLL lock cycle to start in the correct frequency range. It is not necessary to assert MCLK_DET_ENA in PLL Master Mode as the CLK and WCLK outputs are produced by the DA7211 itself.

It is also necessary to assert vco_rst, 0x90[0] to ensure successful PLL lock. To access this bit is necessary to first enter the following register settings 0x8A = 8Bh and 0x8B =B4h.

As with non-PLL slave mode, to set the required sample rate, the correct clock division ratio must be set within register 0x2C[3:0], (see Table 35).

Table 33: PLL Master Mode Register Setting Recommendations

0x2C PLL	4	MCLK_SHAPE_EN	0	Enable MCLK shaper for low level non TTL signals - optional
	5	MCLK_DET_EN	0	Enable automatic detection of sample rate
	6	MCLK_SRM_EN	0	Enable DAI sample rate tracking, sample rate defined by FS
	7	PLL_EN	1	0: Disable and bypass PLL 1: Enable PLL

Renesas recommend that good quality external clocks are used to supply the DAI, but if the only available MCLK source is of poor quality, it can be improved by using the optional bit MCLK_SHAPE_EN.

Figure 39 shows a basic start-up up configuration sequence for PLL master mode.

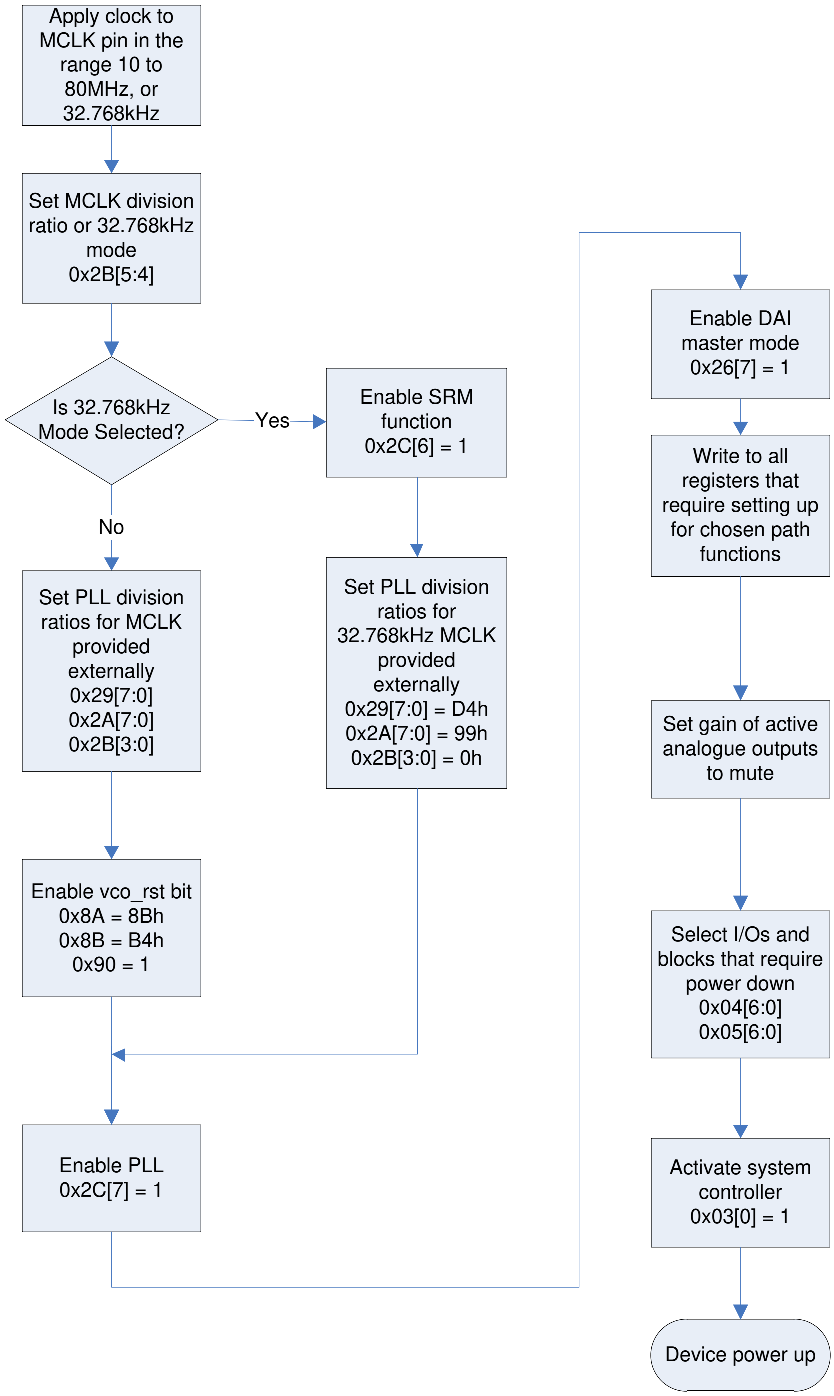


Figure 39: PLL Master Mode Start Up Sequence

9.2 Slave Mode

Slave mode is selected by setting DAI_MODE (address 0x26, Table 73) = 0. The CLK and WCLK signals are supplied by the application.

9.2.1 Conditions

(i) Sample Rate Matching (SRM) Disabled

SRM is not needed if the audio sample rate is known and the CLK and WCLK signals are derived from the same master clock as the MCLK input. In this case CLK and WCLK are synchronised with MCLK, so the SRM function should be disabled and the PLL_DIV registers programmed as shown in Table 32. Alternatively, lowest power dissipation can be achieved if the MCLK frequency can be set to 256×Fs (12.288 MHz or 11.2896 MHz) and the PLL switched off.

(ii) Sample Rate Matching (SRM) Enabled

SRM is needed if the sample rate on the audio interface is unknown, or the CLK and WCLK signals are derived from a different clock domain to the MCLK input.

SRM (MCLK_SRM_EN = 1 address 0x2C, Table 79) keeps the internal clocks synchronised with WCLK.

If the sample rate is known, the value of FS should be set accordingly. If the sample rate is not known, it can be derived from WCLK and automatically programmed by asserting MCLK_DET_EN (address 0x2C, Table 79).

The Sample Rate Matching (SRM) functions by pulling the PLL frequency away from the nominal value specified by the PLL control registers (addresses 0x29 to 0x2B, Table 78). In this mode the register settings shown in Table 33 should be used. Enabling the SRM offers maximum flexibility for clocking schemes as it removes the need to have common clock domains for the application processor and audio codec processor.

9.2.2 Programming Slave Mode – PLL Not Enabled

In either Slave or Master mode, and when the PLL is not enabled, an exact multiple of (256 * Fs) must be input to the MCLK pin (see Table 34).

In order to set the correct clock division ratio within the DA7211 for a particular sample rate, it is necessary to set the correct sample rate setting in the FS register (address 0x2C [3:0], Table 79). The possible sample rates and MCLK frequencies are shown in Table 34.

Table 34: MCLK Frequencies in Non-PLL Slave Mode

Sample Rate (kHz)	MCLK (MHz)			
	MCLK_RANGE = 00	MCLK_RANGE = 01	MCLK_RANGE = 10	MCLK_RANGE = 11
8	n/a	12.288	24.576	49.152
16	n/a	12.288	24.576	49.152
32	n/a	12.288	24.576	49.152
48	n/a	12.288	24.576	49.152
96	n/a	12.288	24.576	49.152
11.025	n/a	11.2896	22.5792	45.1584
25.05	n/a	11.2896	22.5792	45.1584

44.1	n/a	11.2896	22.5792	45.1584
88.2	n/a	11.2896	22.5792	45.1584

Table 35: Non-PLL Slave Mode and PLL Master Mode Sample Rate Settings

0x2C[3:0]	Sample Rate
0000	Not used
0001	8 kHz
0010	11.025 kHz
0011	12 kHz
0100	Not used
0101	16 kHz
0110	22.05 kHz
0111	24 kHz
1000	Not used
1001	32 kHz
1010	44.1 kHz
1011	48 kHz
1100	Not used
1101	Not used
1110	88.1 kHz
1111	96 kHz

If only analogue paths are required then it is possible to use MCLK = 32.768 kHz for the register setup. For all other 32.768 kHz modes, the PLL must be enabled for any operation that requires ADC, DAC or digital filtering.

Figure 40: Non-PLL Mode Start-Up shows a basic start-up up configuration sequence for non-PLL slave mode.

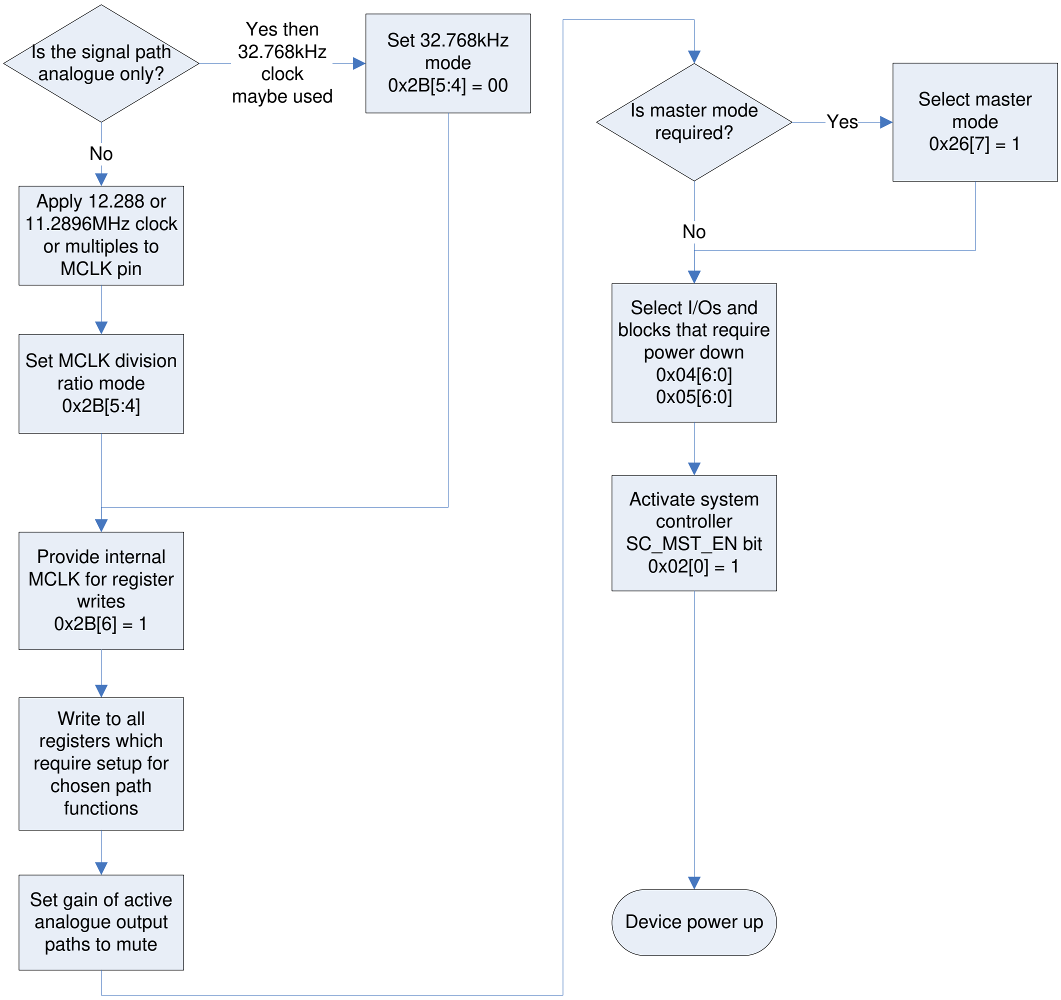


Figure 40: Non-PLL Mode Start-Up Sequence

9.2.3 Programming Slave Mode – PLL Enabled

If PLL mode is enabled and the MCLK_DET_EN (0x2C[5]) bit is set, the value read from this register will be the automatically detected sample rate from the PLL track circuitry. Register 0x2C[3:0] can be set to 0000 in this case. Sample rate changes will be updated on the positive edge of DAI clock.

It is also recommended that the Sample Rate Matching (SRM) tracking function is enabled (register 0x2C[6]) when the PLL is used in slave mode. This means that any changes in the sample rate can be tracked automatically without any input from the controlling processor. Failure to enable SRM can result in intermittent audible clicking on the DAC outputs.

In order to allow the PLL to assume initial lock, it is necessary to set the PLL division ratio bits and the MCLK_RANGE in registers 0x29, 0x2A, 0x2B and 0x2C. These functions cause the PLL lock cycle to start in the correct frequency range. The division ratio settings for SRM mode differ from those of master mode (see section 9.1.8).

It is also necessary to set the vco_rst bit, 0x90[0] = 1 to ensure a successful PLL lock. To access this bit, it is necessary to first enter the following register settings: 0x8A = 8Bh and 0x8B = B4h.

Table 36: SRM Mode PLL Division Ratio Settings

MCLK (MHz)	PLL_DIV_H 0x29[7:0]	PLL_DIV_M 0x2A[7:0]	PLL_DIV_L 0x2B[3:0]
0.032768	0xD4	0x99	0x0
12.0	0xED	0xBF	0x5
13.0	0xE4	0x13	0x0
13.5	0xDF	0xC6	0x8
14.4	0xD8	0xCA	0x1
19.2	0xBE	0x79	0x7
19.68	0xBC	0xAC	0xD
19.8	0xBC	0x35	0xE

Table 35 contains the division ratios for a selection of common oscillator frequencies that can be used for generating the internal 256 * Fs master clock from the PLL. If an uncommon frequency is used, the division ratio values can be calculated.

The feedback divide ratio PLL_DIV is a 20-bit two's complement value in the range -0.5 to +0.5, which can be calculated using

$$PLL\_DIV = \frac{\left(\frac{8 * FSYS}{FMCLK}\right) - 9}{16}$$

For example, if FMCLK = 13.7 MHz and FSYS = 12.288 MHz then PLL_DIV = -0.114033, which equals 0xE2CEC as a 20-bit two's-complement number. This value is written to the three PLL_DIV registers:

- PLL_DIV_H (0x29) = E2h
- PLL_DIV_M (0x2A) = CEh
- PLL_DIV_L (0x2B[3:0]) = Ch

Note

A PLL division ratio calculation tool is available on request.

Renesas recommend that good quality external clocks are used to supply the DAI, but if the only available MCLK source is of poor quality. It can be improved by using the optional bit MCLK_SHAPE_EN.

Table 37: Slave Mode PLL-Enabled Register Setting Recommendations

0x2C PLL	4	MCLK_SHAPE_EN	0	Enable MCLK shaper for low level non TTL signals - optional
	5	MCLK_DET_EN	1	Enable automatic detection of sample rate
	6	MCLK_SRM_EN	1	Enable DAI sample rate tracking, sample rate defined by FS
	7	PLL_EN	1	0: Disable and bypass PLL 1: Enable PLL

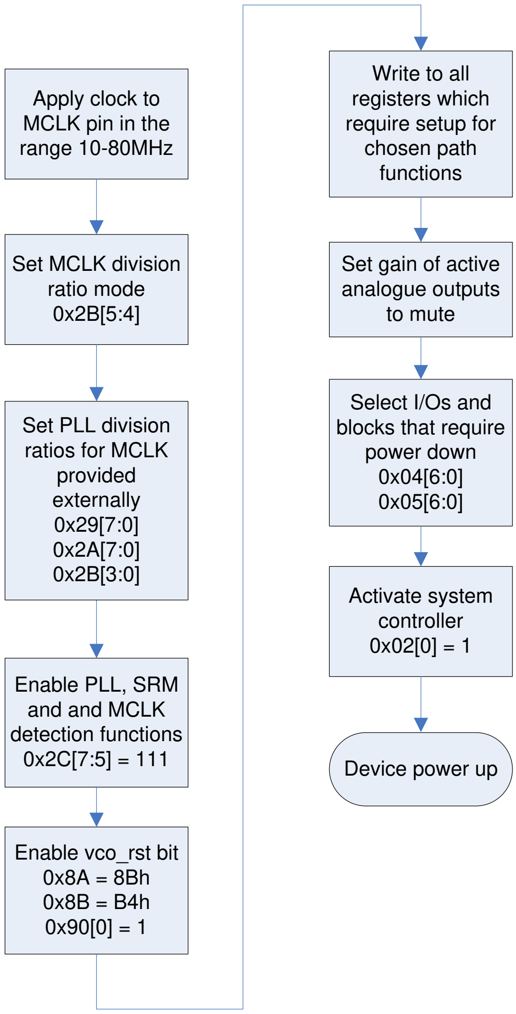


Figure 41: PLL Slave Mode Start-Up Sequence

9.2.4 32 kHz Master or Slave Mode

With the 32 kHz mode enabled, the DA7211 is able to accept a standard watch-crystal frequency (32.768 kHz) input on MCLK. It does this by enabling an on-chip reference oscillator and using the SRM system to track the MCLK input. The 32 kHz mode is enabled by setting MCLK_RANGE (address 0x2B, Table 78), and since the SRM is required, the PLL_DIV settings in Table 31 should be used.

The 32 kHz mode works with the DA7211 in Master (see note below) or Slave modes, but it is not possible to use the automatic detection of audio sample rate.

NOTE
In 32 kHz Master Mode the sample rates 11.025, 22.05, 44.1 and 88.2 kHz will have a maximum offset of 0.14%.

9.2.5 Phase Locked Loop (PLL)

A PLL is integrated into the codec. This uses standard oscillator master clock signals to generate the target audio sample rates and all internal clock signals. If no 256 * Fs master clock signal is provided, the PLL can be enabled with control PLL_EN (address 0x2C, Table 79). The PLL supports a wide range of common oscillator frequencies between 10 and 20 MHz (see Table 31)

The PLL can also be fed from the 2nd or 4th harmonics of these frequencies via an input clock divider (configured using control MCLK_RANGE (address 0x2B Table 78). The master clock input can be either a standard TTL signal. It can also be any kind of saw tooth, square or sine wave if the embedded signal shaper is enabled via control MCLK_SHAPE_EN (address 0x2C, Table 79). If the host provides the 256 * FS master clock, the PLL can be disabled to reduce dissipation power.

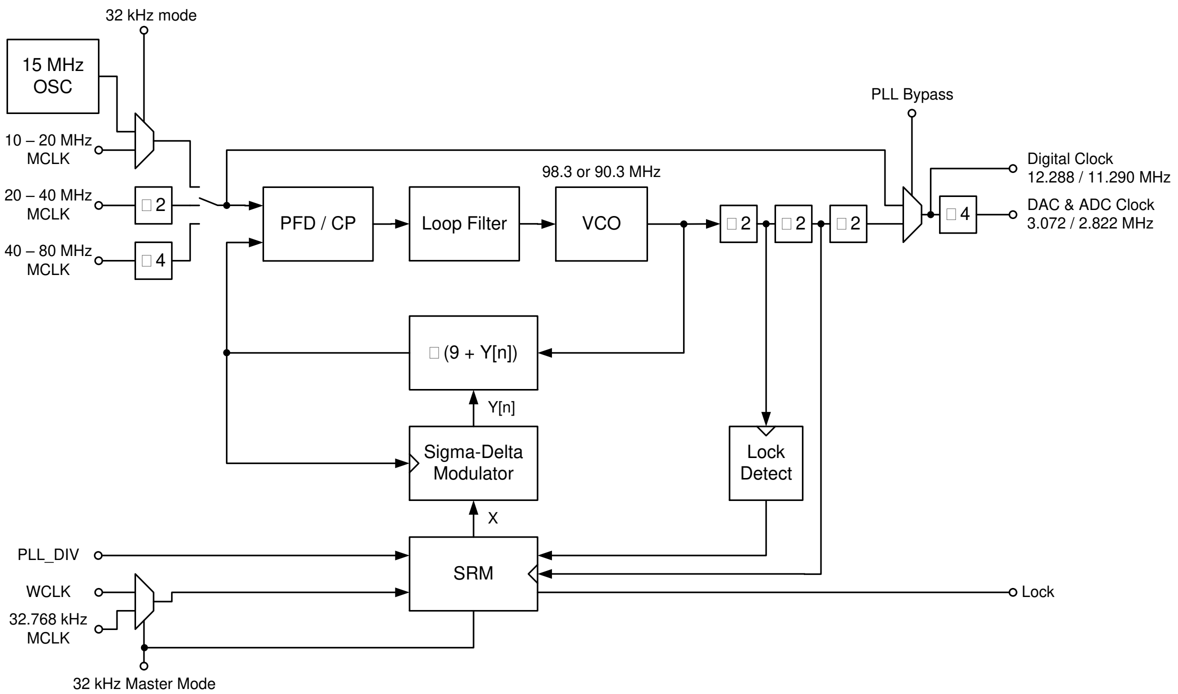


Figure 42: PLL Block Diagram

9.2.6 Control Interface

The DA7211 has a 2-wire control interface.

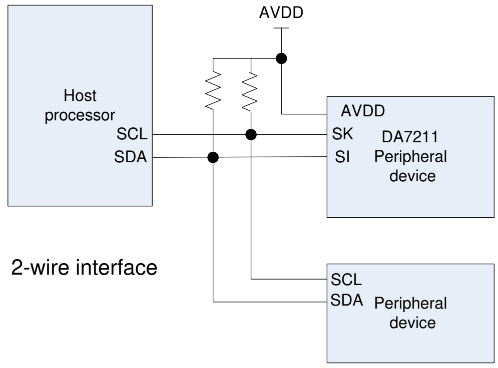


Figure 43: Schematic of a 2-Wire Control Bus

9.2.7 2-Wire Communication

The 2-wire interface supports 7-bit address protocol. DA7211 responds to the device address 001 1010.

SK provides the 2-wire clock and SI carries all the control bidirectional 2-wire data. The 2-wire interface is open-drain, supporting multiple devices on a single line. The attached devices only drive the bus lines low by connecting them to ground.

The bus lines are pulled high by pull-up resistors (2 KΩ to 20 KΩ range). As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz.

The exact frequency can be determined by the application and does not have any relation to the DA7211 internal clock signals. DA7211 will follow the host clock speed within the described limitations, and does not initiate any clock arbitration or slow down.

In high speed mode, the maximum frequency of the bus is 1.7 MHz. This mode is supported if the SK line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the SI pin to decrease the rise time of the data. In this mode the SI line on DA7211 is able to sink up to 12 mA. In all other respects the high speed mode behaves as the standard/fast mode.

Communication on the 2-wire bus always takes place between two devices, one acting as the master and the other as the slave, but DA7211 will only operate as a slave. The 2-wire interface has direct (linear) access to the whole DA7211 register space (except 0x00 and 0x80). This is achieved by using the MSB of the 2-wire 8 bit register address as a selector of the register page.

9.2.8 Details of the 2-Wire Control Bus Protocol

Data is transmitted access the 2-wire bus in groups of eight bits. To send a bit, the SI line is driven towards the intended state while the SK is LOW (a low on SI indicates a zero bit). Once the SI has settled, the SK line is brought HIGH and then LOW. This pulse on SK clocks the SI bit into the receiver's shift register.

A two byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is MSB transmitted first for both read and write operations. All transmission begins with the START condition from the master during the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SI line while the SK is in the high state (a STOP condition is indicated by a low to high transition on the SI line while the SK is in the high state).

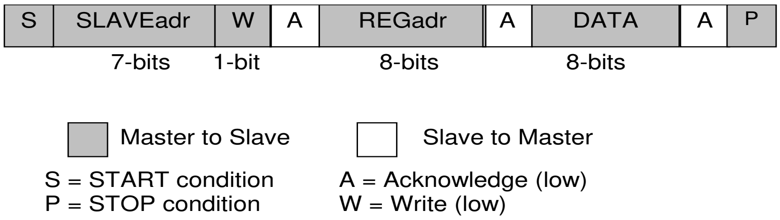


Figure 44: 2-Wire Byte Write (SI/DATA Line)

When the host reads data from a register it first has to write access DA7211 with the target register address. It then read accesses DA7211 with a Repeated START or alternatively a second START condition. After receiving the data the host sends no acknowledge and terminates the transmission with a STOP condition.

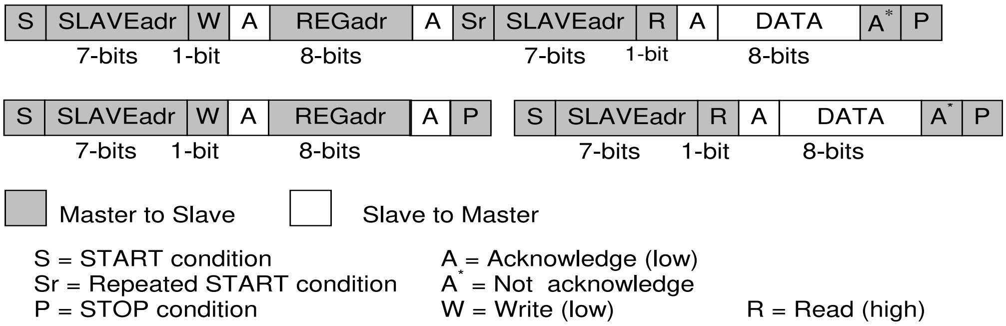


Figure 45: Examples of 2-Wire Byte Read (SI/DATA Line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not acknowledge after receipt of the data word. The 2-wire control block then increments the address pointer to the next 2-wire address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a NACK ('Not Acknowledge') directly after the receipt of data, followed by a subsequent STOP condition.

If a non-existent 2-wire address is read out then the DA7211 will return code zero.

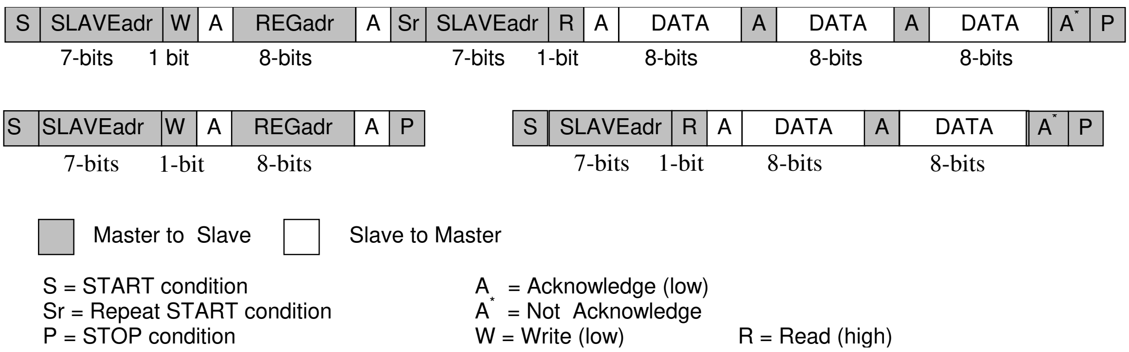


Figure 46: Examples of 2-Wire Page Read (SI/DATA Line)

Note - The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the Master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

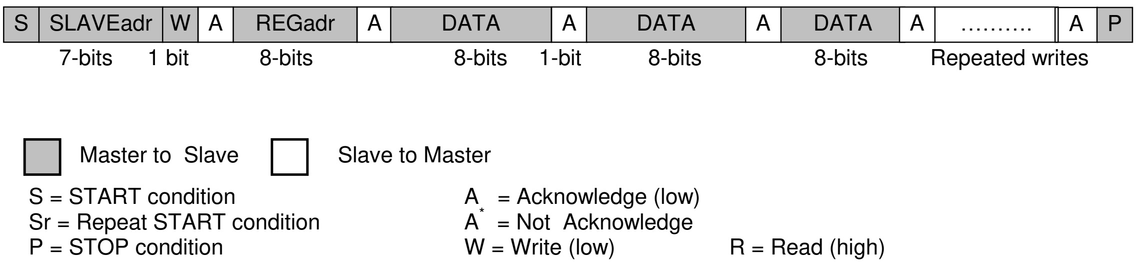


Figure 47: 2-Wire Page Write (SI/DATA Line)

Using the control WRITE_MODE (address 0x01, Table 39) the device can be configured to accept an alternate write mode where the host transmits alternate addresses and

write data. This allows the host to perform several write operations to non consecutive registers. Data will be stored at the previously received register address:

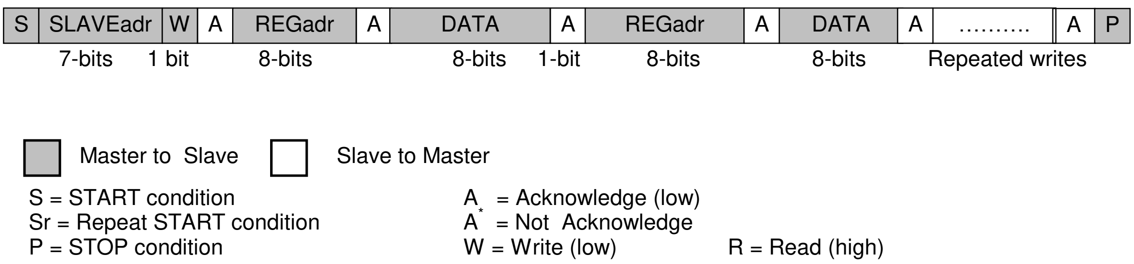


Figure 48: 2-Wire Repeated Write (SI/DATA Line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

10 Register Definitions

WARNING: Any writes to RESERVED registers or bits can result in unexpected operation. This section gives an overview of all user accessible registers in the Register map table.

Detailed descriptions are given in Register description tables, which are grouped per functional block.

10.1 Register Map

Table 38: Register Map

Address	Function	7	6	5	4	3	2	1	0	Default
1	CONTROL	WRITE_MODE				NOISE_SUP	BIAS_EN	V_IO		0b00010000
2	STATUS					MUTING	SOFTMUTED	I2S_LOCK	PLL_LOCK	0b00000000
3	STARTUP1	SC_CLK_DIS			SC_OVERRIDE				SC_MST_EN	0b00000000
4	STARTUP2		STARTUP2[6:0]							0b00000000
5	STARTUP3		STARTUP3[6:0]							0b00000000
7	MIC_L	MIC_L_EN	MICBIAS_EN	MICBIAS_SEL[1:0]		MIC_L_MUTE	MIC_L_VOL[2:0]			0b00000000
8	MIC_R	MIC_R_EN				MIC_R_MUTE	MIC_R_VOL[2:0]			0b00000000
9	AUX1_L	AUX1_L_EN		AUX1_L_VOL[5:0]						0b00010000
0a	AUX1_R	AUX1_R_EN		AUX1_R_VOL[5:0]						0b00010000
0c	IN_GAIN	INPGA_R_VOL[3:0]				INPGA_L_VOL[3:0]				0b00000000
0d	INMIX_L	IN_L_EN			IN_L_OUTMIX_L		IN_L_A1_L	IN_L_MIC_R	IN_L_MIC_L	0b00000000
0e	INMIX_R	IN_R_EN		IN_R_IN_L	IN_R_OUTMIX_R		IN_R_A1_R	IN_L_MIC_L	IN_L_MIC_R	0b00000000
0f	ADC_HPF	ADC_VOICE_EN	ADC_VOICE_F0[2:0]			ADC_HPF_EN		ADC_HPF_F0[1:0]		0b00001000
10	ADC	ADC_R_EN	ADC_R_MUTE			ADC_L_EN	ADC_L_MUTE		ALC_EN	0b00000000
11	ADC_EQ1_2	ADC_EQ2_VOL[7:4]				ADC_EQ1_VOL[3:0]				0b00000000
12	ADC_EQ3_4	ADC_EQ4_VOL[7:4]				ADC_EQ3_VOL[3:0]				0b00000000
13	ADC_EQ5	ADC_EQ_EN		ADC_EQ_GAIN[1:0]		ADC_EQ5_VOL[3:0]				0b00000000
14	DAC_HPF	DAC_VOICE_EN	DAC_VOICE_F0[2:0]			DAC_HPF_EN	DAC_MUTE	DAC_HPF_F0[1:0]		0b00001000
15	DAC_L	DAC_L_INV	DAC_L_GAIN[6:0]							0b00010000
16	DAC_R	DAC_R_INV	DAC_R_GAIN[6:0]							0b00010000
17	DAC_SEL	DAC_R_EN	DAC_R_SRC[2:0]			DAC_L_EN	DAC_L_SRC[2:0]			0b01010100
18	SOFT_MUTE	SOFT_MUTE	RAMP_EN				MUTE_RATE[2:0]			0b01000000
19	DAC_EQ1_2	DAC_EQ2_VOL[7:4]				DAC_EQ1_VOL[3:0]				0b00000000
1a	DAC_EQ3_4	DAC_EQ4_VOL[7:4]				DAC_EQ3_VOL[3:0]				0b00000000
1b	DAC_EQ5	DAC_EQ_EN		DAC_EQ_GAIN		DAC_EQ5_VOL[3:0]				0b00000000
1c	OUTMIX_L	OUT_L_EN	OUT_L_INV		OUT_L_DAC_L	OUT_L_IN_R	OUT_L_IN_L		OUT_L_A1_L	0b00000000
1d	OUTMIX_R	OUT_R_EN	OUT_R_INV		OUT_R_DAC_R	OUT_R_IN_R	OUT_R_IN_L		OUT_R_A1_R	0b00000000
1e	OUT1_L	OUT1_L_EN	OUT1_L_SE	OUT1_L_VOL[5:0]						0b00110101
1f	OUT1_R	OUT1_R_EN	OUT1_R_SE	OUT1_R_VOL[5:0]						0b00110101
21	HP_L_VOL			HP_L_VOL[5:0]						0b00010000
22	HP_R_VOL			HP_R_VOL[5:0]						0b00010000
23	HP_CFG	HP_R_EN	HP_MODE	STEREO_TRACK	HP_HIGHZ_R	HP_L_EN		HP_2CAP_MODE	HP_HIGHZ_L	0b00000010
24	ZEROX	HPZX_R_EN	HPZX_L_EN	OUTZX_R_EN	OUTZX_L_EN	INZX_R_EN	INZX_L_EN	A1ZX_R_EN	A1ZX_L_EN	0b00000000
25	DAI_SRC_SEL	DAI_IN_R_MIX	DAI_OUT_R_SRC[2:0]			DAI_IN_L_MIX	DAI_OUT_L_SRC[2:0]			0b01110110
26	DAI_CFG1	DAI_MODE			DAI_TDM_MONO	DAI_FRAME[1:0]		DAI_WORD[1:0]		0b00000000
27	DAI_CFG2	DAI_TDM_OFFS[7:0]								0b00000000
28	DAI_CFG3	DAI_EN				DAI_OE	DAI_TDM	DAI_FORMAT[1:0]		0b00001000
29	PLL_DIV1	PLL_DIV_H[7:0]								0b00000000
2a	PLL_DIV2	PLL_DIV_M[7:0]								0b00000000
2b	PLL_DIV3		PLL_BYP	MCLK_RANGE[1:0]		PLL_DIV_L[3:0]				0b00010000
2c	PLL	PLL_EN	MCLK_SRM_EN	MCLK_DET_EN	MCLK_SHAPE_EN	FS[3:0]				0b00001010
2d	GP1A_A0L	GP1A_A0L[7:0]								0b00000000
2e	GP1A_A0H	GP1A_A0H[7:0]								0b01000000
2f	GP1B_A0L	GP1B_A0L[7:0]								0b00000000
30	GP1B_A0H	GP1B_A0H[7:0]								0b01000000
31	GP2A_A0L	GP2A_A0L[7:0]								0b00000000

32	GP2A_A0H	GP2A_A0H[7:0]	0b01000000
33	GP2B_A0L	GP2B_A0L[7:0]	0b00000000
34	GP2B_A0H	GP2B_A0H[7:0]	0b01000000
35	GP1C_A0L	GP1C_A0L[7:0]	0b00000000
36	GP1C_A0H	GP1C_A0H[7:0]	0b01000000
37	GP1D_A0L	GP1D_A0L[7:0]	0b00000000
38	GP1D_A0H	GP1D_A0H[7:0]	0b01000000
39	GP2C_A0L	GP2C_A0L[7:0]	0b00000000
3a	GP2C_A0H	GP2C_A0H[7:0]	0b01000000
3b	GP2D_A0L	GP2D_A0L[7:0]	0b00000000
3c	GP2D_A0H	GP2D_A0H[7:0]	0b01000000
3d	GP1A_A1L	GP1A_A1L[7:0]	0b00000000
3e	GP1A_A1H	GP1A_A1H[7:0]	0b00000000
3f	GP1B_A1L	GP1B_A1L[7:0]	0b00000000
40	GP1B_A1H	GP1B_A1H[7:0]	0b00000000
41	GP2A_A1L	GP2A_A1L[7:0]	0b00000000
42	GP2A_A1H	GP2A_A1H[7:0]	0b00000000
43	GP2B_A1L	GP2B_A1L[7:0]	0b00000000
44	GP2B_A1H	GP2B_A1H[7:0]	0b00000000
45	GP1C_A1L	GP1C_A1L[7:0]	0b00000000
46	GP1C_A1H	GP1C_A1H[7:0]	0b00000000
47	GP1D_A1L	GP1D_A1L[7:0]	0b00000000
48	GP1D_A1H	GP1D_A1H[7:0]	0b00000000
49	GP2C_A1L	GP2C_A1L[7:0]	0b00000000
4a	GP2C_A1H	GP2C_A1H[7:0]	0b00000000
4b	GP2D_A1L	GP2D_A1L[7:0]	0b00000000
4c	GP2D_A1H	GP2D_A1H[7:0]	0b00000000
4d	GP1A_A2L	GP1A_A2L[7:0]	0b00000000
4e	GP1A_A2H	GP1A_A2H[7:0]	0b00000000
4f	GP1B_A2L	GP1B_A2L[7:0]	0b00000000
50	GP1B_A2H	GP1B_A2H[7:0]	0b00000000
51	GP2A_A2L	GP2A_A2L[7:0]	0b00000000
52	GP2A_A2H	GP2A_A2H[7:0]	0b00000000
53	GP2B_A2L	GP2B_A2L[7:0]	0b00000000
54	GP2B_A2H	GP2B_A2H[7:0]	0b00000000
55	GP1C_A2L	GP1C_A2L[7:0]	0b00000000
56	GP1C_A2H	GP1C_A2H[7:0]	0b00000000
57	GP1D_A2L	GP1D_A2L[7:0]	0b00000000
58	GP1D_A2H	GP1D_A2H[7:0]	0b00000000
59	GP2C_A2L	GP2C_A2L[7:0]	0b00000000
5a	GP2C_A2H	GP2C_A2H[7:0]	0b00000000
5b	GP2D_A2L	GP2D_A2L[7:0]	0b00000000
5c	GP2D_A2H	GP2D_A2H[7:0]	0b00000000
5d	GP1A_B1L	GP1A_B1L[7:0]	0b00000000
5e	GP1A_B1H	GP1A_B1H[7:0]	0b00000000
5f	GP1B_B1L	GP1B_B1L[7:0]	0b00000000
60	GP1B_B1H	GP1B_B1H[7:0]	0b00000000
61	GP2A_B1L	GP2A_B1L[7:0]	0b00000000
62	GP2A_B1H	GP2A_B1H[7:0]	0b00000000
63	GP2B_B1L	GP2B_B1L[7:0]	0b00000000

64	GP2B_B1H	GP2B_B1H[7:0]								0b00000000
65	GP1C_B1L	GP1C_B1L[7:0]								0b00000000
66	GP1C_B1H	GP1C_B1H[7:0]								0b00000000
67	GP1D_B1L	GP1D_B1L[7:0]								0b00000000
68	GP1D_B1H	GP1D_B1H[7:0]								0b00000000
69	GP2C_B1L	GP2C_B1L[7:0]								0b00000000
6a	GP2C_B1H	GP2C_B1H[7:0]								0b00000000
6b	GP2D_B1L	GP2D_B1L[7:0]								0b00000000
6c	GP2D_B1H	GP2D_B1H[7:0]								0b00000000
6d	GP1A_B2L	GP1A_B2L[7:0]								0b00000000
6e	GP1A_B2H	GP1A_B2H[7:0]								0b00000000
6f	GP1B_B2L	GP1B_B2L[7:0]								0b00000000
70	GP1B_B2H	GP1B_B2H[7:0]								0b00000000
71	GP2A_B2L	GP2A_B2L[7:0]								0b00000000
72	GP2A_B2H	GP2A_B2H[7:0]								0b00000000
73	GP2B_B2L	GP2B_B2L[7:0]								0b00000000
74	GP2B_B2H	GP2B_B2H[7:0]								0b00000000
75	GP1C_B2L	GP1C_B2L[7:0]								0b00000000
76	GP1C_B2H	GP1C_B2H[7:0]								0b00000000
77	GP1D_B2L	GP1D_B2L[7:0]								0b00000000
78	GP1D_B2H	GP1D_B2H[7:0]								0b00000000
79	GP2C_B2L	GP2C_B2L[7:0]								0b00000000
7a	GP2C_B2H	GP2C_B2H[7:0]								0b00000000
7b	GP2D_B2L	GP2D_B2L[7:0]								0b00000000
7c	GP2D_B2H	GP2D_B2H[7:0]								0b00000000
7d	GPF_SRC1		GP_2AB_SRC[2:0]				GP_1AB_SRC[2:0]			0b01100100
7e	GPF_SRC2		GP_2CD_SRC[2:0]				GP_1CD_SRC[2:0]			0b01110101
7f	DSP_CFG		DSP_MIX[2:0]			GP_2CD_EN	GP_1CD_EN	GP_2AB_EN	GP_1AB_EN	0b00000000
81	CHIP_ID	MRC[3:0]				MMRC[3:0]				0b00010001
82	INTERFACE	IF_BASE_ADDR[2:0]								0b00101100
83	ALC_MAX		ALC_MERGE	ALC_MAX[5:0]						0b01000000
84	ALC_MIN			ALC_MIN[5:0]						0b00000000
85	ALC_NOIS			ALC_NOIS[5:0]						0b00000000
86	ALC_ATT	ALC_ATT[7:0]								0b00000000
87	ALC_REL	ALC_REL[7:0]								0b00000000
88	ALC_DEL	ALC_DEL[7:0]								0b00000000
8A	A_HID_UNLOCK	A_HID_UNLOCK[7:0]								0b00000000
8B	A_TEST_UNLOCK	A_TEST_UNLOCK[7:0]								0b00000000
8F	A_PLL0								SIGDEL DISABLE	0b00000000
90	A_PLL1								VCORST_EN	0b00000000
95	A_ADC0					ADC_T2				0b00000000
96	A_DAC0						VMID_BUFF_EN			0b00000000
A2	A_CPHP6	CP_RISE_TIME								0b10000000
A7	A_CP_MODE	A_CP_MODE[7:0]								0b01111110

10.2 Control and Status Registers

Table 39: CONTROL 0x01

Bit	Mode	Symbol	Description	Reset
7	R/W	WRITE_MODE	2-wire multiple write mode 0 = page Write Mode 1 = repeated Write Mode	0
6:4	R	Reserved	Reserved	001
3	R/W	NOISE_SUP	Enable noise suppression mode (see section 8.2.5)	0
2	R/W	BIAS_EN	Bias current to the entire chip 0 = bias off (device power down) 1 = supply bias current (device in operation)	0
1	R/W	VDDDIO_RANGE	VDDDIO voltage 0 = VDDDIO > 2.65 V 1 = VDDDIO <= 2.65 V Must be set to 1	0
0	R/W	REG_EN	Digital Regulator enable 0 = disable 1 = enable	0

Table 40: STATUS 0x02

Bit	Mode	Symbol	Description	Reset
7:4	R	Reserved	Reserved	0000
3	R	MUTING	0 = unmute 1 = mute	0
2	R	SOFTMUTED	0 = normal mute 1 = softmute (ref. SOFTMUTE section)	0
1	R	I2S_LOCK	Digital audio interface (DAI) lock status 0 = not locked 1 = locked to frame rate lock	0
0	R	PLL_LOCK	PLL status 0 = PLL not locked 1 = PLL locked	0

Table 41: STARTUP 1 0x03

Bit	Mode	Symbol	Description	Reset
7	W	SC_CLK_DIS	System Controller Clock Disable 0 = clock enabled 1 = clock disabled (provides power saving)	0
6:5	R	Reserved	Reserved	00
4	R/W	SC_OVERRIDE	Test enable that forces everything to be enabled instantly on the next clock cycle	0
3:1	R	Reserved	Reserved	00
0	R/W	SC_MST_EN	System Controller Master Enable. All subsystems should be enabled first before enabling this bit. 0 = everything off 1 = device active	0

Table 42: STARTUP 2 0x04

Bit	Mode	Symbol	Description	Reset
7	R	Reserved	Reserved	0
6:0	R/W	STARTUP2	Output standby control. 0 = normal 1 = standby [6] – DAC R standby [5] – DAC L standby [4] – HP R standby [3] – HP L standby [2] – Reserved [1] – OUT1R standby [0] – OUT1L standby	0000000

Table 43: STARTUP 3 0x05

Bit	Mode	Symbol	Description	Reset
7	R	Reserved	Reserved	0
6:0	R/W	STARTUP3	Input standby control. 0 = normal 1 = standby [6] – ADC R standby [5] – ADC L standby [4] – Reserved [3] – AUX1_R input standby [2] – AUX1_L input standby [1] – MIC_R input standby [0] – MIC_L input standby Note: Standby is to reduce the power consumption and not necessarily to mute the block.	0000000

10.3 Codec Registers

Table 44: MIC_L 0x07

Bit	Mode	Symbol	Description	Reset
7	R/W	MIC_L_EN	Enable left MIC amplifier 0 = disable 1 = enable (must be set beforeRes SC_MST_EN)	0
6	R/W	MICBIAS_EN	Enable MICBIAS supply 0 = disable 1 = enable	0
5:4	R/W	MICBIAS_SEL	MIC bias voltage selection 00 = 1.5 V 10 = 2.2 V 01 = 1.6 V 11 = 2.3 V	00
3	R/W	MIC_L_MUTE	Mute left MIC amplifier 0 = unmute 1 = mute	0
2:0	R/W	MIC_L_VOL	Gain of left MIC amplifier 000 = -6 dB 001 = 0 dB 010 = +6 dB 011 = +12 dB 100 = +18 dB 101/110/111 = +24 dB	000

Table 45: MIC_R 0x08

Bit	Mode	Symbol	Description	Reset
7	R/W	MIC_R_EN	Enable right MIC amplifier 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6:4	R	Reserved	Reserved	000
3	R/W	MIC_R_MUTE	Mute right MIC amplifier 0 = unmute 1 = mute	0
2:0	R/W	MIC_R_VOL	Gain of right MIC amplifier Setting option is the same as L-channel (0x7[2:0])	000

Table 46: AUX1_L 0x09

Bit	Mode	Symbol	Description	Reset
7	R/W	AUX1_L_EN	Enable left AUX1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R	Reserved	Reserved	0
5:0	R/W	AUX1_L_VOL	Gain of left AUX1 amplifier 000000 to 010000 (default) = mute 010001 = -54 dB 010010 = -52.5 dB 010011 = -51 dB … continuing in 1.5 dB steps through 110101 = 0 dB, to … 111111 = +15 dB	010000

Table 47: AUX1_R 0x0A

Bit	Mode	Symbol	Description	Reset
7	R/W	AUX1_R_EN	Enable right AUX1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R	Reserved	Reserved	0

Bit	Mode	Symbol	Description	Reset
5:0	R/W	AUX1_R_VOL	Gain of right AUX1 amplifier 000000 to 010000 (default) = mute 010001 = -54 dB 010010 = -52.5 dB 010011 = -51 dB … continuing in 1.5 dB steps through 110101 = 0 dB, to … 111111 = +15 dB	010000

Table 48: IN_GAIN 0x0C

Bit	Mode	Symbol	Description	Reset
7:4	R/W	INPGA_R_VOL	Gain of right input PGA 0000 = -4.5 dB 0001 = -3 dB 0010 = -1.5 dB 0011 = 0 dB 0100 = +1.5 dB 0101 = + 3 dB 0110 = +4.5 dB 0111 = + 6 dB 1000 = + 7.5 dB 1001 = + 9 dB 1010 = +10.5 dB 1011 = +12 dB 1100 = +13.5 dB 1101 = +15 dB 1110 = +16.5 dB 1111 = +18 dB *While ALC is active, the gain is controlled by ALC and this register setting is not effective.*	0000

Bit	Mode	Symbol	Description	Reset
3:0	R/W	INPGA_L_VOL	Gain of left input PGA 0000 = -4.5 dB 0001 = -3 dB 0010 = -1.5 dB 0011 = 0 dB 0100 = +1.5 dB 0101 = + 3 dB 0110 = +4.5 dB 0111 = + 6 dB 1000 = + 7.5 dB 1001 = + 9 dB 1010 = +10.5 dB 1011 = +12 dB 1100 = +13.5 dB 1101 = +15 dB 1110 = +16.5 dB 1111 = +18 dB *While ALC is active, the gain is controlled by ALC and this register setting is not effective.*	0000

Table 49: INMIX_L 0x0D

Bit	Mode	Symbol	Description	Reset
7	R/W	IN_L_EN	Enable left input PGA 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6:5	R	Reserved	Reserved	00
4	R/W	IN_L_OUTMIX_L	1 = Add OUTMIX_L into input mixer L	0
3	R/W	Reserved	Reserved	0
2	R/W	IN_L_A1_L	1 = Add AUX1_L into input mixer L	0
1	R/W	IN_L_MIC_R	1 = Add MIC_R into input mixer L	0
0	R/W	IN_L_MIC_L	1 = Add MIC_L into input mixer L	0

Table 50: INMIX_R 0x0E

Bit	Mode	Symbol	Description	Reset
7	R/W	IN_R_EN	Enable right input PGA 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R	Reserved	Reserved	0
5	R/W	IN_R_IN_L	1 = Add INPGA_L (stereo to mono)	0
4	R/W	IN_R_OUTMIX_R	1 = Add OUTMIX_R into input mixer R	0

Bit	Mode	Symbol	Description	Reset
3	R	Reserved	Reserved	0
2	R/W	IN_R_A1_R	1 = Add AUX1_R into input mixer R	0
1	R/W	IN_R_MIC_L	1 = Add MIC_L into input mixer R	0
0	R/W	IN_R_MIC_R	1 = Add MIC_R into input mixer R	0

Table 51: ADC_HPF 0x0F

Bit	Mode	Symbol	Description	Reset
7	R/W	ADC_VOICE_EN	ADC Voice Filter 0 = disable 1 = enable	0
6:4	R/W	ADC_VOICE_F0	ADC Voice (8 kHz) High pass 3 dB cut-off at: 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz	000
3	R/W	ADC_HPF_EN	ADC High Pass Filter 0 = disable 1 = enable	1
2	R	Reserved	Reserved	0
1:0	R/W	ADC_HPF_F0	ADC High Pass Filter f0 is at 00 = Fs/8192 x π 01 = Fs/4096 x π 10 = Fs/2048 x π 11 = Fs/1024 x π	00

Table 52: ADC 0x10

Bit	Mode	Symbol	Description	Reset
7	R/W	ADC_R_EN	Enable right ADC channel 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R/W	ADC_R_MUTE	Mute right ADC channel 0 = unmute 1 = mute	0
5:4	R	Reserved	Reserved	00
3	R/W	ADC_L_EN	Enable left ADC channel 0 = disable 1 = enable (must be set before SC_MST_EN)	0

Bit	Mode	Symbol	Description	Reset
2	R/W	ADC_L_MUTE	Mute left ADC channel 0 = unmute 1 = mute	0
1	R	Reserved	Reserved	0
0	RW	ALC_EN	ALC enable 0 = disable 1 = enable	0

Table 53: ADC_EQ1_2 0x11

Bit	Mode	Symbol	Description	Reset
7:4	R/W	ADC_EQ2_VOL	Gain of ADC 5-Band EQ band 2: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000
3:0	R/W	ADC_EQ1_VOL	Gain of ADC 5-Band EQ band 1: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000

Table 54: ADC_EQ3_4 0x12

Bit	Mode	Symbol	Description	Reset
7:4	R/W	ADC_EQ4_VOL	Gain of ADC 5-Band EQ band 4: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000
3:0	R/W	ADC_EQ3_VOL	Gain of ADC 5-Band EQ band 3: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000

Table 55: ADC_EQ5 0x13

Bit	Mode	Symbol	Description	Reset
7	R/W	ADC_EQ_EN	Enable ADC 5-Band EQ 0 = disable 1 = enable	0
6	R	Reserved	Reserved	0
5:4	R/W	ADC_EQ_GAIN	Gain of ADC 5-Band EQ: 00 = 0 dB 01 = -6 dB 10 = -12 dB 11 = -18 dB	00
3:0	R/W	ADC_EQ5_VOL	Gain of ADC 5-Band EQ band 5: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000

Table 56: DAC_HPF 0x14

Bit	Mode	Symbol	Description	Reset
7	R/W	DAC_VOICE_EN	DAC Voice Filter 0 = disable 1 = enable	0
6:4	R/W	DAC_VOICE_F0	DAC Voice (8 kHz) High pass 3 dB cut-off at: 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz For 11.025/12.0 and 16 kHz see Table 26	000
3	R/W	DAC_HPF_EN	DAC High Pass Filter 0 = disable 1 = enable	1
2	R/W	DAC_MUTE	Mute DAC (both channels)	0
1:0	R/W	DAC_HPF_F0	DAC High Pass Filter f0 is at 00 = Fs/8192 x π 01 = Fs/4096 x π 10 = Fs/2048 x π 11 = Fs/1024 x π	00

Table 57: DAC_L 0x15

Bit	Mode	Symbol	Description	Reset
7	R/W	DAC_L_INV	left DAC channel inversion 0 = normal 1 = Inverted	0
6:0	R/W	DAC_L_GAIN	DAC left channel digital volume control 0000000 = 12 db 0000001 = 11.25 dB … continuing in 0.75 dB steps through 0010000 = 0 dB 0010001 = -0.75 dB …to 1110111 = -77.25 dB 1111xxx = mute	0010000

Table 58: DAC_R 0x16

Bit	Mode	Symbol	Description	Reset
7	R/W	DAC_R_INV	0 = normal 1 = Invert right DAC channel	0
6:0	R/W	DAC_R_GAIN	DAC right channel digital volume control 0000000 = 12 db 0000001 = 11.25 dB … continuing in 0.75 dB steps through 0010000 = 0 dB 0010001 = -0.75 dB …to 1110111 = -77.25 dB 1111xxx = mute	0010000

Table 59: DAC_SEL 0x17

Bit	Mode	Symbol	Description	Reset
7	R/W	DAC_R_EN	Enable right DAC channel 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6:4	R/W	DAC_R_SRC	DAC_R input source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R	101
3	R/W	DAC_L_EN	Enable left DAC channel 0 = disable 1 = enable (must be set before SC_MST_EN)	0
2:0	R/W	DAC_L_SRC	DAC_L input source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R	100

Table 60: SOFTMUTE 0x18

Bit	Mode	Symbol	Description	Reset
7	R/W	SOFT_MUTE	Softmute trigger 0 = disabled 1 = start SOFTMUTE	0
6	R/W	RAMP_EN	Digital gain ramping 0 = disabled (immediate) 1 = enabled (ramping)	1
5:3	R	Reserved	Reserved	000
2:0	R/W	MUTE_RATE	000 = 1 sample/0.1875 dB 001 = 2 samples/0.1875 dB 010 = 4 samples/0.1875 dB 011 = 8 samples/0.1875 dB 100 = 16 samples/0.1875 dB 101 = 32 samples/0.1875 dB 110 = 64 samples/0.1875 dB 111 = not used	000

Table 61: DAC_EQ1_2 0x19

Bit	Mode	Symbol	Description	Reset
7:4	R/W	DAC_EQ2_VOL	Gain of DAC 5-Band EQ band 2: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000
3:0	R/W	DAC_EQ1_VOL	Gain of DAC 5-Band EQ band 1: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000

Table 62: DAC_EQ3_4 0x1A

Bit	Mode	Symbol	Description	Reset
7:4	R/W	DAC_EQ4_VOL	Gain of DAC 5-Band EQ band 4: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000
3:0	R/W	DAC_EQ3_VOL	Gain of DAC 5-Band EQ band 3: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000

Table 63: DAC_EQ5 0x1B

Bit	Mode	Symbol	Description	Reset
7	R/W	DAC_EQ_EN	Enable DAC 5-Band EQ 0 = disable 1 = enable	0
6:4	R	Reserved	Reserved	000
3:0	R/W	DAC_EQ5_VOL	Gain of DAC 5-Band EQ band 5: 0000 = +12 dB 0001 =+10.5 dB 0010 =+9 dB 0011 =+7.5 dB 0100 =+6 dB 0101 =+4.5 dB 0110 =+3 dB 0111 =+1.5 dB 1000= 0 dB 1001= - 1.5 dB 1010= - 3 dB 1011= - 4.5 dB 1100= - 6 dB 1101= - 7.5 dB 1110= - 9 dB 1111= -10.5 dB	0000

Table 64: OUTMIX_L 0x1C

Bit	Mode	Symbol	Description	Reset
7	R/W	OUT_L_EN	Enable left output PGA 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R/W	OUT_L_INV	OUTMIX left channel inversion 0 = normal 1 = Invert (not active for signal routed from DAC_L)	0
5	R	Reserved	Reserved	0
4	R/W	OUT_L_DAC_L	1 = Add DAC_L	0
3	R/W	OUT_L_IN_R	1 = Add IN_R	0
2	R/W	OUT_L_IN_L	1 = Add IN_L	0
1	R	Reserved	Reserved	0
0	R/W	OUT_L_A1_L	1 = Add AUX1_L	0

Table 65: OUTMIX_R 0x1D

Bit	Mode	Symbol	Description	Reset
7	R/W	OUT_R_EN	Enable right output PGA 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R/W	OUT_R_INV	OUTMIX right channel inversion 0 = normal 1 = Invert (not active for signal routed from DAC_L)	0
5	R	Reserved	Reserved	0
4	R/W	OUT_R_DAC_R	1 = Add DAC_R	0
3	R/W	OUT_R_IN_R	1 = Add IN_R	0
2	R/W	OUT_R_IN_L	1 = Add IN_L	0
1	R	Reserved	Reserved	0
0	R/W	OUT_R_A1_R	1 = Add AUX1_R	0

Table 66: OUT1_L 0x1E

Bit	Mode	Symbol	Description	Reset
7	R/W	OUT1_L_EN	Enable left OUT1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R/W	OUT1_L_SE	OUT1 L single-ended mode selection 0 = differential mode 1 = single-ended mode	0
5:0	R/W	OUT1_L_VOL	OUT1 left channel volume control 000000 – 001111 = Reserved 010000 = mute 010001 = -54 dB 010010 = -52.5 dB … continuing in 1.5 dB steps through 110101 = 0 dB (default) to… 111111 = 15 dB	110101

Table 67: OUT1_R 0x1F

Bit	Mode	Symbol	Description	Reset
7	R/W	OUT1_R_EN	Enable right OUT1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R/W	OUT1_R_SE	OUT1 R single-ended mode selection 0 = differential mode 1 = single-ended mode	0
5:0	R/W	OUT1_R_VOL	OUT1 right channel volume control 000000 – 001111 = Reserved 010000 = mute 010001 = -54 dB 010010 = -52.5 dB … continuing in 1.5 dB steps through 110101 = 0 dB (default) to… 111111 = 15 dB	110101

Table 68: HP_L_VOL 0x21

Bit	Mode	Symbol	Description	Reset
7:6	R	Reserved	Reserved	00
5:0	R/W	HP_L_VOL	Head phone left channel volume control 000000 – 001111 = Reserved 010000 = mute (default) 010001 = -54 dB 010010 = -52.5 dB … continuing in 1.5 dB steps through 110101 = 0 dB to… 111111 = 15 dB If you wish the right channel volume to be the same as left channel, please refer to 0x23 HP_CFG[5] STEREO_TRACK	010000

Table 69: HP_R_VOL 0x22

Bit	Mode	Symbol	Description	Reset
7:6	R	Reserved	Reserved	00
5:0	R/W	HP_R_VOL	Head phone right channel volume control 000000 – 001111 = Reserved 010000 = mute (default) 010001 = -54 dB 010010 = -52.5 dB … continuing in 1.5 dB steps through 110101 = 0 dB to… 111111 = 15 dB If you wish the right channel volume to be the same as left channel, please refer to 0x23 HP_CFG[5] STEREO_TRACK	010000

Table 70: HP_CFG 0x23

Bit	Mode	Symbol	Description	Reset
7	R/W	HP_R_EN	Enable right headphone amplifier 0 = disable 1 = enable (must be set before SC_MST_EN)	0
6	R/W	Reserved	Reserved	0
5	R/W	STEREO_TRACK	1 = HP_R volume also controls HP_L	0
4	R/W	HP_HIGHZ_R	Set right head phone out to high impedance	0
3	R/W	HP_L_EN	Enable left headphone amplifier 0 = disable 1 = enable (must be set before SC_MST_EN)	0
2	R/W	Reserved	Reserved	0
1	R/W	HP_2CAP_MODE	Set charge pump to 2 capacitor mode	1
0	R/W	HP_HIGHZ_L	Set left head phone out to high impedance	0

Table 71: ZEROX 0x24

Bit	Mode	Symbol	Description	Reset
7	R/W	HPZX_R_EN	Enable zero crossing for right HP gain update	0
6	R/W	HPZX_L_EN	Enable zero crossing for left HP gain update	0
5	R/W	OUTZX_R_EN	Enable zero crossing for right OUT1 gain update	0
4	R/W	OUTZX_L_EN	Enable zero crossing for left OUT1 gain update	0

Bit	Mode	Symbol	Description	Reset
3	R/W	INZX_R_EN	Enable zero crossing for right input PGA gain update	0
2	R/W	INZX_L_EN	Enable zero crossing for left input PGA gain update	0
1	R/W	AUX1ZX_R_EN	Enable zero crossing for right AUX1 amp gain update	0
0	R/W	AUX1ZX_L_EN	Enable zero crossing for left AUX1 amp gain update	0

Table 72: DAI_SRC_SEL 0x25

Bit	Mode	Symbol	Description	Reset
7	R/W	DAI_IN_R_MIX	1 = DAI receive right channel is mixed from L+R data	0
6:4	R/W	DAI_OUT_R_SRC	DAI_R transmit source selection: 000: = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L (cross loop back) 101 = DAI_R (loop back) 110 = ADC_L 111 = ADC_R	111
3	R/W	DAI_IN_L_MIX	1 = DAI receive left channel is mixed from L+R data	0
2:0	R/W	DAI_OUT_L_SRC	DAI_L transmit source selection: 000: = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L (cross loop back) 101 = DAI_R (loop back) 110 = ADC_L 111 = ADC_R	110

Table 73: DAI_CFG1 0x26

Bit	Mode	Symbol	Description	Reset
7	R/W	DAI_MODE	0 = DA7211 is clock slave 1 = DA7211 is clock master	0
6:5	R	Reserved	Reserved	00
4	R/W	DAI_TDM_MONO	0 = TDM mode is stereo 1 = TDM transmits/receives left channel left DAI channel only	0

Bit	Mode	Symbol	Description	Reset
3:2	R/W	DAI_FRAME	Data transmission frame length: 00 = 2xDAI_WORD 01 = 64 bitclocks 10 = 128 bitclocks 11 = 256 bitclocks	00
1:0	R/W	DAI_WORD	Data word length: 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits	00

Table 74: DAI_CFG2 0x27

Bit	Mode	Symbol	Description	Reset
7:0	R/W	DAI_TDM_OFFS	TDM data for device is valid at this offset from beginning of frame. The offset is measured in the number clock cycles.	00000000

Table 75: DAI_CFG3 0x28

Bit	Mode	Symbol	Description	Reset
7	R/W	DAI_EN	Enable digital audio interface 0 = disable 1 = enable	0
6:4	R	Reserved	Reserved	00
3	R/W	DAI_OE	DATOUT enable: 0 = disable (tristate when ADC is disabled) 1 = enabled	0
2	R/W	DAI_TDM	Tristate DATOUT mode enable 0 = disable (normal) 1 = enable (TDM mode)	0
1:0	R/W	DAI_FORMAT	Digital Audio Interface format selection 00 = I2S mode 01 = Left Justified mode 10 = right justified mode 11 = DSP mode	00

Table 76: PLL_DIV1 0x29

Bit	Mode	Symbol	Description	Reset
7:0	R/W	PLL_DIV_H	Feedback divider ratio bit [19:12]. Refer to Table 31 and Table 32 for suggested settings.	00000000

Table 77: PLL_DIV2 0x2A

Bit	Mode	Symbol	Description	Reset
7:0	R/W	PLL_DIV_M	Feedback divider ratio bit [11:4]. Refer to Table 31 and Table 32 for suggested settings.	00000000

Table 78: PLL_DIV3 0x2B

Bit	Mode	Symbol	Description	Reset
7	R	Reserved	Reserved	0
6	R/W	PLL_BYP	Bypass PLL 0 = disable (do not disable unless PLL is operational) 1 = enable (PLL bypassed)	0
5:4	R/W	MCLK_RANGE	MCLK frequency range: 00 = 32.768 kHz 01 = 10-20 MHz 10 = 20-40 MHz 11 = 40-80 MHz	01
3:0	R/W	PLL_DIV_L	Feedback divider ratio bit [3:0]. Refer to Table 31 and Table 32 for suggested settings.	0000

Table 79: PLL 0x2C

Bit	Mode	Symbol	Description	Reset
7	R/W	PLL_EN	PLL enable 0 = disable and bypass PLL 1 = enable PLL	0
6	R/W	MCLK_SRM_EN	Sample rate tracking 0 = disabled 1 = enabled	0
5	R/W	MCLK_DET_EN	automatic detection of sample rate 0 = disabled 1 = enabled	0
4	R/W	MCLK_SHAPE_EN	Enable MCLK shaper for low level non TTL signals 0 = disabled 1 = enabled	0

Bit	Mode	Symbol	Description	Reset
3:0	R/W	FS	In MCLK_DET mode, the value read from this register will be the automatically detected sample rate from the PLL track circuitry. This will be updated on the positive edge of the DAI clock. 0000 = reserved 0001 = 8 kHz 0010 = 11.025 kHz 0011 = 12 kHz 0100 = reserved 0101 = 16 kHz 0110 = 22.05 kHz 0111 = 24 kHz 1000= reserved 1001 = 32 kHz 1010 = 44.1 kHz 1011 = 48 kHz 1100 = reserved 1101 = reserved 1110 = 88.2 kHz 1111 = 96 kHz	1010

10.4 GP Filter Engine

Table 80: GP1A A0L 0x2D

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 81: GP1A A0H 0x2E

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 82: GP1B A0L 0x2F

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 83: GP1B A0H 0x30

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 84: GP2A A0L 0x31

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 85: GP2A A0H 0x32

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 86: GP2B_A0L 0x33

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 87: GP2B_A0H 0x34

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 88: GP1C_A0L 0x35

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 89: GP1C_A0H 0x36

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 90: GP1D_A0L 0x37

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 91: GP1D_A0H 0x38

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 92: GP2C_A0L 0x39

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 93: GP2C_A0H 0x3A

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 94: GP2D_A0L 0x3B

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_A0L	A0L bit 7:0 of A0 coefficient	00000000

Table 95: GP2D_A0H 0x3C

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_A0H	A0H bit 15:8 of A0 coefficient	01000000

Table 96: GP1A_A1L 0x3D

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 97: GP1A_A1L 0x3E

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_A1L	A1H bit 15:8 of A1 coefficient	00000000

Table 98: GP1B_A1L 0x3F

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 99: GP1B_A1H 0x40

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_A1H	A1H bit 15:8 of A1 coefficient	00000000

Table 100: GP2A_A1L 0x41

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 101: GP2A_A1H 0x42

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_A1H	A1H bit 15:8 of A1 coefficient	00000000

Table 102: GP2B_A1L 0x43

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 103: GP2B_A1H 0x44

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_A1H	A1H bit 15:8 of A1 coefficient	00000000

Table 104: GP1C_A1L 0x45

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 105: GP1C_A1H 0x46

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_A1H	A1H bit 15:8 of A1 coefficient	00000000

Table 106: GP1D_A1L 0x47

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 107: GP1D_A1H 0x48

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_A1H	A1H bit 15:8 of A1 coefficient	00000000

Table 108: GP2C_A1L 0x49

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 109: GP2C_A1H 0x4A

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_A1H	A1H bit 15:8 of A1 coefficient	00000000

Table 110: GP2D_A1L 0x4B

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_A1L	A1L bit 7:0 of A1 coefficient	00000000

Table 111: GP2D_A1H 0x4C

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_A1H	A1H bit 15:8 of A1 coefficient	00000000

Table 112: GP1A_A2L 0x4D

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 113: GP1A_A2H 0x4E

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 114: GP1B_A2L 0x4F

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 115: GP1B_A2H 0x50

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 116: GP2A_A2L 0x51

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 117: GP2A_A2H 0x52

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 118: GP2B_A2L 0x53

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 119: GP2B_A2H 0x54

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 120: GP1C_A2L 0x55

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 121: GP1C_A2H 0x56

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 122: GP1D_A2L 0x57

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 123: GP1D_A2H 0x58

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 124: GP2C_A2L 0x59

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 125: GP2C_A2H 0x5A

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 126: GP2D_A2L 0x5B

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_A2L	A2L bit 7:0 of A2 coefficient	00000000

Table 127: GP2D_A2H 0x5C

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_A2H	A2H bit 15:8 of A2 coefficient	00000000

Table 128: GP1A_B1L 0x5D

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 129: GP1A_B1H 0x5E

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 130: GP1B_B1L 0x5F

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 131: GP1B_B1H 0x60

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 132: GP2A_B1L 0x61

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 133: GP2A_B1H 0x62

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 134: GP2B_B1L 0x63

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 135: GP2B_B1H 0x64

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 136: GP1C_B1L 0x65

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 137: GP1C_B1H 0x66

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 138: GP1D_B1L 0x67

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 139: GP1D_B1H 0x68

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 140: GP2C_B1L 0x69

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 141: GP2C_B1H 0x6A

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 142: GP2D_B1L 0x6B

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_B1L	B1L bit 7:0 of B1 coefficient	00000000

Table 143: GP2D_B1H 0x6C

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_B1H	B1H bit 15:8 of B1 coefficient	00000000

Table 144: GP1A_B2L 0x6D

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 145: GP1A_B2H 0x6E

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1A_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 146: GP1B_B2L 0x6F

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 147: GP1B_B2H 0x70

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1B_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 148: GP2A_B2L 0x71

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 149: GP2A_B2H 0x72

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2A_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 150: GP2B_B2L 0x73

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 151: GP2B_B2H 0x74

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2B_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 152: GP1C_B2L 0x75

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 153: GP1C_B2H 0x76

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1C_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 154: GP1D_B2L 0x77

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 155: GP1D_B2H 0x78

Bit	Mode	Symbol	Description	Reset
7:0	W	GP1D_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 156: GP2C_B2L 0x79

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 157: GP2C_B2H 0x7A

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2C_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 158: GP2D_B2L 0x7B

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_B2L	B2L bit 7:0 of B2 coefficient	00000000

Table 159: GP2D_B2H 0x7C

Bit	Mode	Symbol	Description	Reset
7:0	W	GP2D_B2H	B2H bit 15:8 of B2 coefficient	00000000

Table 160: GPF_SRC1 0x7D

Bit	Mode	Symbol	Description	Reset
7	R	Reserved	Reserved	0
6:4	R/W	GP_2AB_SRC	GP Filter 2AB source selection: 000 = 1AB 001 = reserved 010 = 1CD 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R	110
3	R	Reserved	Reserved	0

Bit	Mode	Symbol	Description	Reset
2:0	R/W	GP_1AB_SRC	GP Filter 1AB source selection: 000 = reserved 001 = reserved 010 = reserved 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R	100

Table 161: GPF_SRC2 0x7E

Bit	Mode	Symbol	Description	Reset
7	R	Reserved	Reserved	0
6:4	R/W	GP_2CD_SRC	GP Filter 2CD source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R	111
3	R	Reserved	Reserved	0
2:0	R/W	GP_1CD_SRC	GP Filter 1CD source selection: 000 = 1AB 001 = reserved 010 = reserved 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R	101

Table 162: DSP_CFG 0x7F

Bit	Mode	Symbol	Description	Reset
7	R	Reserved	Reserved	0
6	R/W	DSP_MIX_3	1 = Output of section 2AB is mixed with 2CD	0
5	R/W	DSP_MIX_2	1 = Output of section 1CD is mixed with 2AB	0
4	R/W	DSP_MIX_1	1 = Output of section 1AB is mixed with 1CD	0

Bit	Mode	Symbol	Description	Reset
3	R/W	GP2CD_EN	Enable GP section 2CD 0 = disable 1 = enable	0
2	R/W	GP1CD_EN	Enable GP section 1CD 0 = disable 1 = enable	0
1	R/W	GP2AB_EN	Enable GP section 2AB 0 = disable 1 = enable	0
0	R/W	GP1AB_EN	Enable GP section 1AB 0 = disable 1 = enable	0

Table 163: CHIP_ID 0x81

Bit	Mode	Symbol	Description	Reset
7:4	R	MRC	Read back of mask revision code (MRC) – code 0 for AA release	0001
3:0	R	MMRC	Read back of metal mask release code (MMRC) – starts with a code 0	0001

Table 164: INTERFACE 0x82

Bit	Mode	Symbol	Description	Reset
7:5	R	IF_BASE_ADDR	3 MSB of 2-wire control interface base address XXX1010 + R/W 00110100 = 0x34 (write address) 00110101 = 0x35 (read address)	001
4:0	R	Reserved	Reserved	00000

10.5 ALC Level Controls

Table 165: ALC_MAX 0x83

Bit	Mode	Symbol	Description	Reset
7	R	Reserved	Reserved	0
6	R/W	ALC_MERGE	ALC joined stereo mode 0 = disabled (channels updates independently) 1 = enabled (channels update synchronously)	1
5:0	R/W	ALC_MAX	ALC max control level (refer to Table 20) maximum value of ALC_MAX = 3Ch = -0.5 dB	000000

Table 166: ALC_MIN 0x84

Bit	Mode	Symbol	Description	Reset
7:6	R	Reserved	Reserved	00
5:0	R/W	ALC_MIN	ALC min control level: (refer to Table 20) maximum value of ALC_MIN = 3Bh = -2 dB	000000

Table 167: ALC_NOIS 0x85

Bit	Mode	Symbol	Description	Reset
7:6	R	Reserved	Reserved	00
5:0	R/W	ALC_NOIS	ALC noise gate level: (refer to Table 20) Note that the minimum value of ALC_NOIS is 86 dB	000000

Table 168: ALC_ATT 0x86

Bit	Mode	Symbol	Description	Reset
7:0	R/W	ALC_ATT	ALC attack rate: Number of sample periods between two gain steps of 0.25 dB 00000000 = 0.25 dB/sample period	00000000

Table 169: ALC_REL 0x87

Bit	Mode	Symbol	Description	Reset
7:0	R/W	ALC_REL	ALC release rate: Number of periods between two gain steps of 0.25 dB in increments of 4 sample periods 00000000 = 0.0625 dB/sample period	00000000

Table 170: ALC_DEL 0x88

Bit	Mode	Symbol	Description	Reset
7:0	R/W	ALC_DEL	ALC release delay: Time delay before ALC release starts in increments of ALC_REL periods	00000000

Table 171: A_HID_UNLOCK 0x8A

Bit	Mode	Symbol	Description	Reset
7:0	W	A_HID_UNLOCK	Register unlock: Set to 0x8B (10001011) to use the registers below	00000000

Table 172: A_TST_UNLOCK 0x8B

Bit	Mode	Symbol	Description	Reset
7:0	W	A_TST_UNLOCK	Register unlock: Set to 0xB4 (10110100) to use the registers below	00000000

Table 173: A_PLL0 0x8F

Unlocking registers 0x8A and 0x8B is required to access this register

Bit	Mode	Symbol	Description	Reset
0	W	SIGDEL_DISABLE	Disable sigma delta modulator in the analogue PLL. If = 1, reduces current when using internal oscillator. Must be enabled when using PLL	0
7:6	W	Reserved	Reserved	0000000

Table 174: A_PLL1 0x90

Unlocking registers 0x8A and 0x8B is required to access this register

Bit	Mode	Symbol	Description	Reset
7:1	W	Reserved	Reserved	0000000
0	W	VCORST_EN	Separate power-down signal for the VCO reset controller 0 = disabled 1 = enabled for all PLL operations	1

Table 175: A_ADC0 0x95

Unlocking registers 0x8A and 0x8B is required to access this register

Bit	Mode	Symbol	Description	Reset
7:4	W	Reserved	Reserved	0000
3	W	ADC_T2	ADC bias current increase: 0 = default current 1 = increased current; improved THD performance	0
2:0	W	Reserved	Reserved	000

Table 176: A_DAC0 0x96

Unlocking registers 0x8A and 0x8B is required to access this register

Bit	Mode	Symbol	Description	Reset
7:3	W	Reserved	Reserved	00000
2:0	W	VMID_BUFF_EN	VMID buffer disable during ADC and analogue only modes to save power 000 = VMID buffer disabled **111 = VMID buffer enabled**	111

Table 177: A_CPHP6 0xA2

Unlocking registers 0x8A and 0x8B is required to access this register

Bit	Mode	Symbol	Description	Reset
7:0	W	CP_RISE_TIME	Set 0x80 (10000000) for maximum output power. Set 0x84 (10000100) for reduced inrush current	10000000

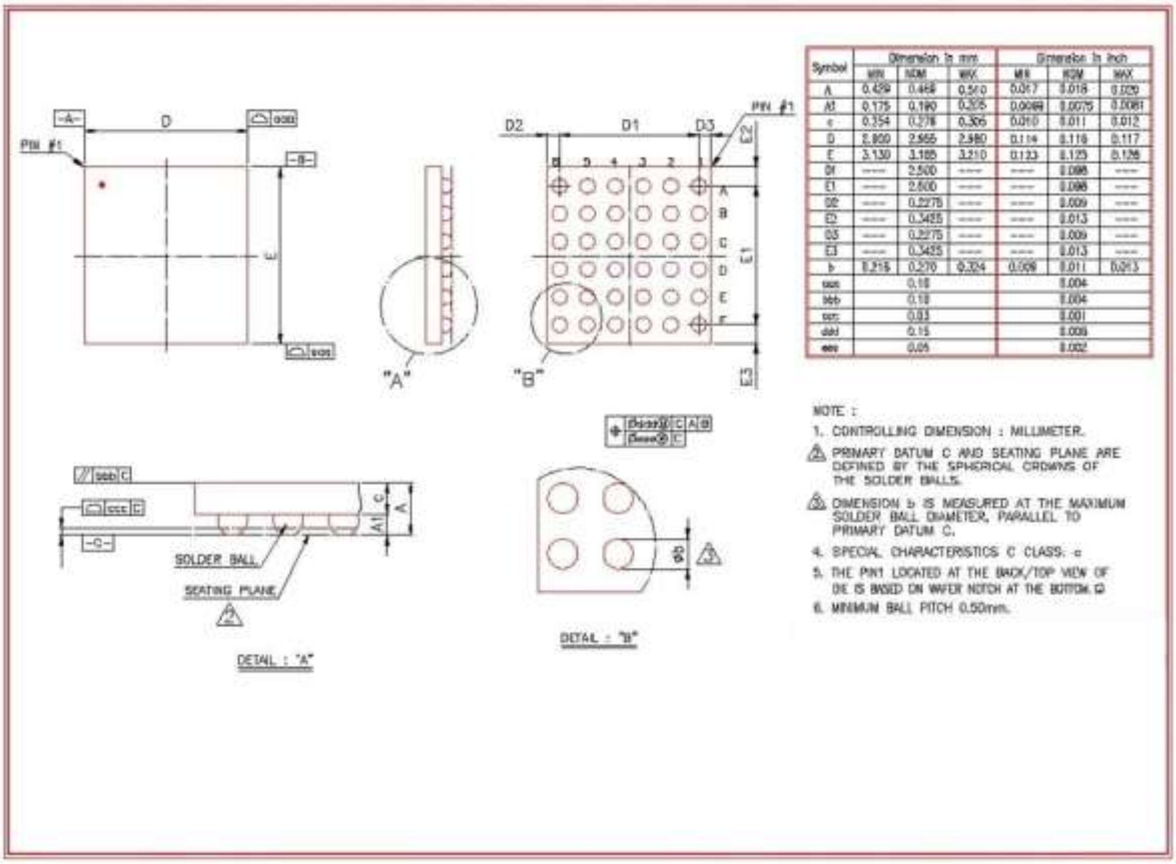
Table 178: A_CP_MODE 0xA7

Unlocking registers 0x8A and 0x8B is required to access this register

Bit	Mode	Symbol	Description	Reset
7:0	W	A_CP_MODE	Headphone charge pump enable: Set 0x7C (01111110)	01111110

11 Package Information

11.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.429	0.469	0.510	0.017	0.018	0.020
A1	0.175	0.190	0.205	0.0069	0.0075	0.0081
c	0.254	0.278	0.306	0.010	0.011	0.012
D	2.930	2.955	2.980	0.114	0.116	0.117
E	3.130	3.185	3.210	0.123	0.125	0.126
D1	----	2.500	----	----	0.098	----
E1	----	2.500	----	----	0.098	----
D2	----	0.2275	----	----	0.009	----
E2	----	0.3425	----	----	0.013	----
D3	----	0.2275	----	----	0.009	----
E3	----	0.3425	----	----	0.013	----
b	0.216	0.270	0.324	0.009	0.011	0.013
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.15			0.006		
eee	0.05			0.002		

Figure 49: 36 Bump WL-CSP 0.5 mm Pitch Package Outline Drawing

11.2 Soldering Information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

12 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please contact Renesas' local sales representative.

Table 179: Ordering Information

Part number	Package	Size (mm)	Shipment form	Pack quantity
DA7211-01UA2	36-bump CSP Pb-free/green		Tape and Reel	2,000 pcs.
DA7211-01UA6	36-bump CSP Pb-free/green		Waffle Pack (engineering samples only - not for mass production)	900 pcs.

13 Applications Information

13.1 Supporting Information

The bass response of the analogue inputs and outputs is determined by the output coupling capacitor and associated resistive load. If smaller footprint, low value capacitors are preferred, then the low frequency cut-off will be increased.

To maintain maximum audio bandwidth, larger capacitors are recommended, taking into account the relationship

$$\text{Low frequency cut-off} = \frac{1}{2\pi RC}$$

The analogue outputs can support between 32 Ω (16 Ω for headphone outputs) and line level loads (e.g. >=10 kΩ), so the range of capacitor values is wider, and care is required when making the selection.

13.2 Minimum Component Recommendations

To ensure datasheet performance is maintained it is recommended that the following minimum component criteria are met. Figure 49 shows recommended components and input/output configurations.

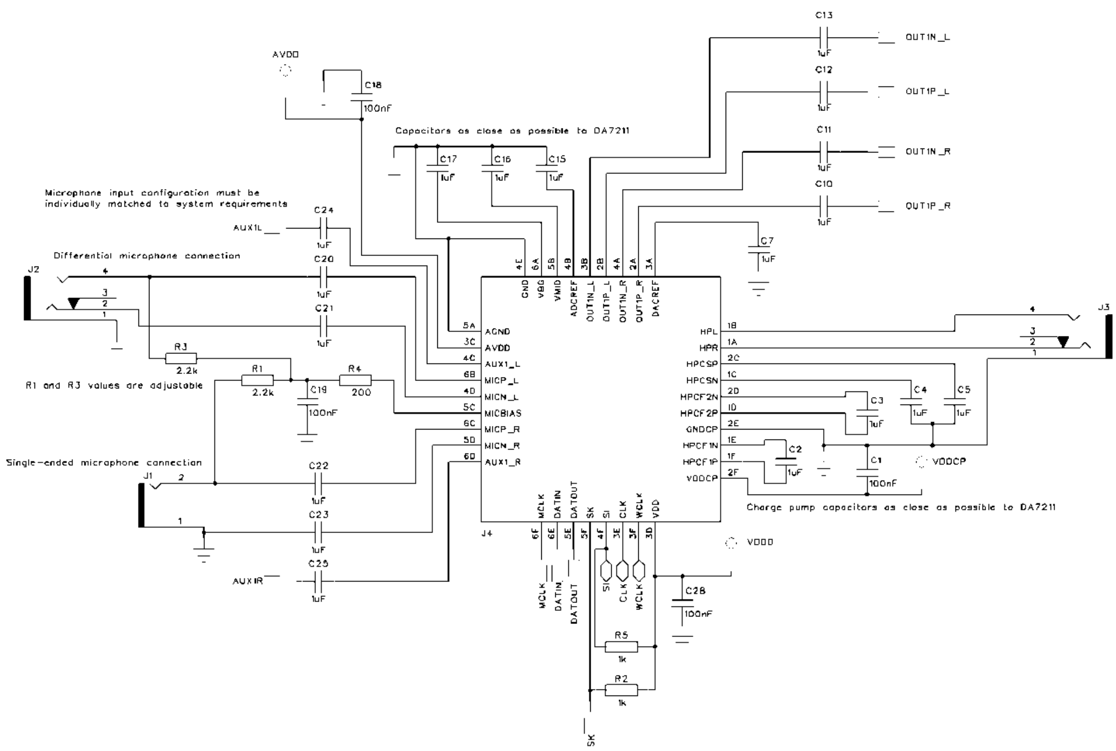


Figure 49: DA7211 36-Pin CSP Component Recommendations

- It is recommended that ceramic capacitors are used where possible for low ESR.

- It is recommended that C0G or X7R dielectric is used where possible to minimise distortion.
- The voltage rating of any capacitor used should be much greater than the maximum peak signal amplitude expected. It has been shown that capacitors with a large voltage rating introduce less distortion into the signal paths.
- For example the voltage rating of the 1 µF capacitors in the output paths should be chosen as 16 V
- All capacitors >=10 µF should use minimum dielectric specification X5R where possible.
- All 100 nF power supply decoupling capacitors should be placed as close as possible to associated pins. Reference: C1, C18 and C28.
- All 1 µF voltage reference capacitors should be placed as close as possible to associated pins. Reference: C7, C15-17.
- The headphone output amplifier is driven by a PWM based charge pump. To maintain efficiency the 1 µF charge pump capacitors should be placed as close as possible to associated pins. Reference: C2-C5.
- The control interface data I/O pin, SI, is open drain and therefore requires an external pull-up. If the control interface data output of the system processor does not support an internal pull-up, then an external resistor R2 is required.

13.3 General Component Suggestions

The following components and input/output configurations are suggested below.

- Headphone output and microphone input connectors shown in Figure 49 are of the 3.5 mm RCA/phono type, but any other suitable connector is acceptable.
- J1 is configured as a mono microphone input. The ground reference connection MICN_R, pin 5D, is internally referenced to a voltage 0.45*AVDD and therefore must be connected to AGND (or ground plane if connected to AGND) through C23. Similarly MICP_R, pin 6C, should be connected to the signal input via C22.
- MICBIAS, pin 5C, can supply up to 2 mA of current for biasing electret microphones. The MICBIAS pin must be separated from the mic input by ≈200 Ω resistor.
- A capacitive load of 100 nF is also required for output stability and doubles as a decoupling capacitor.
- If two microphones are supplied by this pin, then separate RC circuits are implemented for each microphone to provide isolation between inputs, as shown in Figure 49.
- J2 is configured as a differential microphone input. The positive signal input is connected to MICP_L, pin 6B, the inputs pins are internally referenced to voltage 0.45*AVDD and therefore must be connected through C20. Similarly, the negative signal input is connected to MICN_L, pin 4D, through C21. To maintain balance the value of R4 should match that of R3.
- When the line outputs are used to drive a differential load of 32 Ω, coupling caps are not required
- If the analogue outputs, excluding the headphone outputs, are used with line level loads (e.g. ≈10 kΩ) and minimum bass response of the outputs is not deemed important, it could be acceptable to reduce the coupling capacitors for OUT1L/R analogue output pins to less than 1 µF. An absolute minimum value of 100 nF is recommended. Reference: C10-13.
- It is unlikely that the bass response of the microphone used will be much lower than 100 Hz. The microphone inputs have an impedance ≈15 kΩ, it could therefore be acceptable to use coupling capacitors less than 1 µF without significantly affecting the input signal bandwidth. An absolute minimum value of 100 nF is recommended.
- The input impedance of the analogue inputs is ≈30 kΩ. If minimum bass response of the analogue inputs is not deemed important, the input coupling capacitors for MICL/R and AUX1L/R

can be reduced to less than 1 µF. An absolute minimum value of 100 nF is recommended. Reference: C21-27.

Revision History

Revision	Date	Description
3.3	09-Jun-2023	Updated tables: Master mode PLL-DIV look up, DAI_CFG3 0x28, CONTROL 0x01, ADC_EQ5 0x13. Editorial.
3.2	23-Dec-2021	Updated logo, disclaimer, copyright.
3.1	01-Feb-2019	Removed security status
DA7211-01 IDS3e-151015	Oct 2015	Deleted 10 year guarantee note under 'Recommended operating conditions' table. Corrections to table 10 for DAC from pasting errors Corrections to tables 51 and 56. [000 = 2.5 Hz and not 12.5 Hz] Update of block diagram to reference DA7202 device Formatting corrections. Update to ordering information to include 'engineering samples only - not for mass production' for waffle pack option.
DA7211-01 IDS3d_150724	July 2015	Update to latest template with formatting changes DA7211-01 changed to DA7211 everywhere except header and ordering information Changed page references to table references Added blue cross reference format to cross references Removed reserved registry tables and references in registry map In table 0x1B changed title from DAC_EQ_GAIN to DAC_EQ5 Removed remaining referenced to AUX2 and OUT2
DA7211-IDS2e-310310	March/April 2010	Pg 5 AVDD description is chagend to analogue supply & input to the onchip regulator (used to be only analogue) VDDD description is changed to Digital IO supply from Digital Supply. Pg 7 same thing applies to AVDD/VDDD Pg 56 0x01 control register Bit 0 : REG_EN is set to always 1 and 0 is not recommended. Bit 7 : there are two of this and deleted the one at the bottom. Pg 57: added warning regarding reserved reg/bits added notes to reg 0x05 Pg 62 0x1A : corrected to MSB first Pg 63 0x1D bit 2, simple eratta, some of them remained as L, and should be corrected as R Pg 65 0x24 zero cross : clarified A1 amp to AUX1 Pg 69 added DSP mix result table Pg 72 Reg0xB0-B2 : corrected to the MSB first corrected typo: second 0xB0 to be B2. Overall adjusted the layout N/A to be "reserved" and added the description to reserved bits.

Revision	Date	Description
DA7211-IDS2d-080210	Feb 2010	Page7:Removed references to VDDDAC/VDDADC/VDDIO in CSP36 (in both tables) Page10: Removed reference to VDDDAC Page13: Removed reference to nCS/SO. Page50: Removed reference to 4-wire references Page55: VDDDIO_RANGE Page56: Removed reference to OUT2 and AUX2 Page 25: Removed reference to ATB0_HPS Page 56: Updated Startup3 register
DA7211-IDS2d-230210	Feb 2010	Updated the numbering for footnotes pg 79 Updated the ordering information pg 57 Updated the STARTUP3 register pg 76 Renamed register 0xA7 to A_CP_MODE
DA7211-IDS2b-291009	Oct 2009	Pg 41-42 rewrote clocking scheme sections, added 32 Khz description Pg 44 updated figure 36 Pg 7 changed VDD min to 1.2 V Pg 8,9 updated ADC power and SNR/THD Pg 43 updated footnotes Pg 50-75 updated register descriptions
DA7211-IDS2a-090914	Sep 2009	Data Sheet Status Definition added P78
DA7211-IDS-Rev1_51-090817	Aug 2009	Changes to PLL range in register 0x2B Pg 8 PD descriptions Updated ordering information
DA7211-IDS-Rev1_52-090820	Aug 2009	Updated PLL block diagram Updated PLL-DIV look up table settings removed DAC EQ settings
DA7211-IDS-Rev1_53-090828	Aug 2009	Pg 1,10,19 Updated power number to 2.5 mW Pg 5updated CSP packaging drawing Pg 2 updated block diagram Pg 5 updated pin descriptions Pg 14 updated THD+N for HP Pg 26 updated Figure 10 Pg 35 updated para 1 Pg 50,60 updated register map and descriptions for GPO
DA7211-IDS-Rev1_54-090828	Aug 2009	Pg 24 figure 10 updated Updated descriptions for GPO and HPS P52 updated label and pin descriptions P 7 Updated ATB1_HPS for HPS and updated pin description
DA7211-IDS-Rev1_55-090828	Aug 2009	P 74 Changes made to 0x17D GPF_SRC1 description P 74 Changes made to 0x7E GPF_SRC2

Revision	Date	Description
ULTRA-LOW POWER STEREO CODEC-1DS01-160709	July 2009	Initial draft release based on DA7211 IDS rev 1.5
DA7211-IDS-Rev1_5-090722	July 2009	Changes to based on DS Rev 1.5 Updated register map
DA7211-IDS2c-301209	Jan 2009	Pg 20 Updated ALC gain step size Pg 21 Add Softmute section Pg 41- 49 Added programming sections for Slave and master modes Pg 76 added ALC registers
DA7211-01 IDS2f_100615.docx	June 2010	Changed Input Frequency to 11.289 page 13, Phase Lock loop table
DA7211-01 IDS3a_100921.docx	Sept 2010	Changed headline power number to 72 mW, (P1, 1st paragraph). Key features: 2x72 mW Output power Added a line in headphone amplifier table, (P11) “Output power per channel (VDDCP=2.5 V, THD<1%, RL=16 R, 1 kHz) Typ = 72 mW” **Updated diagram for P.24** **P.25 – register addresses, added** Table relates to registers below- HP_L: 0x21[5:0] HP_R: 0x22[5:0] Out1_L: 0x1e[5:0] Out1_R: 0x1f[5:0] **Figure 32 – updated** **Updated paragraph on I2C address, (P.53 – Replace 1st paragraph)** **Update register maps** **P.79 – updated diagram**

Revision	Date	Description
DA7211-01 IDS3b_120926	Sept 2012	Many changes to general descriptive text throughout the entire document to improve clarity/legibility etc. The changes included correcting incorrect cross-references and removing many strange and illegible (font size = 1 point) text-strings from register and bitfield names. Many default values for registers and bitfields were also corrected.
DA7211-01 IDS3c_141223	Dec 2014	Updates made to the register map description defaults to ensure that they match the silicon. I2S timing diagram updated to correct timing error in previous versions (now matches DA7212) General formatting updates made

Status definitions

Revision	Datasheet status	Product status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS compliance

Renesas complies to European Directive 2001/95/EC and from 2 January 2013 onwards to European Directive 2011/65/EU concerning Restriction of Hazardous Substances (RoHS/RoHS2).
Renesas' statement on RoHS can be found on the customer portal https://support.diasemi.com/. RoHS certificates from our suppliers are available on request.

Important Notice and Disclaimer

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

https://www.renesas.com/contact/

Trademarks