

August 1991

Features

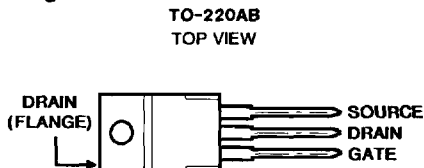
- 16A and 18A, 150V - 200V
- $r_{DS(on)} = 0.18\Omega$ and 0.22Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRF640, IRF641, IRF642, and IRF643 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRF640R, IRF641R, IRF642R and IRF643R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

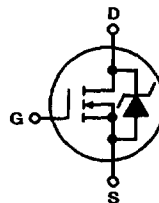
The IRF types are supplied in the JEDEC TO-220AB plastic package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRF640 IRF640R	IRF641 IRF641R	IRF642 IRF642R	IRF643 IRF643R	UNITS
Drain-Source Voltage (1)	V_{DS} 200	150	200	150	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} 200	150	200	150	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	I_D 18	18	16	16	A
$T_C = +100^\circ\text{C}$	I_D 11	11	10	10	A
Pulsed Drain Current (3)	I_{DM} 72	72	64	64	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$	P_D 125	125	125	125	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM} 72	72	64	64	A
(See Figure 14, $L = 100\mu\text{H}$)					
Single Pulse Avalanche Energy Rating (4)	E_{AS}^* 580	580	580	580	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
 - Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
 - Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
 - $V_{DD} = 50\text{V}$, starting $T_J = +25^\circ\text{C}$, $L = 2.7\text{mH}$, $R_{GS} = 25\Omega$, $I_{PEAK} = 18\text{A}$. See Figure 15.
- *R Suffix Types Only

IRF640, IRF641, IRF642, IRF643 IRF640R, IRF641R, IRF642R, IRF643R

Electrical Characteristics $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF640/642, IRF640R/642R IRF641/643, IRF641R/643R	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	200	-	-	V
			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$	-	-	250	μA
		$V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V, T_J = +125^\circ\text{C}$	-	-	1000	μA
On-State Drain Current (Note 2) IRF640/641, IRF640R/641R IRF642/643, IRF642R/643R	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max. } V_{GS} = 10V$	18	-	-	A
			16	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF640/641, IRF640R/641R IRF642/643, IRF642R/643R	$r_{DS(ON)}$	$V_{GS} = 10V, I_D = 10A$	-	0.14	0.18	Ω
			-	0.20	0.22	Ω
			-	-	-	-
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V, I_D = 10A$	6.7	10	-	S(Ω)
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$	-	1275	-	pF
Output Capacitance	C_{OSS}	See Figure 10	-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 100V, I_D = 18A, R_G = 9.1\Omega$	-	13	21	ns
Rise Time	t_r	See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	50	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	46	68	ns
Fall Time	t_f		-	35	54	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8V \text{ Max Rating. See Figure 17 for test circuit.}$	-	43	64	nC
Gate-Source Charge	Q_{gs}	(Gate charge is essentially independent of operating temperature.)	-	8	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	22	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on the tab to center of die	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25in.) from package to center of die	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.0	$^\circ\text{C/W}$
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.5	-	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	80	$^\circ\text{C/W}$

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	18	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	72	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$	-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = +25^\circ\text{C}, I_F = 18A, di_F/dt = 100A/\mu s$	120	240	530	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +150^\circ\text{C}, I_F = 18A, di_F/dt = 100A/\mu s$	1.3	2.8	5.6	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES: 1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
 2. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

4. $V_{DD} = 20V$, Start $T_J = +25^\circ\text{C}$, $L = 3.37\text{mH}$, $R_{GS} = 25\Omega$, $I_{PEAK} = 18A$ (See Figure 15)

4
N-CHANNEL
POWER MOSFETS

Performance Curves

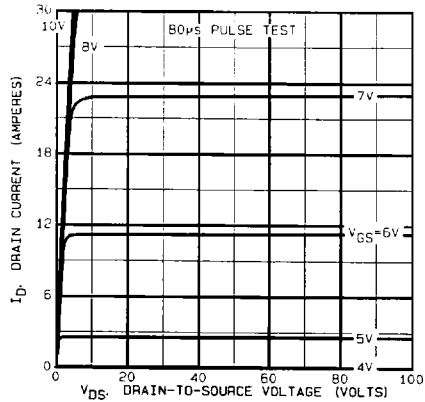


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

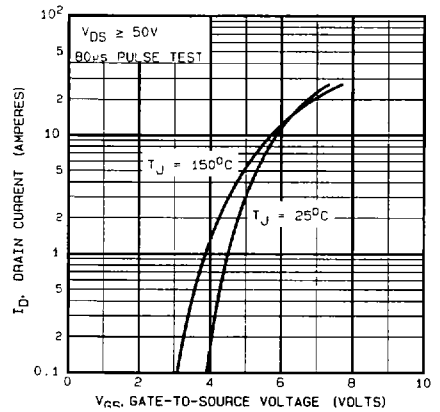


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

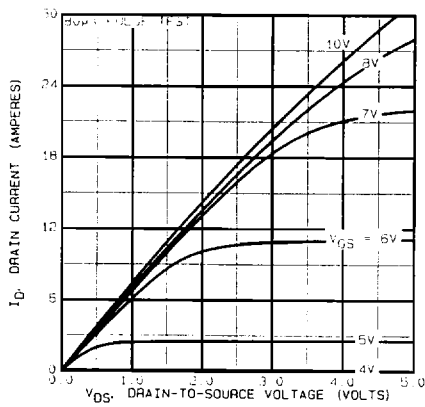


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

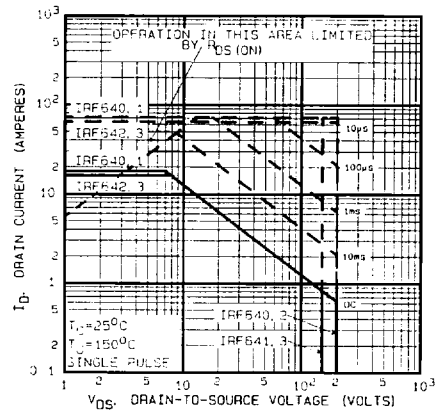


FIGURE 4. MAXIMUM SAFE OPERATING AREA

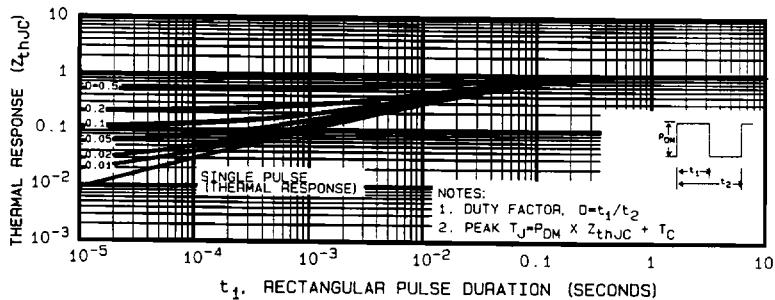


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

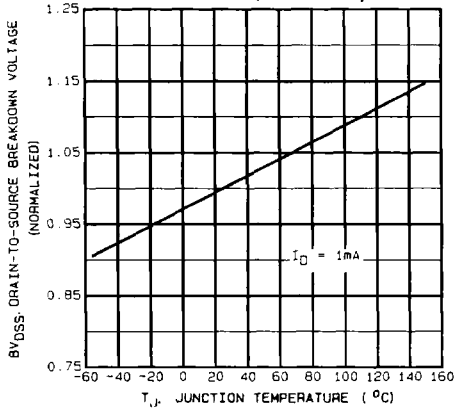


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

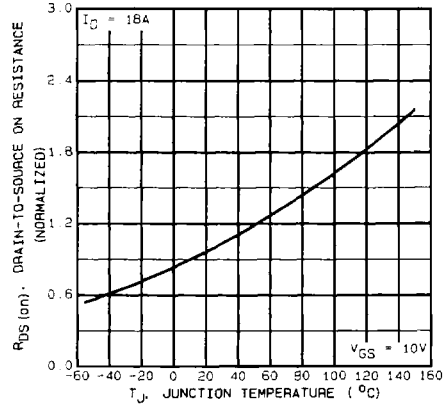


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

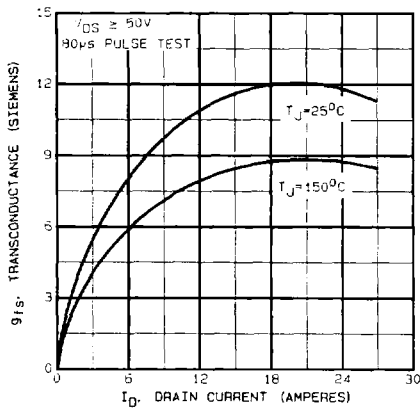


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

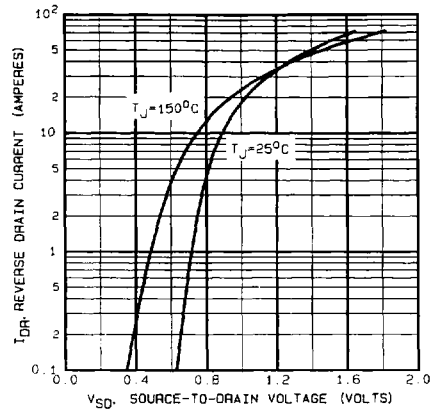


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

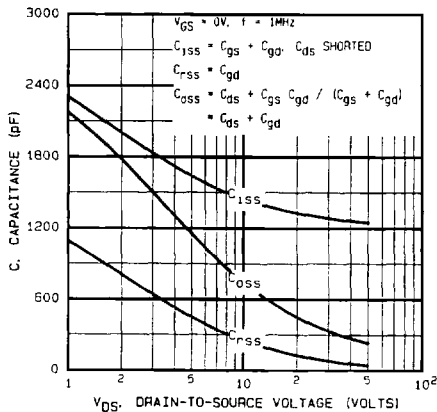


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

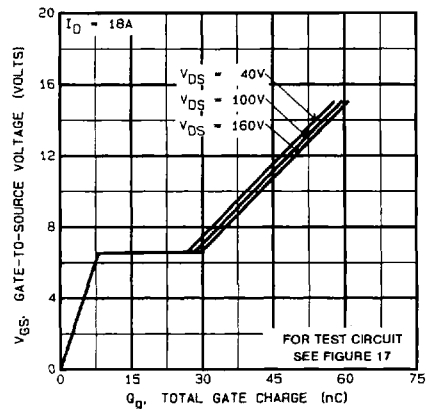


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

4
N-CHANNEL
POWER MOSFETS

Performance Curves (Continued)

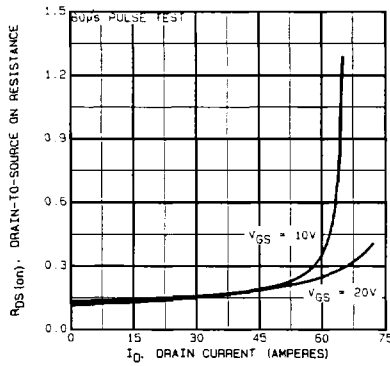


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

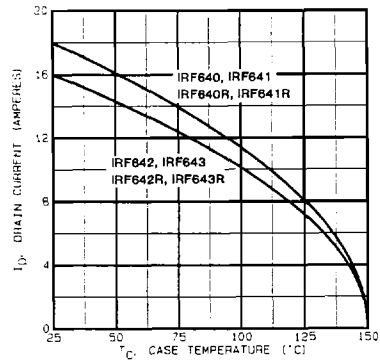


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

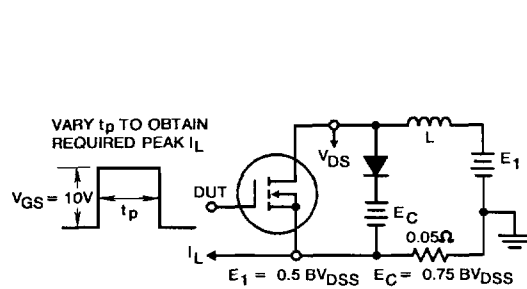


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

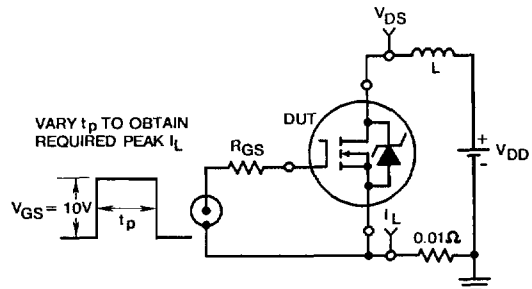


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

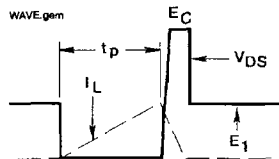


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

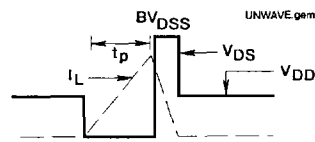


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

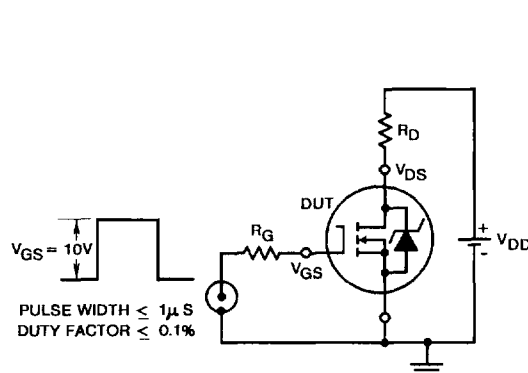


FIGURE 16. SWITCHING TIME TEST CIRCUIT

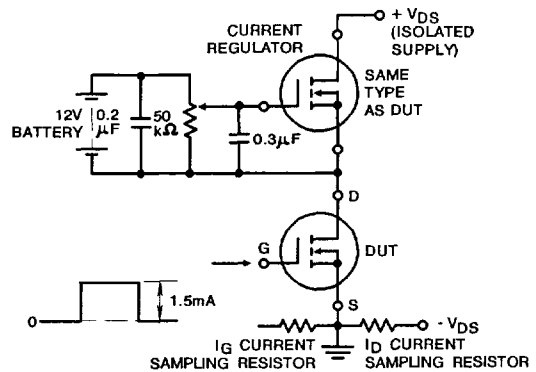


FIGURE 17. GATE CHARGE TEST CIRCUIT