LM8342 Programmable TFT V_{COM} Calibrator with Non-Volatile Memory

Check for Samples: LM8342

FEATURES

- I^2C Compatible Programmable DAC to Set the Output Current
- Ensured Monotonic DAC
- Non-Volatile Memory to Hold the Setting
- EEPROM in System Programmable
- No External Programming Voltage Required
- Maximum Interface Bus Speed is 400 kHz
- SON-10 Package

APPLICATIONS

- TFT Panel Factory Calibration
- Digital Potentiometer
- Programmable Current Sink

DESCRIPTION

The LM8342 is an integrated combination of a non-volatile register (7 bits EEPROM) and a DAC controlled current source. Using the LM8342, the V_{COM} calibration procedure is simplified by elimination of the potentiometer adjustment task. This adjustment task is currently performed at the factory using a trimmer adjustment tool and visual inspection.

The V_{COM} adjustment can be done electronically in production, using the I^2C compatible interface. The factory operator can physically view the screen head-on (frontal viewing) when performing this step, easing manufacturing especially for large TFT panels.

The V_{COM} level is typically at half AV_{DD} (determined by R1 and R2) and is buffered by the actual V_{COM} driver. By controlling the level of I_{OUT}, the V_{COM} level can be tuned. The current level at the output of the LM8342 is a fraction (1/128 to 128/128) of a maximum current which is set by R_{SET} and an analog reference (AV_{DD}). The actual fraction is determined by the 7-bit DAC. As a result, the output current of the LM8342 has a good temperature stability yielding a very stable V_{COM} adjustment. Controlling the DAC setting of the LM8342 is done via its I^2C compatible interface. The actual DAC setting is stored in a volatile register. Using a "Write to EE" command the data can be stored permanently in the embedded EEPROM. At power on of the device, the EEPROM data is copied to the volatile register, setting the DAC. At any time, the data in the EEPROM can be changed again via the I^2C compatible interface.

Typical Application
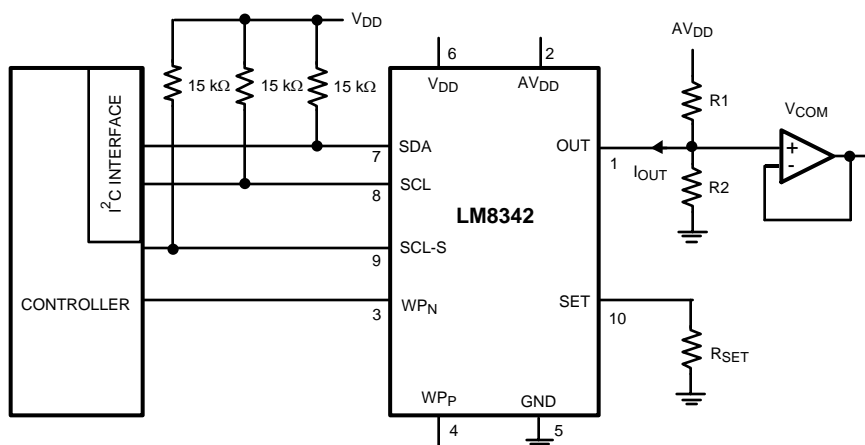
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

ESD Tolerance[2]	Human Body Model	SCL, SDA Pins	4 kV
		All Other Pins	2.5 kV
	Machine Model		250V
Supply and Reference Voltage		V_{DD}	5V
		AV_{DD}	20V
Storage Temperature Range			−65°C to +150°C
Junction Temperature[3]			+150°C
Soldering Information		Infrared or Convection (20 sec.)	235°C
		Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specified specifications and test conditions, see the Electrical Characteristics tables.
(2) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} — T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings[1]

Operating Temperature Range[2]	−40°C to 85°C
Digital Supply (V_{DD})[3]	2.25V to 3.6V
Digital Supply (V_{DD}) @ Programming	2.6V to 3.6V
Analog Reference (AV_{DD})[3]	4.5V to 18V
Package Thermal Resistance θ_{JA}[4]	52°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specified specifications and test conditions, see the Electrical Characteristics tables.
(2) Programming temperature range 0°C to 70°C .
(3) When AV_{DD} is in the voltage range of 4.5V to 13V, the supply voltage V_{DD} can be in 2.25V to 3.6V range. When AV_{DD} is in the voltage range from 13V to 18V, the supply voltage V_{DD} is limited to the 2.6V to 3.6V range
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} — T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Product Folder Links: *LM8342*

Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{DD} = 3V, AV_{DD} = 15V, V_{OUT} = 1/2 AV_{DD} and R_{SET} = 10 kΩ. **Boldface** limits apply at the temperature extremes. [1]

Symbol	Parameter		Conditions	Min[2]	Typ[3]	Max[2]	Units
Supply and Reference Current							
I_{DD}	Supply Current				40	**62**	µA
AI_{DD}	Analog Reference Current				8	**13**	µA
Control and Programming							
	SCL, SDA	Low Voltage				**0.3 * V$_{DD}$**	V
		High Voltage		**0.7 * V$_{DD}$**			
		Input Current				1	µA
		Frequency				400	kHz
	WP$_P$/WP$_N$ Low Level					**0.3 * V$_{DD}$**	V
	WP$_P$/WP$_N$ High Level			**0.7 * V$_{DD}$**			V
	WP$_N$ Input Current		V_{IH} = 3.0V [4]		100		µA
R_{ON}	SCL to SCL-S Switch Resistance				150		Ω
	SDA/SCL Input Capacitance				5		pF
	SCL-S Input Capacitance				3		pF
	SDA/SCL/SCL-S load current		No Supply, V_{SDA}, V_{SCL} = 3.6V			1	µA
	Programming Time		See [5]		200	**300**	ms
	I_{DD} @ Programming				10	**18**	mA
	Programming Cycles			1000			
	Reading Cycles			10000			
Output							
	Output Settling Time		95% of Final Value		10		µs
	Start-Up Time				30		µs
V_{OUT}	Output Voltage			V_{RSET} + 0.5V		AV_{DD}	V
I_{OUT}	Output Current	Adjustability			7		Bits
		Differential Non-Linearity	AV$_{DD}$ = 10V, V$_{OUT}$ = 5V	**−1**		**1**	LSB
		Zero Scale Error		−1		1.5	
		Full Scale Error		−4		4	
		Full Scale Range		**5**		**100**	µA
	Voltage Drift V_{RSET}			**−1**		**1**	LSB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by design or statistical analysis.
(3) Typical values represent the parametric norm at the time of characterization.
(4) On-Chip Pull Down Resistor of 30 kΩ.
(5) Programming temperature range 0°C to 70°C .

CONNECTION DIAGRAM
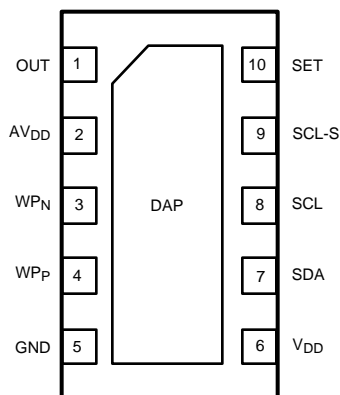
**Figure 1. 10-Pin SON
Top View**

PIN DESCRIPTIONS

Pin Name	Pin #	Function				
OUT	1	Current sink output, adjustable in 128 steps. See Application Section for details.				
AV_{DD}	2	Analog reference voltage input				
WP_N	3	Write protect (input)				
			READ (I^2C)	WRITE→Reg	WRITE→EE	SCL Switch
		WP_N = Low	yes	yes	no	open
		WP_N = High	yes	yes	yes	closed
WP_P	4	Inverted WP_N (output)				
GND	5	Ground				
V_{DD}	6	Supply voltage				
SDA	7	I^2C compatible serial data input/output				
SCL	8	I^2C compatible serial clock input				
SCL-S	9	Switched SCL connection. Serial clock input when WP_N is set to high				
SET	10	Maximum output current adjustment pin (see block diagram)				
DAP		Left floating or connect to GND				

Block Diagram
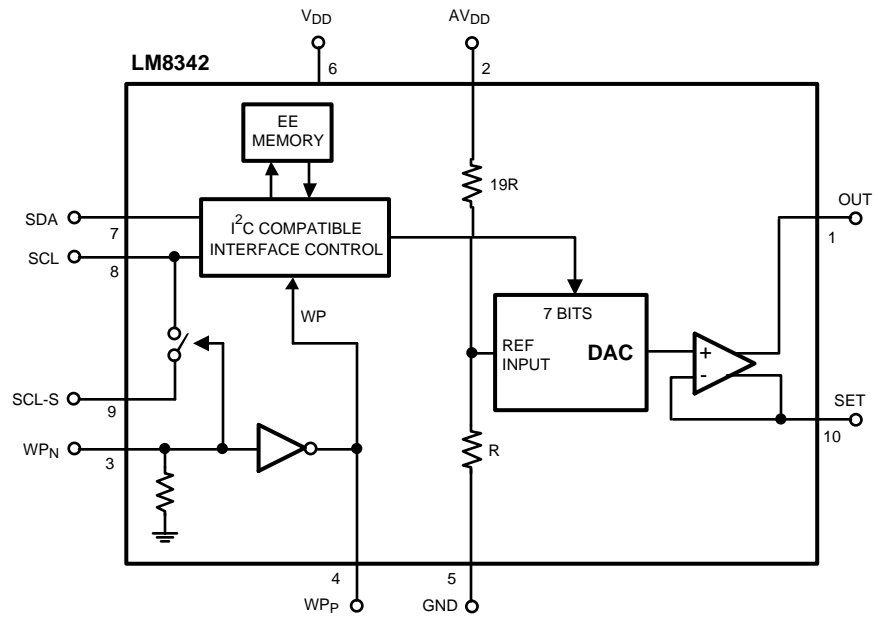
Typical Performance Characteristics

At T_J = 25°C, V_{DD} = 3V, AV_{DD} = 15V, V_{OUT} = 1/2 AV_{DD} and R_{SET} = 10 kΩ, unless otherwise specified.
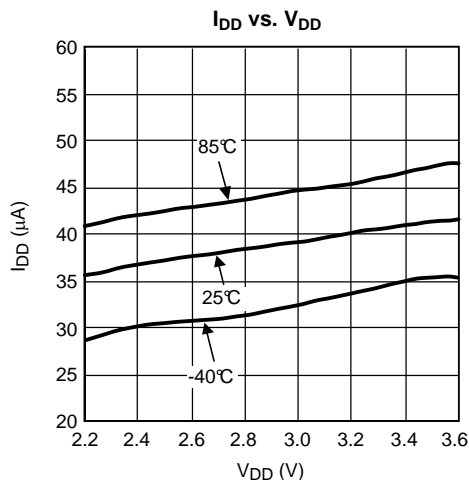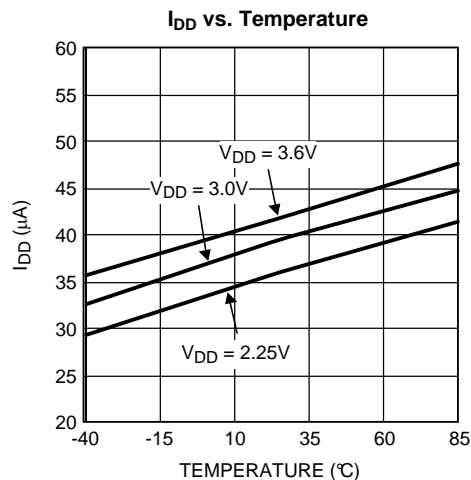
I_{DD} vs. V_{DD}

Figure 2.

I_{DD} vs. Temperature

Figure 3.

AV_{DD} Startup (Full Scale)

Figure 4.

V_{DD} Startup (Full Scale)

Figure 5.

I_{OUT} vs. R_{SET}

Figure 6.

I_{OUT} vs. R_{SET}

Figure 7.

Product Folder Links: *LM8342*
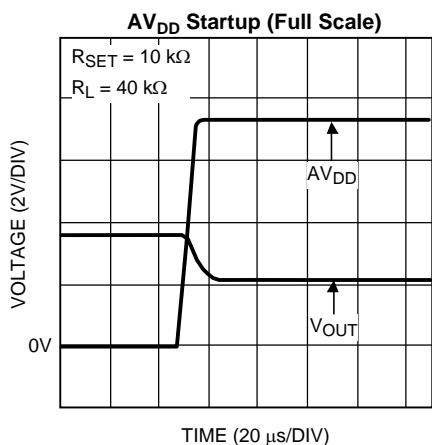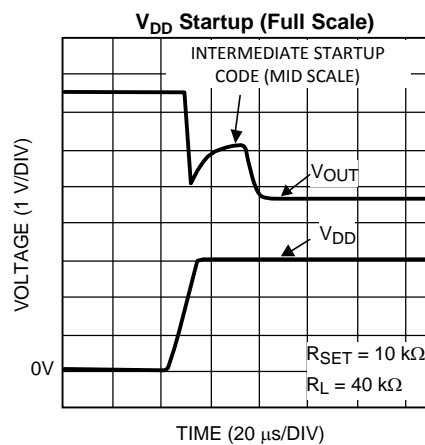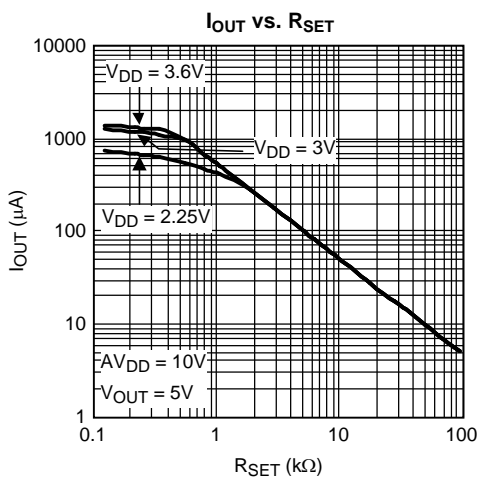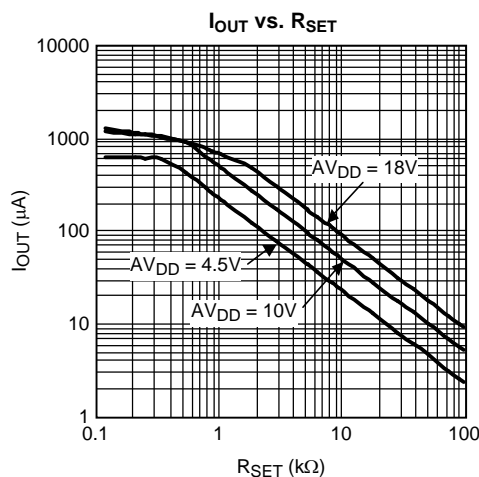
Typical Performance Characteristics (continued)

At T_J = 25°C, V_{DD} = 3V, AV_{DD} = 15V, V_{OUT} = 1/2 AV_{DD} and R_{SET} = 10 kΩ, unless otherwise specified.
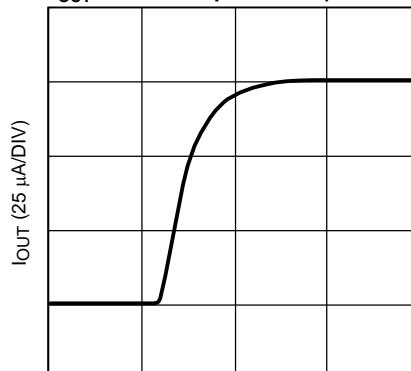
I_{OUT} Current Step Negative (Full Scale)
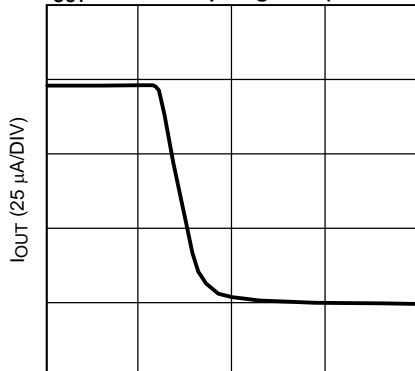
TIME (10 μs/DIV)

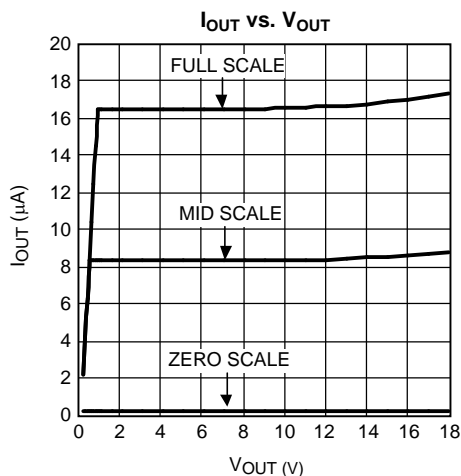**Figure 8.**

I_{OUT} Current Step Positive (Full Scale)

TIME (10 μs/DIV)

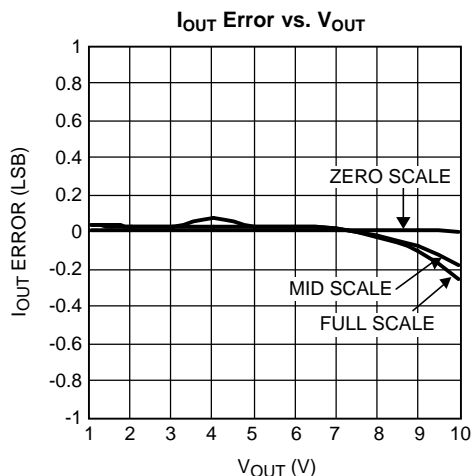**Figure 9.**

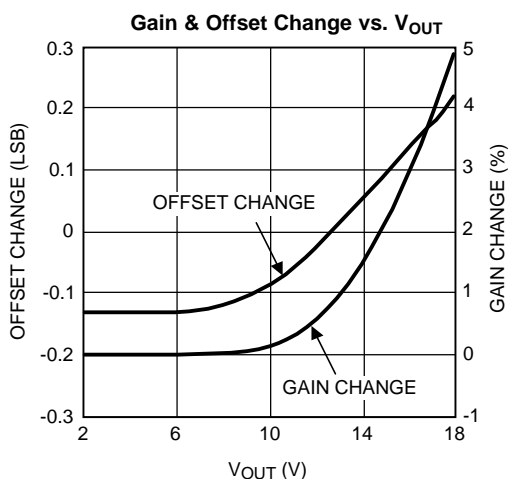**I_{OUT} vs. V_{OUT}**

Figure 10.

I_{OUT} Error vs. V_{OUT}

Figure 11.

Gain & Offset Change vs. V_{OUT}

Figure 12.

Differential Non-Linearity Error vs. DAC (V_{OUT} = 18V)
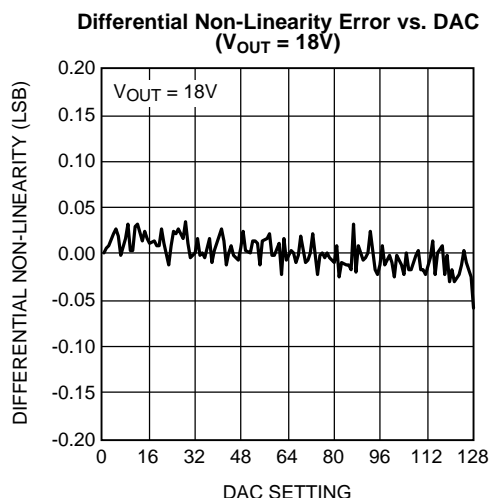
Figure 13.

Typical Performance Characteristics (continued)

At T_J = 25°C, V_{DD} = 3V, AV_{DD} = 15V, V_{OUT} = 1/2 AV_{DD} and R_{SET} = 10 kΩ, unless otherwise specified.

I_{OUT} Error vs. V_{DD}

Figure 14.

I_{OUT} Error vs. AV_{DD}

Figure 15.

I_{OUT} Error vs. Temperature

Figure 16.

Total Unadjusted Error vs. DAC

Figure 17.

Integral Non-Linearity Error vs. DAC

Figure 18.

Product Folder Links: *LM8342*

Typical Performance Characteristics (continued)

At T_J = 25°C, V_{DD} = 3V, AV_{DD} = 15V, V_{OUT} = 1/2 AV_{DD} and R_{SET} = 10 kΩ, unless otherwise specified.

Differential Non-Linearity Error vs. DAC
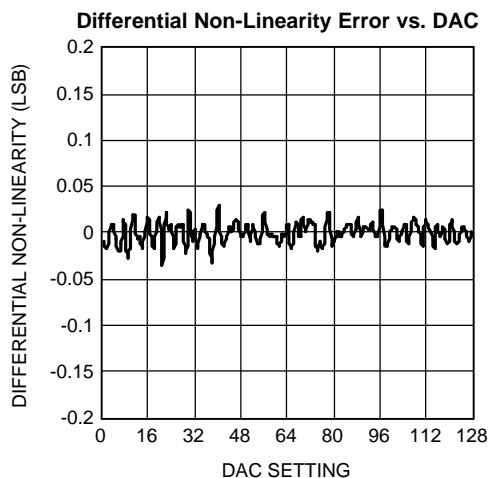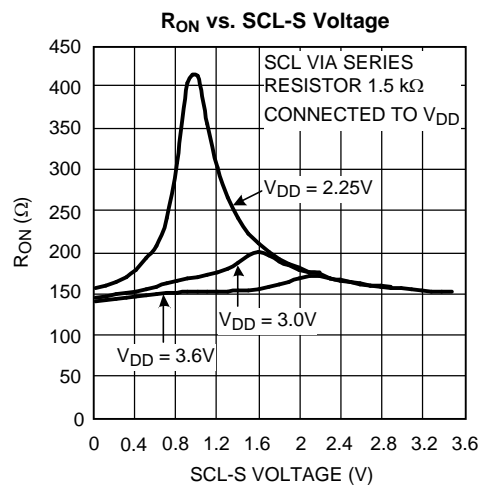
Figure 19.

R_{ON} vs. SCL-S Voltage
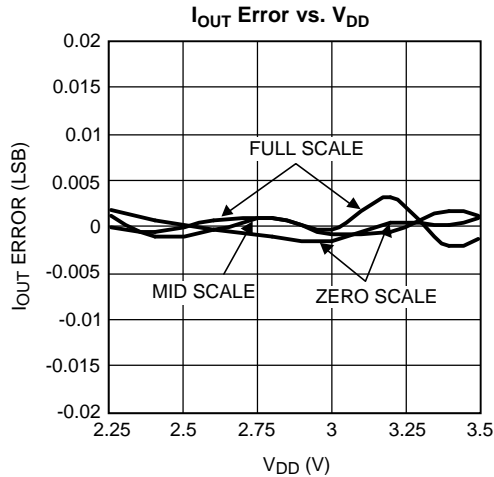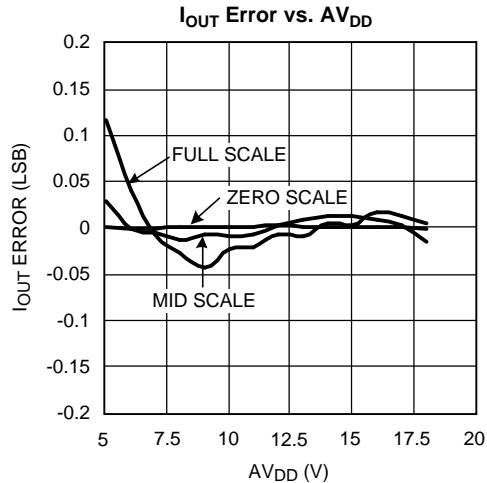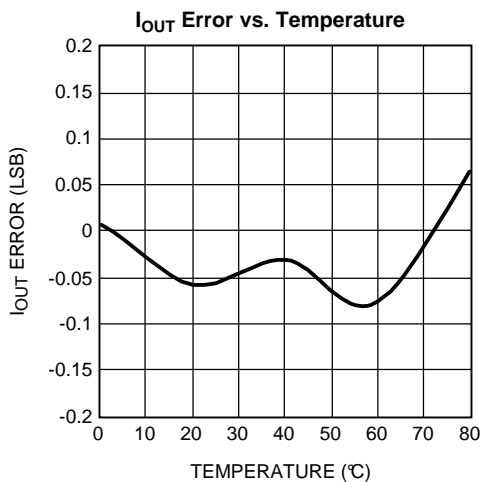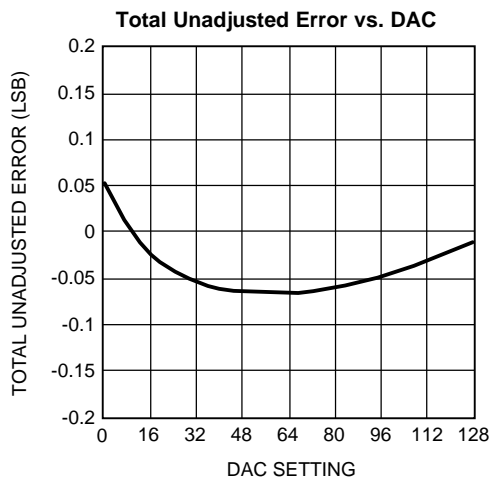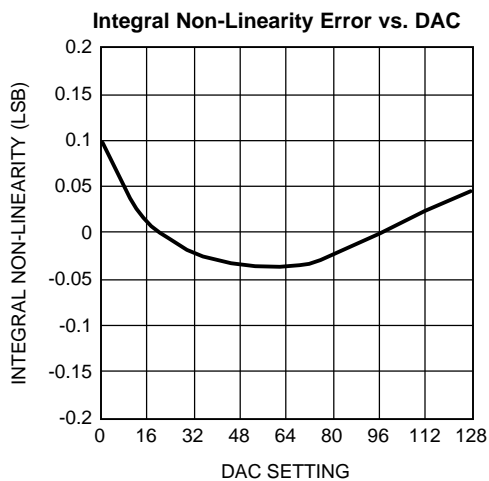
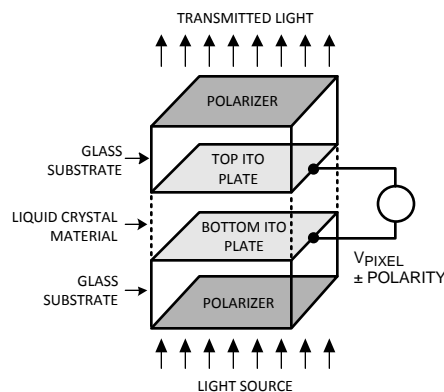**Figure 20.**

APPLICATION SECTION

INTRODUCTION

The LM8342 is an integrated combination of a digitally controlled current sink and a non-volatile register (7 bits EEPROM). Programming the register can be done using the I²C compatible interface. The LM8342 replaces the potentiometer adjustment, and thereby simplifies the V_{COM} calibration procedure. With the LM8342, the factory operator can physically view the screen head-on when performing this step, easing manufacturing especially for large TFT panel sizes.

The following sections discuss the principle of operation of a TFT-LCD and, subsequently give a description of how to use the LM8342, including the I²C compatible interface and control inputs. After this, two typical LM8342 configurations are presented. Subsequently an evaluation system is introduced, including a μC-board programming using the I²C compatible interface. At the end of this application section board layout recommendations are given.

PRINCIPLE OF OPERATION OF A TFT-LCD

This section offers a brief overview of the principle of operation of TFT-LCD's. It gives a detailed description of how information is presented on the display. Further an explanation of how data is written to the screen pixels and how the pixels are selected is included.

Figure 21. Individual LCD Pixel

Figure 21 shows a simplified illustration of an individual LCD pixel. The top and bottom plates of a pixel consist of Indium-Tin Oxide (ITO), which is a transparent, electrically conductive material. ITO is at the inner surfaces of two glass substrates that are the front and back glass panels of a TFT display. Sandwiched between two ITO plates is an insulating material (liquid crystal). Liquid crystals alter the polarization of light, depending on how much voltage (V_{PIXEL}) is applied across the two plates. Polarizers are placed on the outer surfaces of the two glass substrates. In combination with the liquid crystal, the polarizers create an electrically variable light filter that modulates light transmitted from the back to the front of a display. A pixel's bottom plate is at the backside of a display where a light source is applied, and the top plate is at the front, facing the viewer. For most TFT displays, a pixel transmits the greatest amount of light when $V_{PIXEL} \leq \pm 0.5V$, and it becomes less transparent as the voltage increases with either positive or negative polarity.
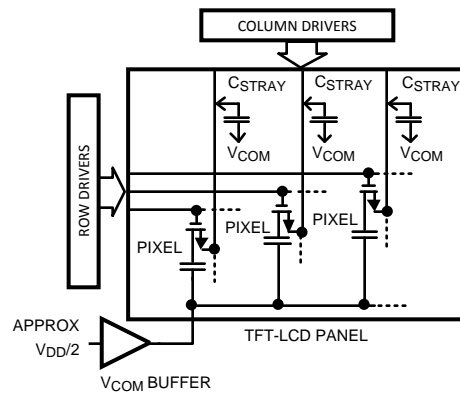
Product Folder Links: *LM8342*

Figure 22. TFT Display

Figure 22 shows a simplified diagram of a TFT display, showing how individual pixels are connected to the row, column and V_{COM} driver. Each pixel is represented by a capacitor with an NMOS transistor connected to its top plate. Pixels in a TFT panel are arranged in rows and columns. Row lines are connected to the NMOS gates, and column lines to the NMOS sources. The back plate of every pixel is connected to a common voltage called V_{COM}. The voltage applied to the top plates (i.e. Gamma Voltage) controls the pixel brightness. The column drivers supply this gamma voltage via the column lines, and 'write' this voltage to the pixels one row at a time. This is accomplished by having the row drivers selecting an individual row of pixels when the column drivers write the gamma voltage levels. The row drivers sequentially apply a large positive pulse (typically 25V to 35V) to each row line. This turns on the NMOS transistors connected to an individual row, allowing voltage from the column lines to be written to the pixels.
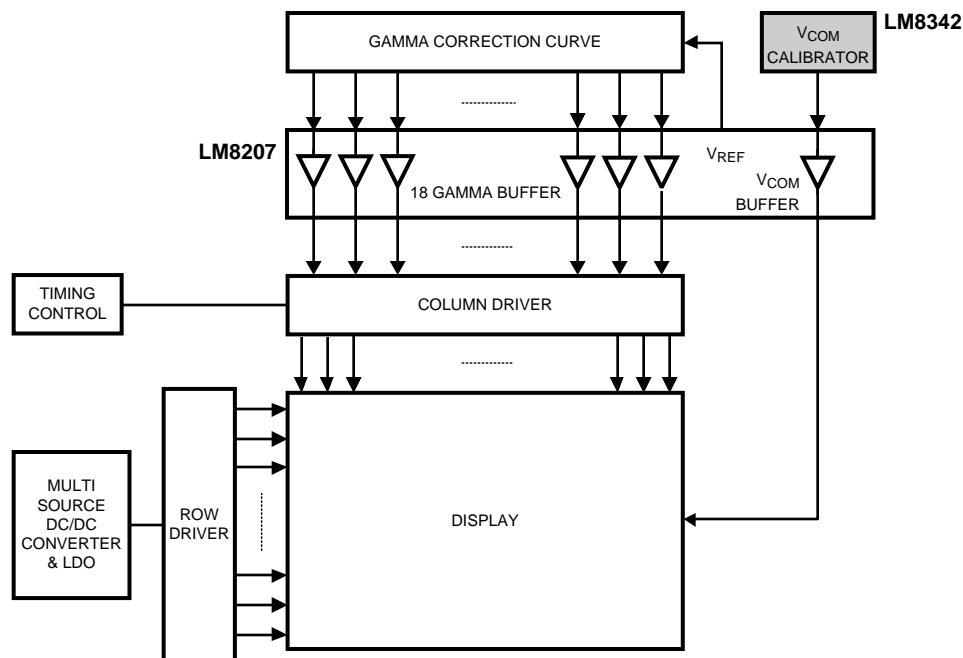
Figure 23. TFT Panel Block Diagram

Figure 23 shows a block diagram of a TFT panel. The V_{COM} buffer supplies a common voltage (V_{COM}) to all the pixels in a TFT panel. In general, V_{COM} is a DC voltage that is in the middle of the gamma voltage range. Screen performance can be optimized by tuning the V_{COM} voltage in the calibration procedure. Using the LM8342, the V_{COM} calibration procedure is simplified by elimination of the potentiometer adjustment task. This task is currently performed at the factory using a trimmer adjustment tool and visual inspection, when using a stable reference voltage and a potentiometer as a voltage divider to generate the V_{COM} voltage.

PRINCIPLE OF OPERATION OF THE LM8342

The LM8342 is an integrated combination of a digitally controlled current sink and a non-volatile register (7 bits EEPROM). Writing data can be done using the I²C compatible interface. Data can be written to a volatile register and can also be stored in the non-volatile EEPROM. A simplified block diagram of the LM8342 is given in Figure 24.
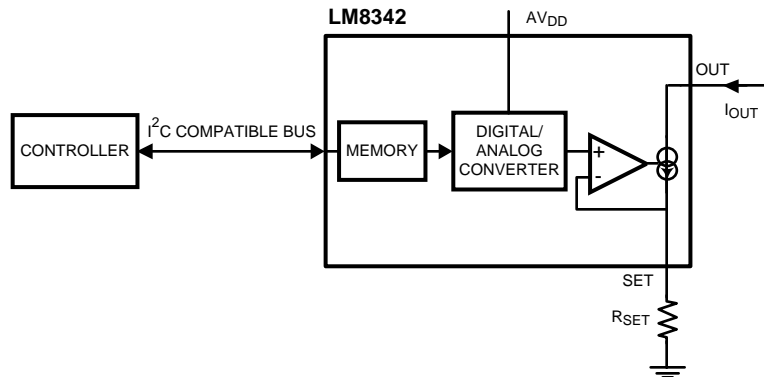
Figure 24. Block Diagram of the LM8342

The maximum output current of the LM8342 can be defined using an external resistor R_{SET} in combination with an analog reference voltage AV_{DD}. This maximum current can be calculated using Equation 1.

$$I_{OUT\_MAX} = \frac{AV_{DD}}{20} \times \frac{1}{R_{SET}}$$

(1)

The operating range for the output current is given in the Electrical Characteristics table. Variations of the voltage reference AV_{DD} or the external resistor R_{SET} will affect this output current. Using a resistor with a low temperature coefficient is recommended.

The relative value of I_{OUT} with respect to the maximum current can be controlled digitally in 128 steps, using the internal DAC. This results in an output current described by Equation 2.

$$I_{OUT} = I_{OUT\_MAX} \times \frac{DAC_{10} + 1}{128}$$

(2)

Using the serial interface bus the operator can store the DAC value in the LM8342s 7-bits volatile register temporarily, or permanent in the EEPROM. During a start-up sequence the LM8342 will copy the contents of the EEPROM to the register setting the DC value.

CONTROLLING THE DEVICE

The LM8342s current sink can be programmed using a serial interface bus. Additional functions (e.g. storing data in the EEPROM) can be controlled in combination with external inputs. Table 1 shows the pins of the LM8342 and gives a short functional description.

Table 1. Pin Descriptions

Pin name	Function
SDA & SCL (Serial interface bus)	The LM8342 output current can be controlled using the serial I²C compatible interface. This 2-Wire interface uses a clock and a data signal. New values can be written to the memory, or the current value can be read back from the device. The I²C compatible interface is discussed in more detail in the next chapter.
AV_{DD}	Analog reference voltage for the DAC.
V_{DD}	Supply voltage for both the analog and digital circuitry.
SET	An external resistor R_{SET} connected to the SET pin determines the maximum output current, see Equation 1.
OUT	The output of the programmable current sink.

Table 1. Pin Descriptions (continued)

Pin name	Function
SCL-S	For in-circuit PCB testing, the LM8342 can use the additional Switched SCL signal (SCL-S) input for applying the SCL clock signal.
WP$_N$	"Write Protect Not" (Input) has 2 functions: 1. Prohibits programming the EEPROM, when low or left floating (Internal a pull-down resistor is connected) When WP$_N$ is set to a low level, only the volatile register is accessible. If WP$_N$ is set to a high level also the EEPROM is accessible. Actual writing to the EEPROM or the register is done using the "P-bit" in the serial communication. 2. WP$_N$ switches the SCL-S clock line. When WP$_N$ is set to a high level SCL-S is connected to SCL. The operator should turn off the original SCL clock.
WP$_P$	Write Protect Signal (Output). This is the inverted WP$_N$ signal.

I²C SERIAL INTERFACE BUS

The LM8342 supports an I²C compatible communication protocol, which is a bidirectional bus oriented communication protocol. Any device that sends data on the bus is defined as a transmitter and the receiving device as a receiver. The I²C compatible communication protocol uses 2 wires: SDA (Serial Data Line) and SCL (Serial Clock Line). For both lines an external pull-up resistor, connected to the supply voltage, is required. The device controlling the bus is known as the master, and the device or devices being controlled are the slaves. Each device has its own specific address. The address of the LM8342 is 9E$_{HEX}$. The master initiates the communication and provides the clock. The LM8342 always operates as a slave. A typical system using an I²C compatible interface bus is given in Figure 25.
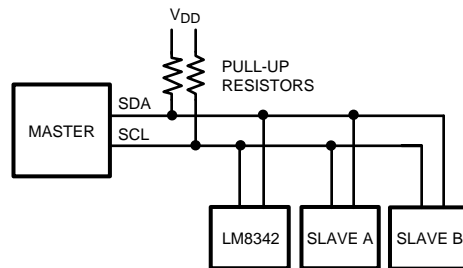
Figure 25. System Using an I²C compatible Bus

The LM8342 can be used in an I²C compatible system. All specifications of the LM8342, dealing with the interface bus, are ensured by design. Except for the bus speed, which is specified in the Electrical Characteristics table.

KEY ASPECT OF I²C COMPATIBLE COMMUNICATION

In this section a brief overview is presented, discussing the key aspect of I²C compatible communication. Figure 26 shows the timing aspects of the I²C compatible serial interface.
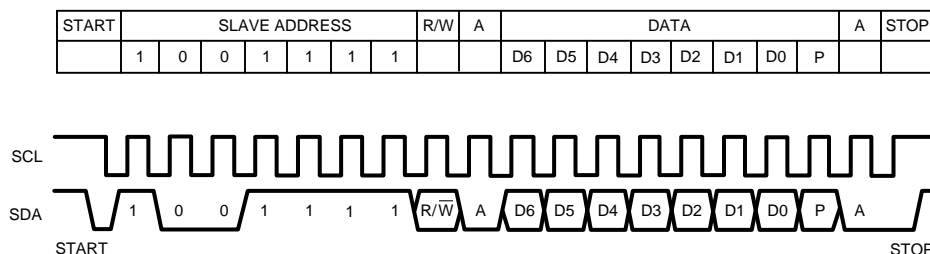
Figure 26. Timing Diagram

The timing diagram shows the major aspect of the communication protocol and represents a typical data stream. In case a master wants to setup a data transfer, it tests if "the bus is busy." If it is not busy, then the master starts the data transfer by creating a "start data transfer" situation. Accordingly the corresponding receiver is selected by sending the appropriate "slave address." This receiver gives an "acknowledge" on recognizing its address on the bus. The master continues the data transfer by sending the data stream. Again the receiver gives an "acknowledge" after receipt. Depending on the amount of data the master will continue or create a "stop data transfer" situation. Table 2 gives a more detailed description of the I^{2}C compatible communication.

Table 2. Detailed Description of I^{2}C compatible Communication Definitions

Bus not busy	The I^{2}C compatible bus is not busy when both data (SDA) and clock (SCL) lines remain HIGH. The controller can initiate data transfer only when the bus is not busy.
Start Data Transfer	Starting from an idle state (bus not busy) a START condition consists of a HIGH to LOW transition of SDA while SCL is HIGH. All commands must start with a START condition.
Slave address	After generating a start condition, the master transmits a 7-bit slave address. (The LM8342 uses the 8th bit for selecting the R/W operation, but this does not affect the address.) The address for the LM8342 is 9E$_{HEX}$.
R/W-bit	If the value of the R/W bit is HIGH, the data is read from the register of the LM8342. Otherwise the current DAC setting is written to the LM8342.
Acknowledge	A receive device, when addressed, is obliged to generate an "acknowledge" after the reception of each byte. The master generates an extra clock cycle that is associated with this acknowledge bit. The receiver has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of SCL, with respect to the SCL timing specifications.
Data byte	A data byte consists of 8 bits. 7 bits are used for the DAC setting of the LM8342. The 8th bit is known as the P-bit.
P-bit	The function of the P-bit depends on the Read/Write operation (R/W-bit). During a Read operation of the LM8342, the P-bit indicates the programming state of the EEPROM. During a Write operation, the register or both the register and the EEPROM of the LM8342 can be selected as destination. A more detailed description of the P-bit is given in Table 3 .
Stop Data Transfer	A STOP condition consists of a LOW to HIGH transition of SDA while SCL is HIGH. All operations must be ended with a STOP condition.

Table 3. P-bit Truth Table

Operation	P-bit	Description
Read	1	Programming Ready
Read	0	Programming Busy (don't turn off the device)
Write	1	Register Write
Write	0	EEPROM Write

The LM8342 can be used in I^{2}C compatible systems with clock speeds of up to 400 kbps (Fast mode). For low speed applications, an initial resistor value for the pull-up resistors is 15 kΩ is suitable. When increasing the speed of the interface bus, the user should decrease the value of the pull-up resistors.

Typical Application

The following section discusses two typical applications for the LM8342. In the first application the LM8342 is used as a programmable current sink, for example to drive a programmable bias generator. In the second application the LM8342 is used to adjust the voltage level of a V$_{COM}$ driver.

PROGRAMMABLE CURRENT SINK

As described in the "Principle of Operation of the LM8342" section the LM8342 basically operates as a programmable current sink. Figure 27 shows a general current sink application.
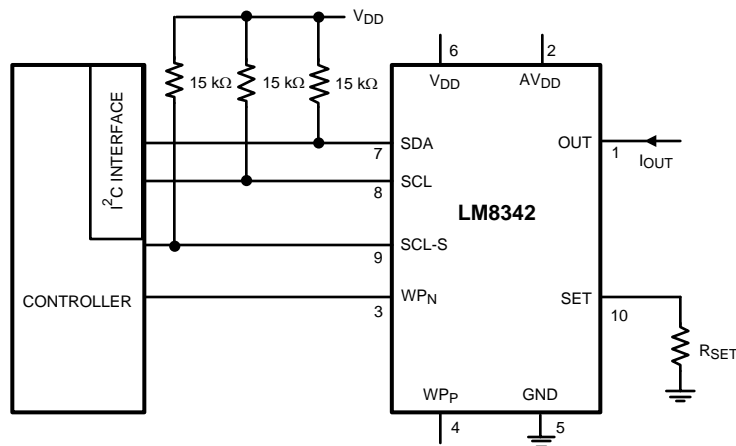
Figure 27. Programmable Current Sink

The output current of the LM8342 can be calculated using Equation 3.

$$I_{OUT} = \frac{AV_{DD}}{20} \times \frac{1}{R_{SET}} \times \frac{DAC_{10} + 1}{128}$$

(3)

DRIVING A V_{COM} LEVEL

Another typical application, given in Figure 28, is using the LM8342 to adjust the "voltage tap" of a resistive voltage divider. The V_{COM} driver buffers the "voltage tap" in this application.
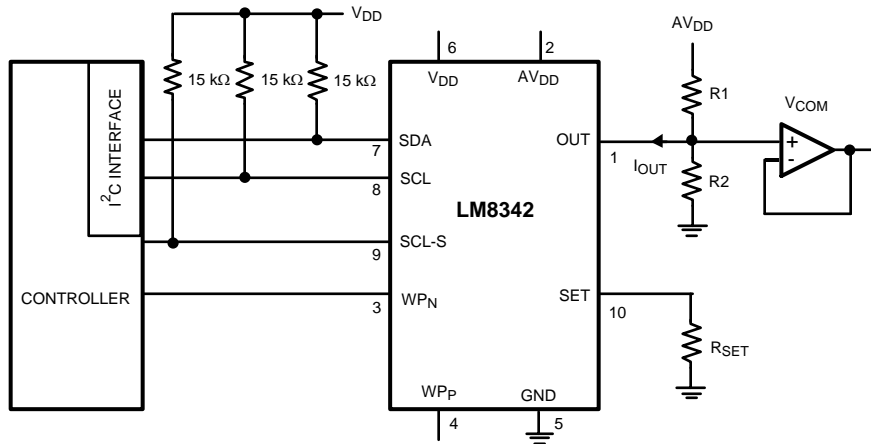
Figure 28. Typical Application Driving a V_{COM} Level

The voltage level of the V_{COM} driver, for a general setting of (DAC_{10}) , is calculated using Equation 4.

$$V_{COM} = AV_{DD} \times \left(\frac{R2}{R1 + R2} \right) \times \left(1 - \frac{(DAC_{10} + 1) \times R1}{128 \times R_{SET} \times 20} \right)$$

(4)

For calibrating the V_{COM} level (see Figure 28) the tuning range of the design needs to be aligned to the required V_{COM} tuning range (ΔV_{COM}). Figure 29 gives a graphical presentation of the desired voltage levels.
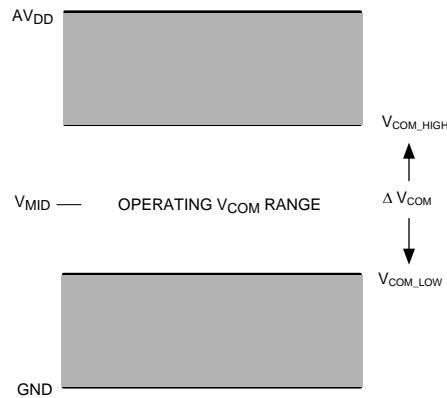
Figure 29. V$_{COM}$ Voltage Levels

Assume the calibrator needs to cover the voltage range given in Equation 5.

$$\Delta V_{COM} = V_{COM\_HIGH} - V_{COM\_LOW}$$

(5)

The limits of V$_{COM}$ for DAC$_{10}$ = 0 (high limit) and DAC$_{10}$ = 127 (low limit) are given by:

$$V_{COM\_HIGH} = AV_{DD} \times \left(\frac{R2}{R1 + R2}\right) \times \left(1 - \frac{R1}{128 \times R_{SET} \times 20}\right)$$

(6)

$$V_{COM\_LOW} = AV_{DD} \times \left(\frac{R2}{R1 + R2}\right) \times \left(1 - \frac{R1}{R_{SET} \times 20}\right)$$

(7)

Using Equation 5, Equation 6, and Equation 7 the value for resistors R1 and R2 can be obtained, resulting in Equation 8 and Equation 9:

$$R1 = \frac{40 \times R_{SET} \times \Delta V_{COM}}{AV_{DD} + \Delta V_{COM}}$$

(8)

and

$$R2 = \frac{40 \times R_{SET} \times \Delta V_{COM}}{AV_{DD} - \Delta V_{COM}}$$

(9)

Table 4 gives an overview of resistor values for a typical value of AV$_{DD}$, and 2 R$_{SET}$ values. All settings are for a V$_{COM}$ level at V$_{MID}$ = ½ AV$_{DD}$, and a maximum variation of ΔV$_{COM}$.

$$V_{MID} - \frac{1}{2} \Delta V_{COM} < V_{COM} < V_{MID} + \frac{1}{2} \Delta V_{COM}$$

(10)

Table 4. Overview Resistor Values for Different R$_{SET}$ Settings at AV$_{DD}$ = 15V

| AV$_{DD}$ = 15V (V$_{COM}$ Level = 7.5 V)					
R$_{SET}$ = 10 kΩ			R$_{SET}$ = 45 kΩ		
ΔV$_{COM}$ (V)	R1 (Ω)	R2 (Ω)	ΔV$_{COM}$ (V)	R1 (Ω)	R2 (Ω)
±0.5	25k	28.6k	±0.5	113k	129k
±1	47.1k	61.5k	±1	212k	277k
±1.5	66.7k	100k	±1.5	300k	450k
±2	84.2k	146k	±2	379k	655k

Product Folder Links: *LM8342*

Table 4. Overview Resistor Values for Different R$_{SET}$ Settings at AV$_{DD}$ = 15V (continued)

±2.5	100k	200k	±2.5	450k	900k
±3	114k	267k	±3	514k	1.2M

EVALUATION SYSTEM

For the LM8342 a complete evaluation system is available, including two boards. Figure 30 gives a schematic representation.

- **LM8342 Evaluation Board**This board demonstrates the functionality of the LM8342 using the I^{2}C compatible interface for communication. The LM8342 can easily be demonstrated in 2 applications:
  - Programmable current sink
  - Programmable V$_{COM}$ level driver
- **LM8342 Programmer Board**This test board has dedicated functionality for communicating with the LM8342, using the I^{2}C compatible interface. This board can operate in two different modes:
  - **Write mode:** The digitized value of a potentiometer setting is written to the LM8342. The user can select on the programmer board to write the data to the register or to store the data in the EEPROM.
  - **Read mode:** The board reads the stored values from the LM8342's EEPROM and presents this data onto a 3-digit display.
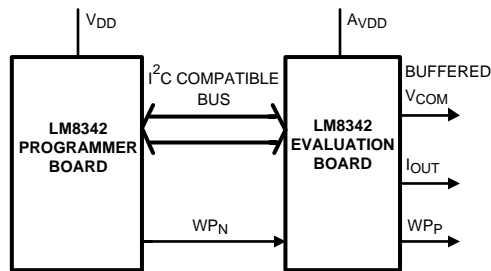
Figure 30. LM8342 Evaluation System

LAYOUT RECOMMENDATIONS

A proper layout is necessary for optimum performance of the LM8342. A low impedance and proper ground plane (free of disturbances) is recommended, since a current of up to 10 mA can flow with HF contents during programming. The traces from the GND pin to the ground plane should be as short as possible. It is recommended to place decoupling capacitors close to the V$_{DD}$ and AV$_{DD}$ pins. Connections of these decoupling capacitors to the ground plane should be short.

As SET is a sensitive input, crosstalk to that pin should be prevented. Special care should be taken when routing the interface connections. The signals on the serial interface can be more than 60 dB larger than the equivalent LSB at the SET input pin. Crosstalk between the interface bus and R$_{SET}$ results in disturbance of the output current I$_{OUT}$ of the LM8342.

For applications requiring a low output current (using high values for R$_{SET}$ in combination with low DAC settings) special attention should be paid to the parasitic capacitance (C$_{PAR}$) parallel to R$_{SET}$. For C$_{PAR}$ larger than tens of pF, a small (<1 LSB) unwanted ripple at the output current might be obtained. It is recommended to place the R$_{SET}$ resistor close to the LM8342, in combination with a good board layout to reduce this parasitic capacitance.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B   **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM8342SD	ACTIVE	WSON	DSC	10		TBD	Call TI	Call TI	-40 to 85	L8342	Samples
LM8342SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L8342	Samples
LM8342SDX	ACTIVE	WSON	DSC	10		TBD	Call TI	Call TI	-40 to 85	L8342	Samples
LM8342SDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L8342	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
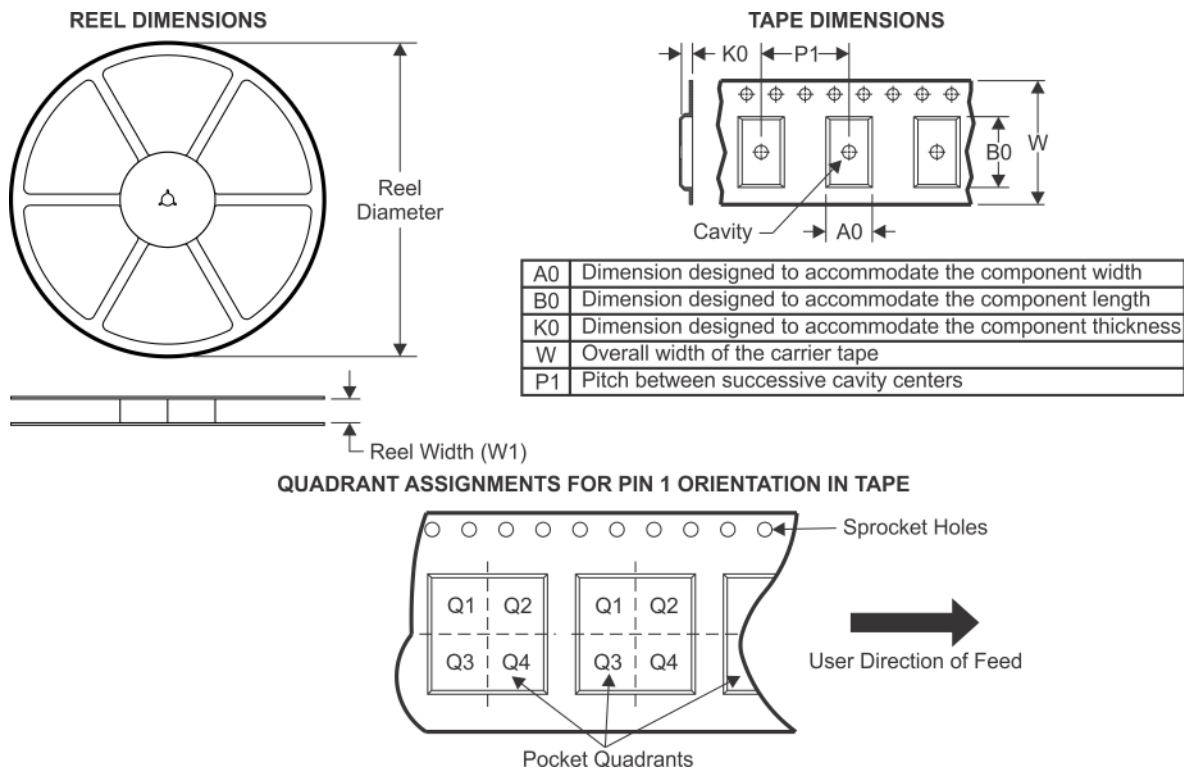
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8342SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM8342SDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8342SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LM8342SDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

DSC0010A
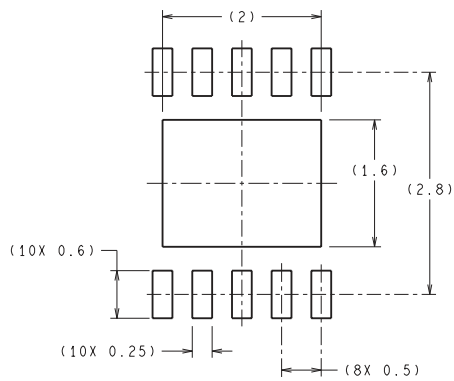
RECOMMENDED LAND PATTERN

(2)

(1.6)   (2.8)

(10X 0.6)

(10X 0.25)   (8X 0.5)
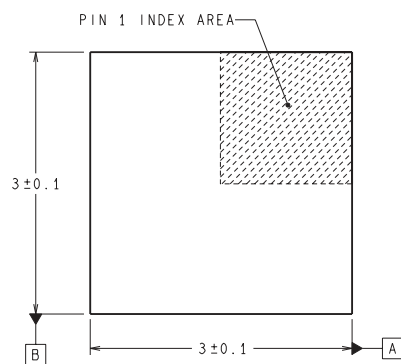
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

(0.1)

PIN 1 INDEX AREA

3 ±0.1

B   3 ±0.1   A

C   0.8 MAX

2 ±0.1

(45° X 0.25)

PIN 1 ID

1   5

1.6 ±0.1

10   6

10X 0.25±0.05

⊕ 0.1Ⓜ C AⓈ BⓈ

10X 0.4±0.1

8X 0.5

2X 2.0
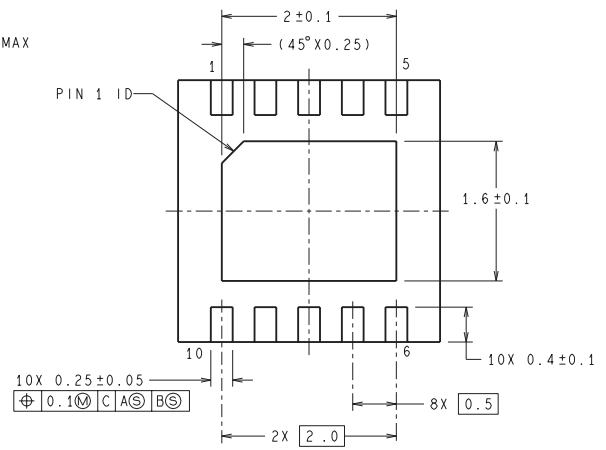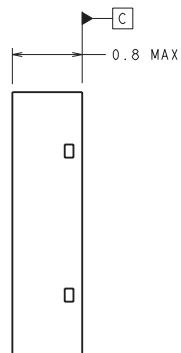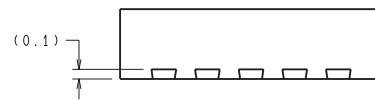
SDA10A (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		